[Notes]
Smart Configurator for RH850

R20TS0679EC0100
Rev.1.00
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Outline

When using Smart Configurator for RH850, note the following points.

1. When using CSI Master and CSI Slave with CSIG
2. When using CSI Master with CSIH
3. When using Data CRC
4. When using One-Pulse Output and One-Shot Pulse Output
5. When using PWM Output and Triangle PWM Output

1. When using CSI Master and CSI Slave with CSIG

1.1 Applicable Products

Smart Configurator for RH850 V1.3.0 or previous version

1.2 Applicable Devices

RH850 family: RH850/F1KM group

- RH850/F1KM-S1 (48-pin, 64-pin, 80-pin, and 100-pin products)
- RH850/F1KM-S4 (100-pin, 144-pin, 176-pin, and 233-pin products)

1.3 Details

When using CSI master mode and CSI Slave mode on the following peripherals, data transmission occurs error when data length are selected as “2 bits”, “3 bits”, “4 bits”, “5 bits” and “6 bits” on GUI (refer to Figure 1-1 Setting of CSI Master Data length and Figure 1-2 Setting of CSI Slave Data length).

- RH850/F1KM-S1: 48-pin, 64-pin, 80-pin, 100-pin products

  CSIG0
- RH850/F1KM-S4: 100-pin products

  CSIG0
- RH850/F1KM-S4: 144-pin products

  CSIG0, CSIG1
- RH850/F1KM-S4: 176-pin, 233-pin products

  CSIG0, CSIG1, CSIG2, CSIG3

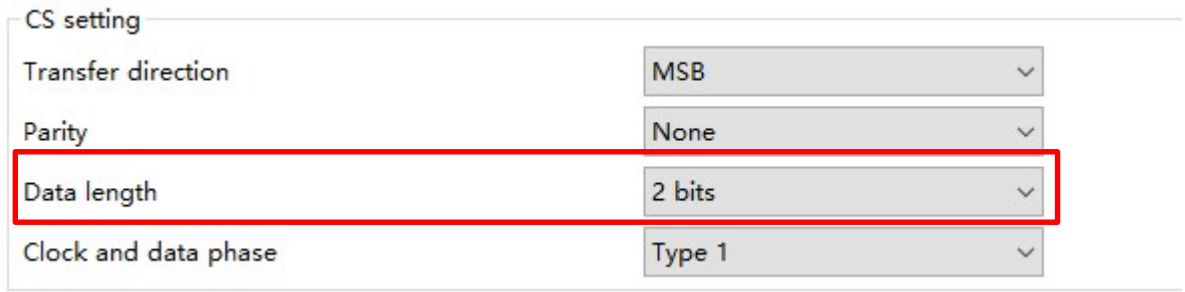

Figure 1-1 Setting of CSI Master Data length

Figure 1-2 Setting of CSI Slave Data length

1.4 Workaround

Please don't select data length as "2 bits", "3 bits", "4 bits", "5 bits" and "6 bits" on CSI Master and CSI slave GUI when using CSIG.

1.5 Schedule for Fixing the Problem

This problem will be fixed in the next version. (Scheduled to be released in May 2021.)

2. When using CSI Master with CSIH

2.1 Applicable Products

Smart Configurator for RH850 V1.3.0 or previous version

2.2 Applicable Devices

RH850 family: RH850/F1KM group

- RH850/F1KM-S1 (48-pin, 64-pin, 80-pin, and 100-pin products)
- RH850/F1KM-S4 (100-pin, 144-pin, 176-pin, and 233-pin products)

2.3 Details

When using CSI mater mode on the following peripherals and specifying "High level" as CS active signal (refer to Figure 2-1 Setting of Active output level), the data transmission with slave device failed.

- RH850/F1KM-S1: 48-pin, 64-pin products

  CSIH0
- RH850/F1KM-S1: 80-pin products

  CSIH0, CSIH1, CSIH2
- RH850/F1KM-S1: 100-pin products

  CSIH0, CSIH1, CSIH2, CSIH3
- RH850/F1KM-S4: 100-pin, 144-pin, 176-pin, 233-pin products

  CSIH0, CSIH1, CSIH2, CSIH3

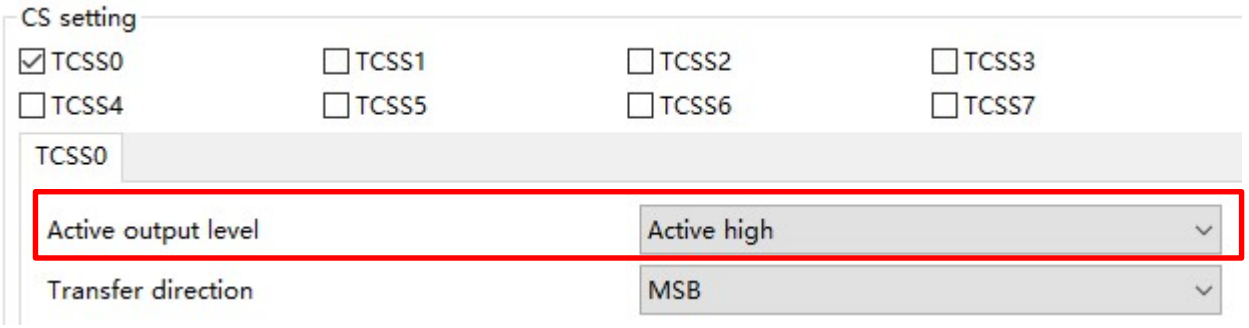

Figure 2-1 Setting of Active output level

2.4 Workaround

User can manually modify the register setting code in the following source file

- Source file: “<Configuration-name>.c”.
- Function: “void R_<*Configuration-name*>_ Create (void)”

Note: If code is generated again, the previous state is restored. Modification is necessary each time you perform code generation.

The following is an example of the required modification when <*Configuration-name*> is Config_CSIH0 in the RH850/F1KM group. Manually add the code in red.

```
void R_Config_CSIH0_Create(void)
{
    uint32_t tmp_port;


    CSIH0.CTL0 = _CSIH_OPERATION_CLOCK_STOP;
    ……
    /* Set CSIH0 control setting */
    CSIH0.CTL1 = _CSIH_INTERRUPT_TIMING_NORMAL |
_CSIH_DATA_CONSISTENCY_CHECK_DISABLE | _CSIH_HANDSHAKE_DISABLE |
                _CSIH_CHIPSELECT_SIGNAL_HOLD_ACTIVE |
_CSIH_SLAVE_SELECT_DISABLE | _CSIH_CHIPSELECT0_ACTIVE_HIGH;
    ……
}
```

2.5 Schedule for Fixing the Problem

This problem will be fixed in the next version. (Scheduled to be released in May 2021.)

3. When using Data CRC

3.1 Applicable Products

Smart Configurator for RH850 V1.1.0 or later version

3.2 Applicable Devices

RH850 family: RH850/F1KM group

- RH850/F1KM-S1 (48-pin, 64-pin, 80-pin, and 100-pin products)
- RH850/F1KM-S4 (100-pin, 144-pin, 176-pin, and 233-pin products)

3.3 Details

When using Data CRC on the following peripherals and specifying “16 bits” or “8 bits” as the CRC input bit width (refer to Figure 3-1 Setting of CRC input bit width), the CRC result will be wrong.

- RH850/F1KM-S1: 48-pin, 64-pin products

  DCRA0
- RH850/F1KM-S1: 80-pin, 100-pin products

  DCRA0, DCRA1, DCRA2, DCRA3
- RH850/F1KM-S4: 100-pin, 144-pin, 176-pin, 233-pin products

  DCRA0, DCRA1, DCRA2, DCRA3

Figure 3-1 Setting of CRC input bit width

3.4 Workaround

User can manually modify 2 functions code in the following source file

- Source file: “<Configuration-name>.c”.
- Functions:
  1) void R_<*Configuration-name*>_Input16bitData(const uint16_t * data, uint32_t data_num)
  2) void R_<*Configuration-name*>_Input8bitData(const uint8_t * data, uint32_t data_num)

Note: If code is generated again, the previous state is restored. Modification is necessary each time you perform code generation.

The following is an example of the required modification when <*Configuration-name*> is Config_DCRA0 in the RH850/F1KM group. Manually modify the code in red.

```
void R_Config_DCRA0_Input16bitData(const uint16_t * data, uint32_t data_num)
{
    uint32_t i;
    uint16_t * data_address = (uint16_t *)data;

    for(i=0; i<data_num; i++)
    {
        DCRA0.CIN = *data_address;
        data_address++;
    }
}
```

```
void R_Config_DCRA0_Input8bitData(const uint8_t * data, uint32_t data_num)
{
    uint32_t i;
    uint8_t * data_address = (uint8_t *)data;

    for(i=0; i<data_num; i++)
    {
        DCRA0.CIN = *data_address;
        data_address++;
    }
}
```

3.5 Schedule for Fixing the Problem

This problem will be fixed in the next version. (Scheduled to be released in May 2021.)

4. When using One-Pulse Output and One-Shot Pulse Output

4.1 Applicable Products

Smart Configurator for RH850 V1.1.0 or later version

4.2 Applicable Devices

RH850 family: RH850/F1KM group and RH850/U2A group

- RH850/F1KM-S1 (48-pin, 64-pin, 80-pin, and 100-pin products)
- RH850/F1KM-S4 (100-pin, 144-pin, 176-pin, and 233-pin products)
- RH850/U2A16 (292-pin and 516-pin products)
- RH850/U2A8 (292-pin product)

4.3 Details

When using One-Pulse Output and One-Shot Pulse Output on the following peripherals, the actual output pulse width has one count clock cycle error due to wrong value is set to timer data register.

- RH850/F1KM-S1: 48-pin, 64-pin products

  TAUD0
- RH850/F1KM-S1: 80-pin, 100-pin products

  TAUB0, TAUD0
- RH850/F1KM-S4: 100-pin, 144-pin products

  TAUB0, TAUD0
- RH850/F1KM-S4: 176-pin, 233-pin products

  TAUB0, TAUB1, TAUD0
- RH850/U2A16 (292-pin and 516-pin products)

  TAUD0, TAUD1, TAUD2
- RH850/U2A8 (292-pin product)

TAUD0, TAUD1, TAUD2

4.4 Workaround

User can manually modify the macro value in the following source file

- Source file: “<Configuration-name>.h”.
- Macro:
  1) #define _TAUBnm_COMPARE_VALUE
  2) #define _TAUDnm_COMPARE_VALUE

Note: If code is generated again, the previous state is restored. Modification is necessary each time you perform code generation.

The following steps show an example of the required modification when using One-Shot Pulse Output function. In this example, <*Configuration-name*> is Config_TAUB0 in the RH850/F1KM group.

[Modification example]

Step1: User can config a One-Shot Pulse Output function, including “One-shot pulse width setting” of slave channel (refer to Figure 4-1 Setting of One-shot pulse width).

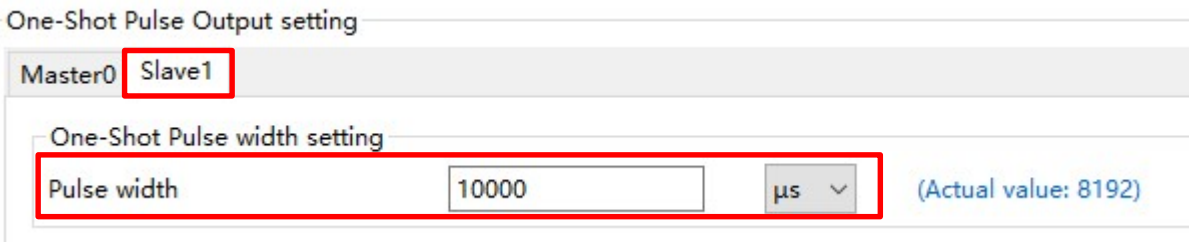

Figure 4-1 Setting of One-shot pulse width

Step2: Click “Generate Code” and check the following macro value in “Config_TAUB0.h” file, the value in red need to be confirmed.

```
/***********************************************************************
Macro definitions
***********************************************************************/
#define _TAUB0_CHANNEL0_COMPARE_VALUE               (0x270FU)
#define _TAUB0_CHANNEL1_COMPARE_VALUE               (0x270FU)
```

Step3: If user find the actual One-shot pulse width output in his own system is not as expected 10000 us, user can increase this macro value by “1”, as the following value in blue.

```
/***********************************************************************
Macro definitions
***********************************************************************/
#define _TAUB0_CHANNEL0_COMPARE_VALUE               (0x270FU)
#define _TAUB0_CHANNEL1_COMPARE_VALUE               (0x2710U)
```

4.5 Schedule for Fixing the Problem

This problem will be fixed in the next version. (Scheduled to be released in May 2021.)

5. When using PWM Output and Triangle PWM Output

5.1 Applicable Products

Smart Configurator for RH850 V1.3.0 or previous version

5.2 Applicable Devices

RH850 family: RH850/F1KM group

- RH850/F1KM-S1 (48-pin, 64-pin, 80-pin, and 100-pin products)
- RH850/F1KM-S4 (100-pin, 144-pin, 176-pin, and 233-pin products)

5.3 Details

When using PWM Output and Triangle PWM Output on the following peripherals, the slave channel interrupt priority is always same as master channel even though user has set different priority level on GUI (refer to Figure 5-1 Setting of master and slave interrupt priority).

- RH850/F1KM-S1: 48-pin, 64-pin, 80-pin, and 100-pin products

  TAUD0
- RH850/F1KM-S4: 100-pin, 144-pin, 176-pin, and 233-pin products

  TAUD0

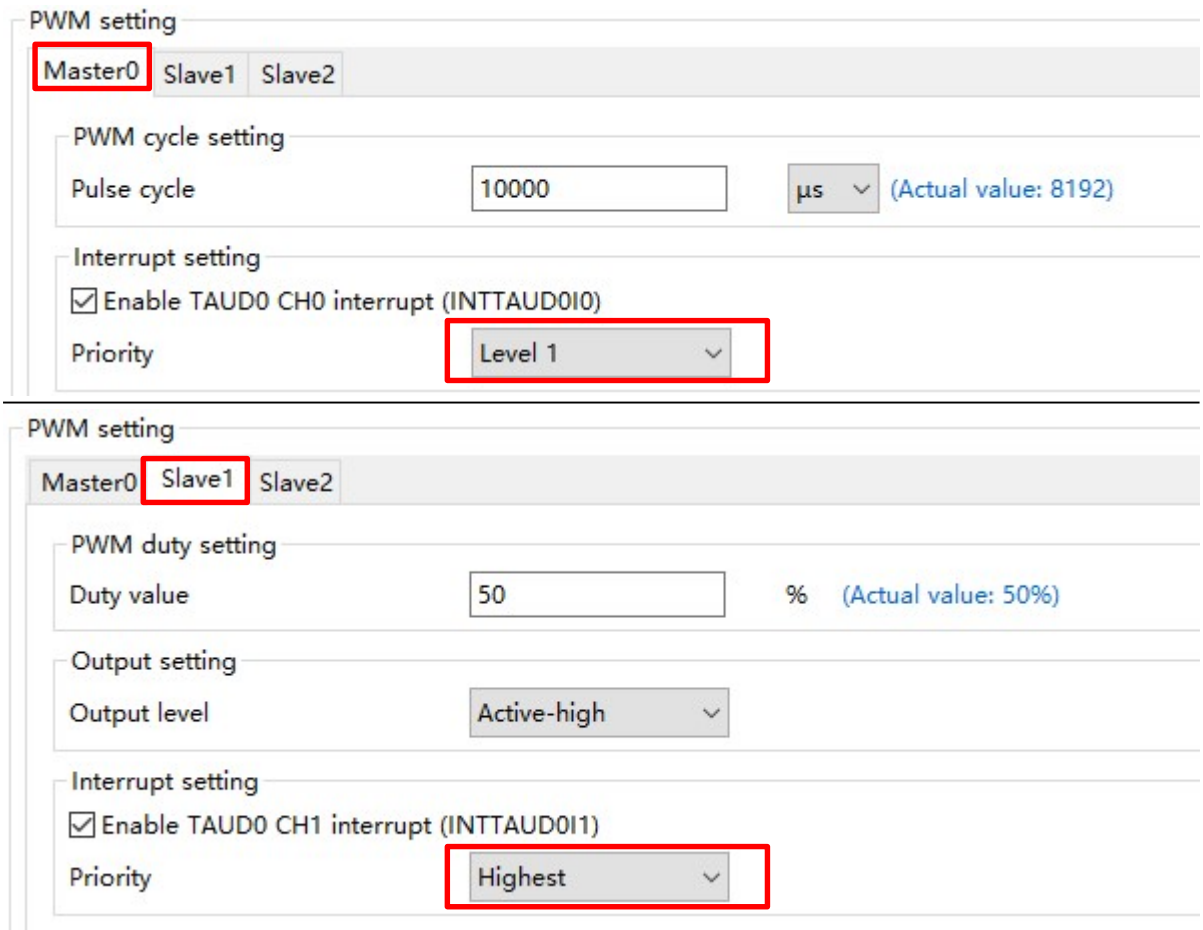

Figure 5-1 Setting of master and slave interrupt priority

5.4 Workaround

User can manually modify the register setting code in the following source file: change the slave channel interrupt priority macro to the priority which is set on GUI. The interrupt priority macro name can be found in "¥smc_gen¥general¥r_cg_macrodriver.h" file.

- Source file: “<Configuration-name>.c”.
- Function: “void R_<*Configuration-name*>_ Create (void)”

Note: If code is generated again, the previous state is restored. Modification is necessary each time you perform code generation.

The following is an example of the required modification when <*Configuration-name*> is Config_TAUD0 in the RH850/F1KM group. Manually modify the code in red.

```
 void R_Config_TAUD0_Create(void)
 {
    /* Disable channel counter operation */
    TAUD0.TT |= (_TAUD_CHANNEL2_COUNTER_STOP | _TAUD_CHANNEL1_COUNTER_STOP |
_TAUD_CHANNEL0_COUNTER_STOP);
    ……
    /* Set INTTAUD0I0 setting */
    INTC1.ICTAUD0I0.BIT.TBTAUD0I0 = _INT_TABLE_VECTOR;
    INTC1.ICTAUD0I0.UINT16 &= _INT_PRIORITY_LEVEL1;
    /* Set INTTAUD0I1 setting */
    INTC2.ICTAUD0I1.BIT.TBTAUD0I1 = _INT_TABLE_VECTOR;
    INTC2.ICTAUD0I1.UINT16 &= _INT_PRIORITY_HIGHEST;
    ……
 }
```

5.5 Schedule for Fixing the Problem

This problem will be fixed in the next version. (Scheduled to be released in May 2021.)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Apr.01.21	-	First edition issued

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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