[Notes]

CS+ Code Generator for RL78 (CS+ for CC / CA,CX)

R20TS0926EJ0100 Rev.1.00 Mar. 01, 2023

e² studio Code Generator Plug-in

Applilet3 Coding Assistance Tool for RL78

Outline

When using any of the products in the title, note the following point.

- 1. Notes on using the data flash library by using the data flash API generated by a code generator
- 1. Notes on Using the Data Flash Library by Using the Data Flash API Generated by a Code Generator

1.1 Applicable Products

- CS+ Code Generator for RL78 (CS+ for CC) V2.22.00 and earlier
- > CS+ Code Generator for RL78 (CS+ for CA, CX) V2.22.00 and earlier
- > e² studio Code Generator Plug-in (e² studio V2.19.0) and earlier
- > Applilet3 for RL78 V1.21.00 and earlier

1.2 Applicable Devices

➢ RL78 Family:

RL78/F12, RL78/F13, RL78/F14, RL78/F15, RL78/G13 RL78/G13A, RL78/G14

1.3 Details

The data flash library might not operate properly if [Setting of data flash library] is set to [Used], [Main system clock (fMAIN) setting] in [Clock setting] is [High-speed system clock (fMX)], and [High-speed OCO clock setting] and [CPU and peripheral clock setting] are set to different frequencies.

If the frequency of [High-speed OCO clock setting] is lower than that of [CPU and peripheral clock setting], the data flash library might not program properly.

If the frequency of [High-speed OCO clock setting] is higher than that of [CPU and peripheral clock setting], the data flash library programs properly but its waiting time becomes longer.



1.4 Conditions

If [Setting of data flash library] is set to [Used] and [High-speed OCO clock setting] and [CPU and peripheral clock setting] are set to different frequencies (both are set in [Clock setting]), the problems described in 1.3 occur.

Invalid setting examples (RL78/F14 group 48-pin products)

- · Main system clock (fMAIN) setting: High-speed system clock (fMX)
- · High-speed OCO clock setting: 32 MHz
- · High-speed system clock setting: 20 MHz

Main system clock (fMAIN) setting — O High-speed OCO (fIH)		High-speed system clock (fMX)	
High-speed OCO clock setting			
Operation	Frequency	32 ~	(MHz)
High-speed system clock setting			
Operation			
X1 oscillation (FX)		O External clock input (FEX)	
Frequency		20	(MHz)
Stable time		13107.2 (2^18/fX) ~	(µs)

Figure 1: High-speed OCO clock setting

• CPU and peripheral clock setting: 20 MHz

- CPU and peripheral clock setting			
CPU and peripheral clock (fCLK)	20000 (fMP)	~	(kHz)

Figure 2: CPU and peripheral clock setting

1.5 Workarounds

Workaround 1: Set [High-speed OCO clock setting] and [CPU and peripheral clock setting] to a frequency at the same phase, and then generate code. (This minimizes the waiting time for the data flash library.)

Workaround 2: If [High-speed OCO clock setting] and [CPU and peripheral clock setting] cannot be set to a frequency at the same phase, set close frequencies to them (note that the frequency of [High-speed OCO clock setting] should be higher), and then generate code. (The data flash library operates properly although its waiting time is long.)

High-speed OCO clock setting: Frequency examples (RL78/F14 group 48-pin products)

CPU and peripheral clock setting	High-speed OCO clock setting
Lower than 4 MHz	See Workaround 3.
4 MHz	4 MHz
4 MHz < fMAIN <= 8 MHz	8 MHz
8 MHz < fMAIN <= 12 MHz	12 MHz
12 MHz < fMAIN <= 16 MHz	16 MHz
16 MHz < fMAIN <= 20 MHz	24 MHz

Table 1: Frequency setting examples

Note: The data flash library does not operate properly if the CPU clock is set to lower than 1 MHz.



Workaround 3: If you select Workaround 2 (unable to set a frequency at the same phase), you can minimize the waiting time for the data flash library by modifying the generated code.

As the following example shows, enter the frequency set to [CPU and peripheral clock setting].

_xx_HOCO_CLOCK_MHz (r_cg_pfdl.h and r_cg_pfdl.c): Change xx (macro value).

Example: [High-speed system clock (fMX)] is set to 20 MHz

r	ca	pfdl.	h file
·_	_~9_	_pron.	

#define _32_HOCO_CLOCK_MHz	(32) /* HOCO clock value in MHz */
Change as follows:	
#define <u>20</u> HOCO_CLOCK_MHz	(20) /* HOCO clock value in MHz */

r_cg_pfdl.c file

gFdlDesc.fx_MHz_u08 = _32_HOCO_CLOCK_MHz; /* Set an integer of the range from 1 to 32 according to GUI setting of HOCO. */

Change as follows:

gFdlDesc.fx_MHz_u08 = <u>20_HOCO_CLOCK_MHz</u>; /* Set an integer of the range from 1 to 32 according to GUI setting of HOCO. */

For values to be entered, see the specifications of the data flash library.

1.6 Schedule for Fixing the Problem

Smart Configurator is released as a code generator. Note that while Smart Configurator will continue to be updated, code generators will no longer be updated.

Problems in code generators will not be fixed. If you continue to use the code generator, apply either of the workarounds.



Revision History

		Description	
Rev.	Date	Page	Summary
1.00	Mar.01.23	-	First edition issued

Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.

The past news contents have been based on information at the time of publication. Now changed or invalid information may be included.

The URLs in the Tool News also may be subject to change or become invalid without prior notice.

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit: www.renesas.com/contact/

© 2023 Renesas Electronics Corporation. All rights reserved. TS Colophon 4.3

