Date: Nov. 21, 2016

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RL*-A069A/E	Rev.	1.00
Title	Restriction regarding Watchdog timer		Information Category	Technical Notification		
Applicable Product	RL78/G11, RL78/G12, RL78/G13, RL78/G14, RL78/G1A, RL78/G1C, RL78/G1D, RL78/G1E, RL78/G1F, RL78/G1G, RL78/G1H, RL78/L12, RL78/L13, RL78/L1A, RL78/L1C, RL78/I1A, RL78/I1B, RL78/I1C, RL78/I1D, RL78/I1E	Lot No. -	Reference Document	Latest user's Manual of applicable products		

The restriction below applies to watchdog timer in the above mentioned Applicable Products.

1. Description

Wrong WDT-RESET may assert when WDT counter is cleared (writing ACh to WDTE register) at just 50% of count-overflow-value and when window open period of watchdog timer is set to 75%.

When all of following conditions is established, the restriction applies.

(1) “Operation of watchdog timer” is “enabled” (WDTON = “1”)

(2) “Operation of watchdog timer in the HALT or STOP mode” is “enabled” (WDSTBYON = “1”)

(3) “Setting of window open period of watchdog timer” is “75%” (WINDOW1, WINDOW0 = “10b”)

(4) During watchdog timer operates, counter is cleared at just 50% of count-overflow-value (writing WDTE register to ACh).

Note: Each bit such as WDTON, WDSTBYON, WINDOW1 and WINDOW0 is a part of user option byte (000C0h)

Table 1. Watchdog timer overflow time and Counter is 50% period

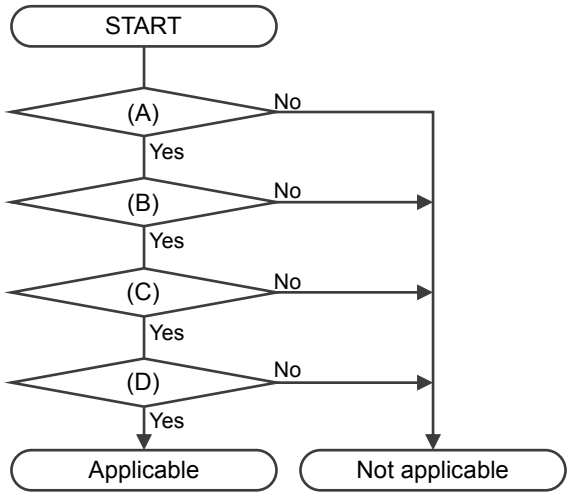
Bit of 000C0H			Watchdog timer overflow time	Counter is 50% period
WDCS2	WDCS1	WDCS0		
0	0	0	$2^6/f_{WDT}$	1.85ms to 2.51ms
0	0	1	$2^7/f_{WDT}$	3.71ms to 5.02ms
0	1	0	$2^8/f_{WDT}$	7.42ms to 10.04ms
0	1	1	$2^9/f_{WDT}$	14.84ms to 20.08ms
1	0	0	$2^{11}/f_{WDT}$	59.36ms to 80.32ms
1	0	1	$2^{13}/f_{WDT}$	237.44ms to 321.26ms
1	1	0	$2^{14}/f_{WDT}$	474.89ms to 642.51ms
1	1	1	$2^{16}/f_{WDT}$	1899.59ms to 2570.04ms

Remark. $f_{WDT} = f_{IL}$ (Lows-peed on-chip oscillator clock frequency) 15kHz ±15%

[Flowchart for judging applicable of this restriction]

Figure 1 shows flowchart for judging applicable of this restriction that affect your own usage of the watch-dog timer.

Figure 1. Flowchart for judging applicable if your software is affected



(A)	Is “operation of watchdog timer” “enabled” ? [WDTON =1?] If that is not, it is not applicable.
(B)	Is “operation of watchdog timer in the HALT/STOP/SNOOZE mode” “enabled” ? [WDSTBYON = 1?] If that is not, it is not applicable because window open period is set as 100%.
(C)	Is “setting of window open period of watchdog timer” “75%” ? [WINDOW [1:0] = 10B?] If that is 50%/100%, it is not applicable even if counter is cleared at just 50%.
(D)	Is counter cleared at just 50% of count-overflow-value? [Is WDTE written to ACh at this timing?] If that is not, it is not applicable

2. Countermeasure

Please correspond with either of the following countermeasures.

1) Set “window open period” to “50%” or “100%”.

Set bit 6 and bit 5 in user option byte (000C0h) to 01b (50%) or 11b (100%)

2) If “window open period” is set to “75%” (WINDOW1, WINDOW0 = “10b”), please perform Counter- clear within the period except for just 50%.

Note

If boot swap function is used, set 010C0h to same value as user option byte (000C0h).

3. Parts number of applicable product

Table 2 shows product group and parts number of applicable product.

Table 2. Product group and parts number of applicable product

Product group	Parts number
RL78/G11	R5F105xxx
RL78/G12	R5F102xxx, R5F103xxx
RL78/G13	R5F100xxx, R5F101xxx
RL78/G14	R5F104xxx
RL78/G1A	R5F10Exxx
RL78/G1C	R5F10Jxxx, R5F10Kxxx
RL78/G1D	R5F11Axxx
RL78/G1E	R5F112xxx
RL78/G1F	R5F11Bxxx
RL78/G1G	R5F11Exxx
RL78/G1H	R5F11Fxxx
RL78/L12	R5F10Rxxx
RL78/L13	R5F10Wxxx
RL78/L1A	R5F11Mxxx
RL78/L1C	R5F110xxx, R5F111xxx
RL78/I1A	R5F107xxx
RL78/I1B	R5F10Mxxx
RL78/I1C	R5F10Nxxx
RL78/I1D	R5F117xxx
RL78/I1E	R5F11Cxxx