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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-R8C-A052A/E	Rev.	1.00
Title	Precaution of using DTC(Data Transfer Controller)		Information Category	Technical Notification		
Applicable Product	Described below	Lot No. -	Reference Document			

Precaution described below is added to the following products in the User's Manual.

1. Applied Product

R8C/32A Group, R8C/33A Group, R8C/35A Group, R8C/36A Group, R8C/38A Group,
R8C/3GA Group, R8C/3JA Group,
R8C/32C Group, R8C/33C Group, R8C/34C Group, R8C/35C Group, R8C/36C Group,
R8C/38C Group, R8C/3GC Group, R8C/3JC Group,
R8C/32M Group, R8C/33M Group, R8C/34M Group, R8C/35M Group, R8C/36M Group,
R8C/38M Group, R8C/3GM Group, R8C/3JM Group,
R8C/33T Group, R8C/3JT Group, R8C/36T-A Group, R8C/38T-A Group,
R8C/34U Group, R8C/34K Group, R8C/3MU Group, R8C/3MK Group, R8C/3MQ Group,
R8C/L35A Group, R8C/L36A Group, R8C/L38A Group, R8C/L3AA Group,
R8C/L35B Group, R8C/L36B Group, R8C/L38B Group, R8C/L3AB Group,
R8C/L35C Group, R8C/L36C Group, R8C/L38C Group, R8C/L3AC Group,
R8C/L35M Group, R8C/L36M Group, R8C/L38M Group, R8C/L3AM Group

2. Precaution regarding the use of DTC

2-1. Do not execute DTC transfer to interrupt control registers, while CPU is executing Read-Modify-Write instruction.

2-2. Change DTCENi0~DTCENi7 bits when the interrupt to these bits will not occur.

2-3. Do not execute DTC transfer to the address that CPU rewrites data by Read-Modify-Write instruction.

Item No.	Target address of Read-Modify-Write instruction	Target address of DTC transfer
2-1	All address	Interrupt Control registers
2-2	DTC Activation Enable Register	Same DTC Activation Enable Register
2-3	Specified address	Same specified address

3. Detail explanation

3-1. Do not execute DTC transfer to interrupt control registers, while CPU is executing Read-Modify-Write instruction.

As shown figure 1. , the write operation to interrupt control register by DTC transfer is invalid, in case DTC transfer timing conflicts with timing of Read-Modify-Write execution to every address by CPU.

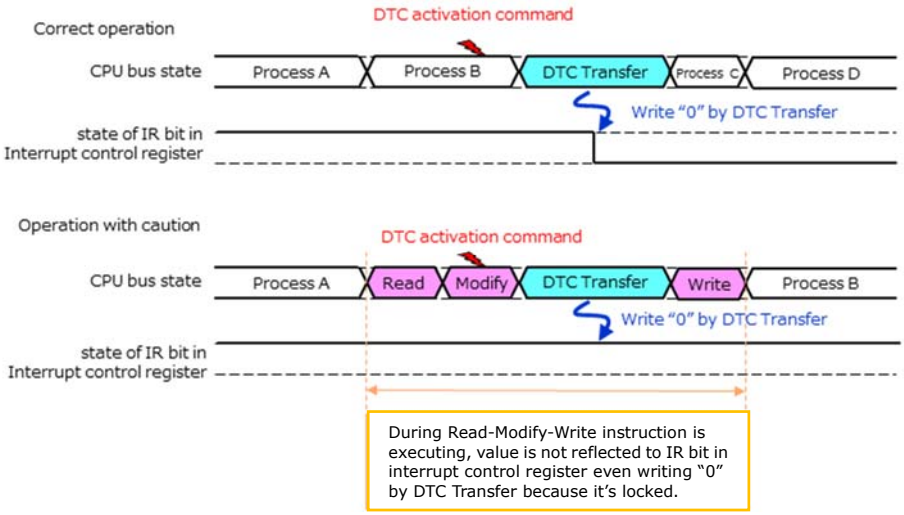

Figure 1. condition of CPU bus and interrupt control register

3-2. In case changing any of DTCENi0~DTCENi7 bit by Read-Modify–Write instruction, please change them when interrupt to these bits will not occur.

As shown figure 2. , target bit to change to "0" will not occur, in case change timing from "1" to "0" of target bit in DTC Activation Enable Register(DTCENi) conflicts with timing of changing different bit in same register by Read-Modify-Write instruction by CPU.

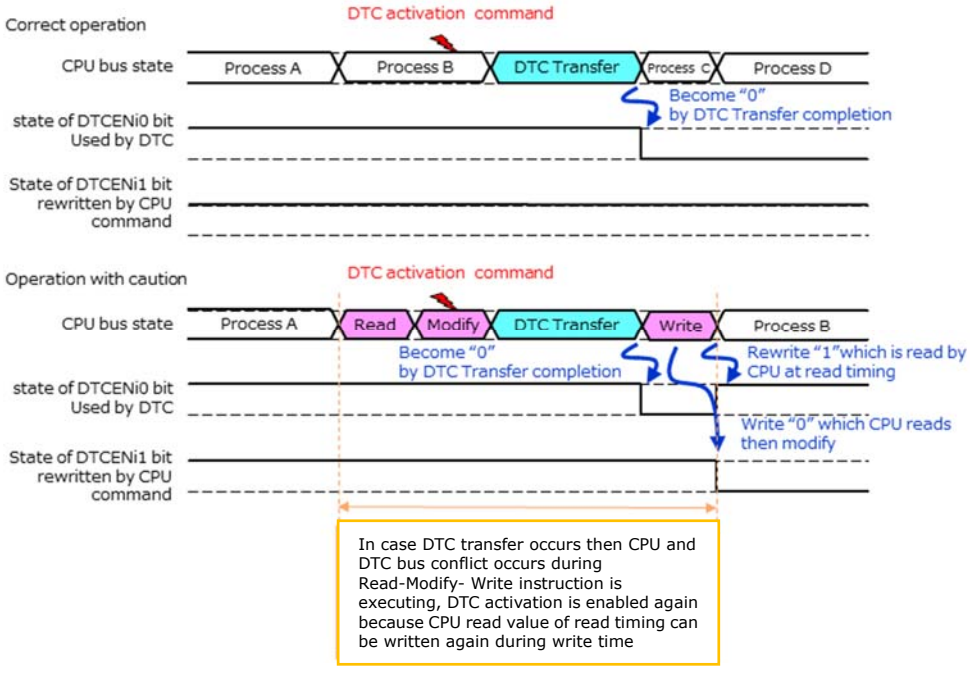

Figure 2. condition of CPU bus and DTC Activation Enable Register

3-3. Do not execute DTC transfer to the address that CPU rewrites data by Read—Modify-Write instruction.

As shown figure 3. , write operation by DTC transfer may be invalid, in case rewrite to specific address by Read-Modify-Write instruction by CPU conflicts with write operation by DTC transfer.

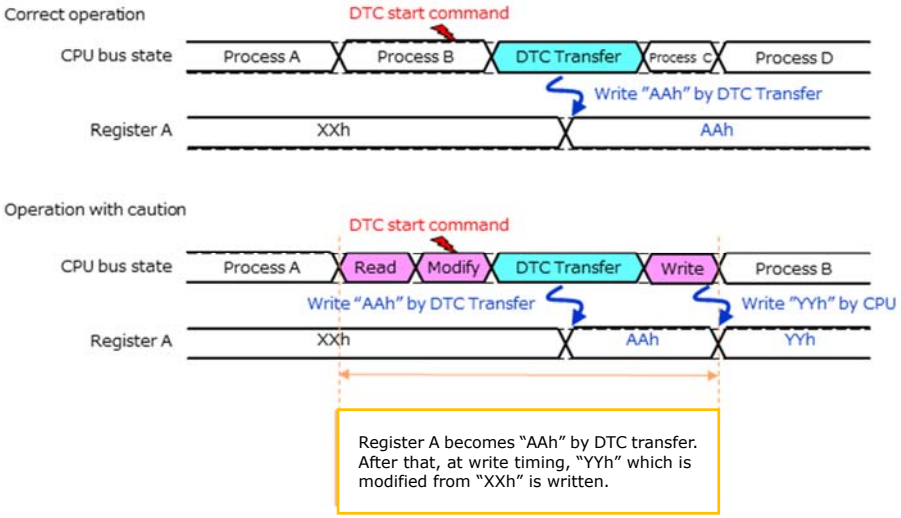

Figure 3. Condition of CPU bus and specific register

4. Regarding Read-Modify-Write instruction

R8C CPU designed to arbitrate bus not based on instruction but the bus access base. Bus access of Read-Modify-Write instruction is executed as the following sequence and if DTC access trigger occurs during Read-Modify-Write instruction, the bus control right is transferred from CPU to DTC after (1),(2).

The sequence of Read-Modify-Write instruction is shown below. The detail is refer to figure 4.

1. Read the data at the specified address
2. Modify specified bit of the read data
3. Write the data to the original address

Data read and write are executed with byte or word access. In case BIT processing or logical calculation, the read data in unspecified bit with byte or word access will be written to original address without any modification.

List of Read-Modify-Write instruction is shown in table 1.

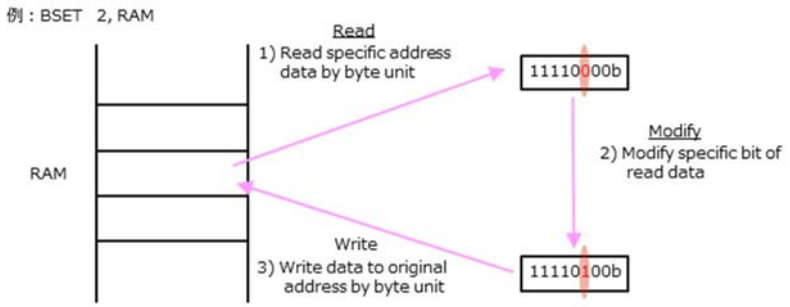

Figure 4. operation of Read-Modify-Write instruction

Table 1. List of Read-Modify-Write instruction

Function	Mnemonic
Transfer	MOVDir
Bit operation	BCLR, BMCnd, BNOT, BSET, BTSTC, BTSTS
Shift	ROLC, RORC, ROT, SHA, SHL
Calculation	ABS, ADC, ADCF, ADD, DADC, DADD, DEC, DIV, DIVU, DIVX, DSBB, DSUB, EXTS, INC, MUL, MULU, NEG, SBB, SUB
Logical calculation	AND,NOT,OR,XOR
Jump	ADJNZ,SBJNZ