To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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GRADE A

RENESAS TECHNICAL NEWS

No.M16C-94-0306

M16C/62 Group, M16C/6H Group, M16C/30L Group
Cautions for Selecting Both Edges of $\overline{\text{INT0}}$ pin as DMA Request Factor for DMA0

Classification	Products Effected
Corrections and supplementary explanation of documents ✓Notes Knowhow Others	M16C/62 Group M16C/6H Group M16C/30L Group

1. Cautions

This is a caution about using DMA0 on products listed on Table 2. This caution does not apply to DMA1. The following is necessary to trigger DMA requests on both edges of $\overline{\text{INT0}}$:

a. Set the DSEL3 to DSEL0 bits in DM0SL register to ”0110_2”.

b. Set the DMS bit in DM0SL to ”1”.

c. Set the IFSR0 bit in IFSR register to ”1” (both edges).

Please note that in this case $\overline{\text{INT0}}$ interrupts will occur at both edges because the IFSR0 bit is set to “1” (both edges).

2. Description of Behavior

When the DSEL3 to DSEL0 bits in the DM0SL register are set to ”0110_2” and the DMS bit to ”1” (to trigger DMA requests on both edges of $\overline{\text{INT0}}$ pin), if the IFSR0 bit in the IFSR register is set to “0” (one edge), DMA transfers will only occur on the falling edge. To initiate DMA transfers on both edges, the IFSR0 bit must be set to “1”. Table 1 summarizes the DMA0 transfer trigger operation based on the DSEL3 to DSEL0 bits and DMS bit in DM0SL register, IFSR0 bit in IFSR register, and POL bit in INT0IC register. As mentioned earlier, this caution does not apply to DMA1. When both edges of $\overline{\text{INT1}}$ pin are selected for the DMA1, DMA transfer is performed at both edges regardless how the IFSR1 bit in IFSR register is set.

Table 1. DSEL3 to DSEL0 Bits in DM0SL Register and DMA0 Transfer Trigger

DM0SL		IFSR	INT0IC	DMA0 Transfer Trigger
DSEL3 - DSEL0	DMS	IFSR0	POL	
0000_2	0	0	0	Falling edge of $\overline{\text{INT0}}$ pin
0000_2	0	0	1	Falling edge of $\overline{\text{INT0}}$ pin
0000_2	0	1	0	Falling edge of $\overline{\text{INT0}}$ pin
0110_2	***1***	***0***	***0***	***Falling edge of $\overline{\text{INT0}}$ pin***
0110_2	***1***	***0***	***1***	***Falling edge of $\overline{\text{INT0}}$ pin***
0110_2	1	1	0	Both edges of $\overline{\text{INT0}}$ pin

3. Products Affected

Table 2 lists products affected.

Table 2. Products Affected

	Products Affected
M16C/62A Group	M30620FCAFP/GP, M30621FCAGP
M16C/62M Group	M30620FCMFP/GP, M30621FCMGP
M16C/62N Group	All products (M3062GF8NFP/GP included)
M16C/6H Group	M306H2FCFP
M16C/30L Group	All products