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RENESAS TECHNICAL UPDATE

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Title	Correction items for RL78/F13, F14 User's Manual: Hardware		Information Category	Technical Notification		
Applicable Product	RL78/F13, RL78/F14	Lot No. –	Reference Document	User's Manuals: Hardware of Applicable Products		

This document describes misstatements found in the RL78/F13, F14 User's Manual: Hardware Rev. 2.00 (R01UH0368EJ0200).

Table 1 Corrections in the User's Manual (1)

No	Pages		Corrections and Applicable Items	References
	Rev.2.10	Rev.2.00		
1	P10 to 31	P10 to 12	1.4 Block Diagram for each product	-
2	P147	P128	Reset value of P13 register in Table 3-5 SFR List (1/4)	p.4
3	P256	P237	Explanations of the 4.2.7 Port 7	p.4
4	P271	P252	Table 4-14. Setting Functions of P80/ANI2/ANO0 Pin	p.4
5	P321	P302	Reset value of P13 register in Figure 4-75. Format of Port Register (100-pin products)	p.4
6	P325	P306	Notes and Cautions in Figure 4-79. Format of Port Mode Control Register (100-pin products)	p.5
7	P389	P370	Cautions of Figure 5-18. Format of LIN Clock Select Register (LINCKSEL)	p.5
8	P423	P404	Explanations of 5.7.2 High-Speed On-Chip Oscillator	p.5
9	P438	P419	Explanations of 6.2.2 Timer data register mn (TDRmn)	p.5
10	P569	P550	Access Size in Table 8-2. Timer RD Register Configuration	p.5
11	P602	P583	Explanations of [Complementary PWM Mode] in 8.2.19 Timer RD General Registers Ai, Bi, Ci, and Di (TRDGRAi, TRDGRBi,TRDGRCi, TRDGRDi) (i = 0 or 1)	p.5
12	P621	P602	Figure 8-44. Pulse Output Forced Cutoff	p.6
13	P666	P647	Notes of Figure 9-8. Format of Real-time Clock Control Register 1 (RTCC1) (2/2)	p.7
14	P697	P678	Notes of Table 11-3. Setting of Overflow Time of Watchdog Timer	p.7
15	P703	P684	Cautions of (1) ANI0 to ANI23 (V_{DD}) and ANI24 to ANI30 (EV_{DD}) pins in 12.2 Configuration of A/D Converter	p.7
16	P730	P711	Notes and Cautions of Figure 12-18. Formats of Port Mode Control Registers 7, 9, and 12 (PMC7, PMC9, PMC12)	p.8
17	P772	P753	Table 13-1. Setting Functions of ANO0/ANI2/P80 Pin	p.8
18	P792, P833, P895, P959, P992	P773, P814, P876, P940, P973	CHAPTER 15 SERIAL ARRAY UNIT Note of Tables "Group A, B, C-1, C-2, D-1, D-2 and E"	p.9
19	P807	P788	Note of Figure 15-7. Format of Serial Communication Operation Setting Register mn (SCRmn)	p.10
20	P821	P802	Note of Figure 15-17. Format of Serial Slave Select Enable Register m (SSEm)	p.10

Table 2 Corrections in the User's Manual (2)

No	Pages		Corrections and Applicable Items	References
	Rev.2.10	Rev.2.00		
21	P1112, P1140, P1165	P1093, P1121, P1146	17.2.1 LIN Registers for Master Mode 17.2.2 LIN Registers for Slave Mode 17.2.3 Registers for UART Cautions of (4) LIN Clock Select Register (LINCKSEL)	p.11
22	P1123, P1124, P1150	P1104, P1105, P1131	Explanations of bit error and framing error in 17.2.1 LIN Registers for Master Mode and in 17.2.2 LIN Registers for Slave Mode	p.11
23	P1153	P1134	Explanations of FTS bits in (16) LIN/UART Transmission Control Register (LTRCn) of 17.2.2 LIN Registers for Slave Mode	p.11
24	P1160	P1141	Explanations of RFDL bits in (20) LIN/UART Data Field Configuration Register (LDFCn) of 17.2.2 LIN Registers for Slave Mode	p.11
25	P1176	P1157	Explanations of IBS bits in (11) LIN/UART Space Configuration Register (LSCn) of 17.2.3 Registers for UART	p.11
26	P1181	P1162	Explanations of FTC flag in (16) LIN/UART Status Register (LSTn) of 17.2.3 Registers for UART	p.12
27	P1189	P1170	Explanations of UROE bit in (22) UART Operation Enable Register (LUOERn) 17.2.3 Registers for UART	p.12
28	P1216, P1217	P1197, P1198	Notes of Table 17-14. Types of Statuses in LIN Master Mode and Table 17-15. Types of Statuses in LIN Slave Mode	p.12
29	P1218	P1199	Notes of Table 17-16. Types of Error Statuses in LIN Master Mode	p.12
30	P1218, P1221	P1199, P1202	Notes of Table 17-16. Types of Error Statuses in LIN Master Mode and Table 17-17. Types of Error Statuses in LIN Slave Mode	p.12
31	P1231	P1212	Cautions of Figure 17-30. Expansion Bit Reception Example (with Data Comparison) (LSB First, UEBDL = 0)	p.12
32	P1246, P1247, P1248, P1249	P1226, P1227, P1228, P1229	Explanations of 17.6.2 Transmission in LIN Master Self-Test Mode, 17.6.3 Reception in LIN Master Self-Test Mode, 17.6.4 Transmission in LIN Slave Self-Test Mode and 17.6.5 Reception in LIN Slave Self-Test Mode	p.13
33	P1251, P1253	P1231, P1233	Explanations of Figure 17-41. Block Diagram of Baud Rate Generation in LIN Master Mode and Figure 17-42. Block Diagram of Baud Rate Generation in LIN Slave Mode	p.13
34	P1255	P1235	Explanations of Figure 17-43. Block Diagram of Baud Rate Generation in UART Mode	p.13
35	P1295, P1327, P1342, P1372	P1275, P1307, P1322, P1352	Notes of 18.3.7 CANi Error Flag Register L (CiERFLL) (i = 0), 18.3.35 CAN Receive FIFO Status Register m (RFSTSm) (m = 0, 1), 18.3.47 CANi Transmit/Receive FIFO Status Register k (CFSTSk) (i = 0) (k = 0) and 18.3.75 CANi Transmit History Buffer Status Register (THLSTSi) (i = 0)	p.14
36	P1305	P1285	Notes of 18.3.14 CAN Global Error Flag Register (GERFLL)	p.14
37	P1340	P1320	Explanations of CFITR bit in 18.3.46 CANi Transmit/Receive FIFO Control Register kH (CFCCHk) (i = 0) (k = 0)	p.14
38	P1461	P1441	Explanations of 19.4.3 DTC Pending Instruction	p.14
39	P1478	P1458	Table 21-1. Interrupt Source List (3/4)	p.14
40	P1512	P1492	Cautions of 21.4.4 Interrupt servicing during division instruction	p.14
41	P1514	P1493	Explanations of 21.4.5 Interrupt request hold	p.15
42	P1591	P1570	Cautions of Figure 27-9. Format of 1-bit Error Detection Interrupt Enable Register (ECCIER)	p.15
43	P1596	P1575	Cautions of 27.3.4 CPU stack pointer monitor function	p.15
44	P1601	P1580	Notes of Figure 27-20. Format of Invalid Memory Access Detection Control Register (IAWCTL)	p.15
45	P1672	P1651	Cautions of Table 33-5. Operation List (12/18)	p.16
46	P1686, P1737, P1788	P1665, P1716, P1767	Notes of 34.3.1 Pin Characteristics (1/4), 35.3.1 Pin Characteristics (1/4) and 36.3.1 Pin Characteristics (1/4)	p.16
47	P1687, P1738, P1789	P1666, P1717, P1768	Notes of 34.3.1 Pin Characteristics (2/4), 35.3.1 Pin Characteristics (2/4) and 36.3.1 Pin Characteristics (2/4)	p.16

Table 3 Corrections in the User's Manual (3)

No	Pages		Corrections and Applicable Items	References
	Rev.2.10	Rev.2.00		
48	P1697, P1748, P1799	P1676, P1727, P1778	Notes of 34.4.1 Basic Operation (1/2), 35.4.1 Basic Operation (1/2) and 36.4.1 Basic Operation (1/2)	p.16
49	P1708, P1759, P1810	P1687, P1738, P1789	(7) During communication at same potential (simplified I 2 C mode) in 34.5.1 Serial Array Unit, 35.5.1 Serial Array Unit and 36.5.1 Serial Array Unit	p.17
50	P1729, P1780, P1831	P1708, P1759, P1810	34.9 Flash Memory Programming Characteristics 35.9 Flash Memory Programming Characteristics 36.9 Flash Memory Programming Characteristics	p.17
51	P1783	P1762	Corrections of 36.1 Absolute Maximum Ratings (2/2)	p.17

No.2 Table 3-5. SFR List (1/4)

Table 3-5. SFR List (1/4)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset
				1-bit	8-bit	16-bit	
FFF0DH	Port register 13	P13	R/W	√	√	–	Undefined note

Note P130 bit depends on the setting of User Option Byte (000C2H/020C2H).

No.3 4.2.7 Port 7

4.2.7 Port 7

To use P70/ANI26 to P74/ANI30 as digital input pins, set them in the digital I/O mode by using the port mode control register 7 (PMC7) and in the input mode by using the PM7 register. Use these pins starting from the upper bit.

To use P70/ANI26 to P74/ANI30 as digital output pins, set them in the digital I/O mode by using the port mode control register 7 (PMC7) and in the output mode by using the PM7 register.

To use P70/ANI26 to P74/ANI30 as analog input pins, set them in the analog input mode by using the port mode control register 7 (PMC7) and in the input mode by using the PM7 register.

No.4 Table 4-14. Setting Functions of P80/ANI2/ANO0 Pin

Table 4-14. Setting Functions of P80/ANI2/ANO0 Pin

ADPC Register	PM8 Register	DAM Register	DAM2 Register	ADS Register	Functions of ANO0/ANI2/P80 Pin
Digital I/O	Input mode	—	Enables analog output	—	Setting prohibited
			Disables analog output		Digital input
	Output mode	—	Enables analog output	—	Setting prohibited
			Disables analog output		Digital input
Analog I/O	Input mode	Enables D/A conversion operation	Enables analog output	Selects ANI	Setting prohibited
				Does not selects ANI	Analog output (D/A conversion output)
			Disables analog output	Selects ANI	Analog input (to be converted)
				Does not selects ANI	Analog input (not to be converted) Note
		Stops D/A conversion operation	Enables analog output	Selects ANI	Setting prohibited
				Does not selects ANI	Setting prohibited
			Disables analog output	Selects ANI	Analog input (to be converted)
				Does not selects ANI	Analog input (not to be converted)
	Output mode	—	—	—	Setting prohibited

Note This is a setting that the D/A converter is used for internal reference voltage of comparator. In this case, set CVRS1, CVRS0 bits of CMPSEL register to 10b (internal reference voltage (DAC output) is selected).

No.5 Figure 4-75. Format of Port Register (100-pin products)

Figure 4-75. Format of Port Register (100-pin products)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
P13	P137	0	0	0	0	0	0	P130	FFF0DH	Undefined Note 2	R/W Note 1

Notes 1. P121 to P124 and P137 are read-only.

2. P130 bit depends on the setting of User Option Byte (000C2H/020C2H).
RESOUTB = 0 (Selects P130 as the RESOUT pin): P130 = 1
RESOUTB = 1 (Selects P130 as a general port pin): P130 = 0

No.6 Figure 4-79. Format of Port Mode Control Register (100-pin products)

Figure 4-79. Format of Port Mode Control Register (100-pin products)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PMC7	1	1	1	PMC74 Note 1	PMC73 Note 1	PMC72 Note1	PMC71 Note1	PMC70	F0067H	FFH	R/W

Notes 1. Be sure to clear the following bits to 0.
PMC71 to PMC74 bits in the RL78/F14 products with 64 pins and 128 Kbytes to 256 Kbytes of code flash memory.
PMC73 bit in the RL78/F14 products with 48 pins and 128 Kbytes to 256 Kbytes of code flash memory.
2. The ADPC and PMC9 registers are used to select the digital I/O or analog input functions for the P96/ANI16 and P97/ANI17 pins and for the P96/ANI26 and P97/ANI27 pins, respectively. For details on pin functions allocated to each product, see 1.5 Pin Configurations.

Cautions 1. Be sure to set bits for pins that are not present to their initial values, and see Note 1 for PMC71 to PMC74.
2. Set port pins specified as analog input pins to input mode by using port mode register x (PMx).

No.7 Figure 5-18. Format of LIN Clock Select Register (LINCKSEL)

Figure 5-18. Format of LIN Clock Select Register (LINCKSEL)

Address: F02C3H After reset: 00H R/W

Symbol	7	6	<5>	<4>	3	2	<1>	<0>
LINCKSEL	0	0	LIN1MCKE Note	LIN0MCKE	0	0	LIN1MCK Note	LIN0MCK

Cautions 1. Select the LINn operating clock with the LINnMCK bit before setting the LINnMCKE (n = 0, 1) bit to 1.
2. When operating LINn in SNOOZE mode, set the LINnMCK bit to 0.
3. In case of LINnMCK is set to 1, do not use the timeout error detection.
In that case, set at least 1.2 times the frequency of the LIN communication clock source to the f_{CLK} clock.

No.8 5.7.2 High-Speed On-Chip Oscillator

5.7.2 High-Speed On-Chip Oscillator

When the FRQSEL3 bit is set to 0 (high-speed on-chip oscillator = 48/ 24/ 12/ 6/ 3 MHz), and moreover the CPU/peripheral hardware clock is selected as the PLL clock, the CPU/peripheral hardware clock frequency (f_{CLK}) must not be set to 32 MHz.

No.9 6.2.2 Timer data register mn (TDRmn)

6.2.2 Timer data register mn (TDRmn)

This is a 16-bit register from which a capture function and a compare function can be selected.
The capture or compare function can be switched by selecting an operation mode by using the MDmn3 to MDmn0 bits of timer mode register mn (TMRmn).
When the TDRmn register is used for compare function, the value can be changed at any time.

No.10 Table 8-2. Timer RD Register Configuration

Table 8-2. Timer RD Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
Timer RD Control Register 1	TRDCR1	00H Note	F0280H	1, 8

Note The timer RD SFRs are undefined when FRQSEL4 = 1 in the user option byte (000C2H/020C2H) and TRD0EN = 0 in the PER1 register. If it is necessary to read the initial value, set f_{CLK} to f_{IH} and TRD0EN = 1 before reading.

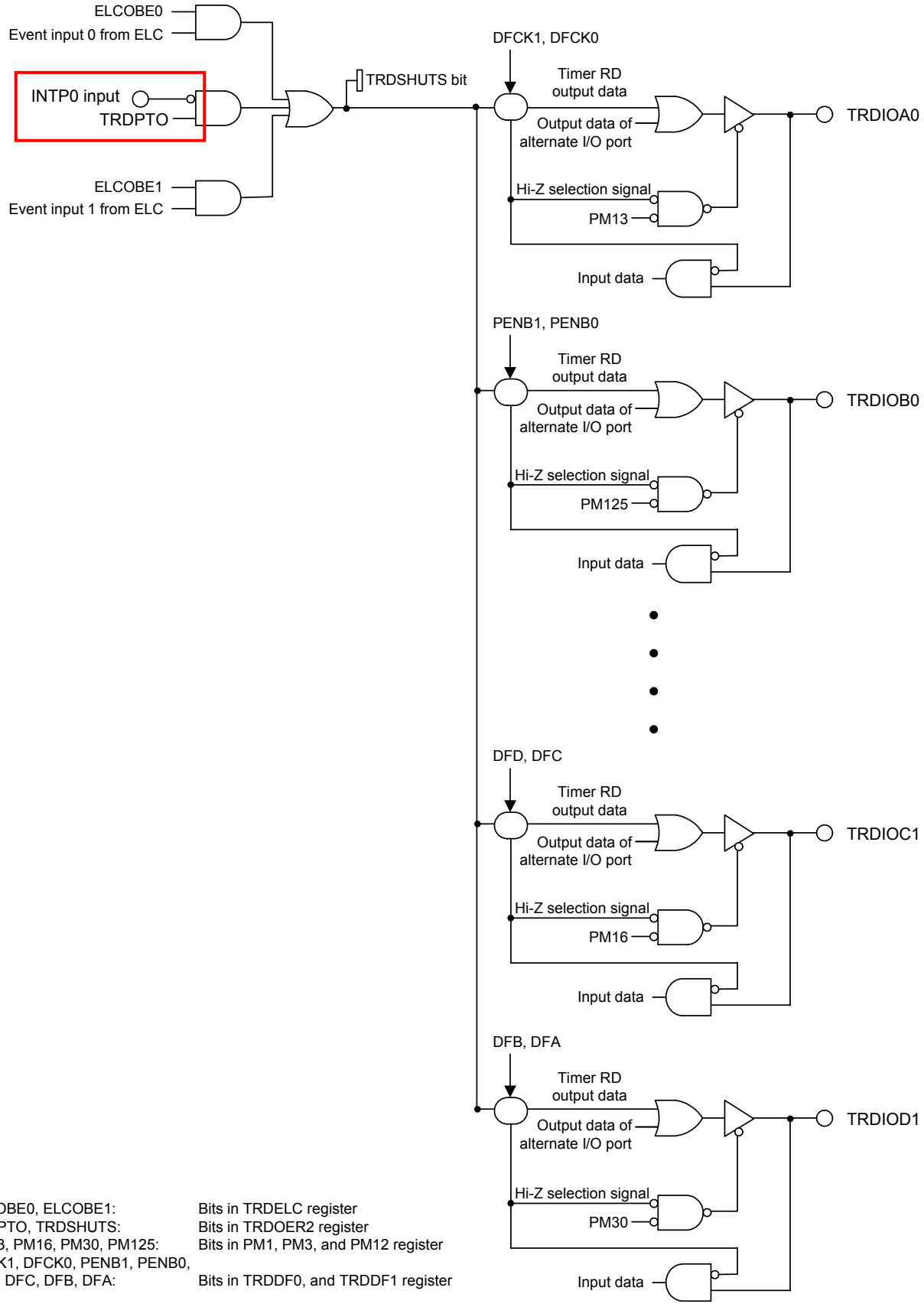
No.11 8.2.19 Timer RD General Register Ai, Bi, Ci, Di (TRDGRAi, TRDGRBi, TRDGRCi, TRDGRDi)

[Complementary PWM Mode]

Access registers TRDGRAi to TRDGRDi in 16-bit units. Do not access them in 8-bit units.
The TRDGRC0 register is not used in complementary PWM mode.
The following registers are disabled in complementary PWM mode.
TRDPMR, TRDOCR Note, ~~TRDDF0, TRDDF1,~~ TRDIORA0, TRDIORC0, TRDPOCR0, TRDIORA1, TRDIORC1, and TRDPOCR1

No.12 Figure 8-44. Pulse Output Forced Cutoff Correction of INTP0 input part (active level).

Figure 8-44. Pulse Output Forced Cutoff



ELCOBE0, ELCOBE1: Bits in TRDELC register
TRDPTO, TRDSHUTS: Bits in TRDOER2 register
PM13, PM16, PM30, PM125: Bits in PM1, PM3, and PM12 register
DFCK1, DFCK0, PENB1, PENB0, DFD, DFC, DFB, DFA: Bits in TRDDF0, and TRDDF1 register

No.13 Figure 9-8. Format of Real-time Clock Control Register 1 (RTCC1)

RWAIT	Wait control of real-time clock
0	Sets counter operation.
1	Stops SEC to YEAR counters. Mode to read or write counter value

This bit controls the operation of the counter.
Be sure to write "1" to it to read or write the counter value.

As the internal counter (16 bits) is continuing to run, complete reading or writing within one second and turn back to 0.
When RWAIT = 1, it takes up to 1 operating clock (f_{RTC}) until the counter value can be read or written (RWST = 1). Notes 1, 2
When the internal counter (16 bits) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT = 0, then counts up.

However, when it wrote a value to second count register, it will not keep the overflow event.

Notes 1. When setting RWAIT=1 during 1 operating clock (f_{RTC}) after setting RTCE=1, it may take two clock time of the operation clock (f_{RTC}) until RWST bit becomes "1".

Notes 2. When setting RWAIT=1 during 1 operating clock (f_{RTC}) after returning from a stand-by (HALT mode, STOP mode, SNOOZE mode), it may take two clock time of the operation clock (f_{RTC}) until RWST bit becomes "1".

No.14 Table 11-3. Setting of Overflow Time of Watchdog Timer

Table 11-3. Setting of Overflow Time of Watchdog Timer

WDCS2	WDCS1	WDCS0	Overflow Time of Watchdog Timer (f_{WDT} = 17.25 kHz (MAX.))
0	0	0	$2^6/f_{WDT}$ (3.71 ms)
0	0	1	$2^7/f_{WDT}$ (7.42 ms)
0	1	0	$2^8/f_{WDT}$ (14.84 ms)
0	1	1	$2^9/f_{WDT}$ (29.68 ms)
1	0	0	$2^{11}/f_{WDT}$ (118.72 ms)
1	0	1	$2^{13}/f_{WDT}$ Note (474.89 ms)
1	1	0	$2^{14}/f_{WDT}$ Note (949.79 ms)
1	1	1	$2^{16}/f_{WDT}$ Note (3799.18 ms)

Note When the interval interrupt of watchdog timer is used, do not set the overflow time to $2^{13}/f_{WDT}$, $2^{14}/f_{WDT}$ or $2^{16}/f_{WDT}$.

No.15 12.2 Configuration of A/D Converter

(1) ANI0 to ANI23 (V_{DD}) and ANI24 to ANI30 (EV_{DD}) pins

These are the analog input pins of the twenty channels of the A/D converter. They input analog signals to be converted into digital signals. Pins other than the one selected as the analog input pin can be used as I/O port pins.

Caution ~~If the setting other than $AV_{REFP} = V_{DD}$, $AV_{REFM} = V_{SS}$~~ If the supply setting other than AV_{REFP}, AV_{REFM} is used as the reference voltage of the A/D converter, the conversion accuracy decreases. In addition, since the EV_{DD} system analog pins have lower accuracy than the V_{DD} system analog pins, the V_{DD} analog pins should be used for highly accurate conversion.

No.16 Formats of Port Mode Control Registers 7, 9, and 12 (PMC7, PMC9)

Figure 12-18. Formats of Port Mode Control Registers 7, 9, and 12 (PMC7, PMC9, PMC12)

Address: F0067H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PMC7	1	1	1	PMC74 Note 1	PMC73 Note 1	PMC72 Note 1	PMC71 Note 1	PMC70

Notes 1. Be sure to clear the following bits to 0.
PMC71 to PMC74 bits in the RL78/F14 products with 64 pins and 128 Kbytes to 256 Kbytes of code flash memory.
PMC73 bit in the RL78/F14 products with 48 pins and 128 Kbytes to 256 Kbytes of code flash memory.

2. The ADPC and PMC9 registers are used to select the digital I/O or analog input functions for the P96/ANI16 and P97/ANI17 pins and for the P96/ANI26 and P97/ANI27 pins, respectively. For details on pin functions allocated to each product, see 1.5 Pin Configurations.

Cautions 1. Set port pins specified as analog input pins to input mode by using port mode register x (PMx).

2. Be sure to set bits for pins that are not present to their initial values, and see Note 1 for PMC71 to PMC74.

No.17 Table 13-1. Setting Functions of ANO0/ANI2/P80 Pin

Table 13-1. Setting Functions ANO0/ANI2/P80 Pin

ADPC Register	PM8 Register	DAM Register	DAM2 Register	ADS Register	Functions of ANO0/ANI2/P80 Pin
Digital I/O	Input mode	—	Enables analog output	—	Setting prohibited
			Disables analog output		Digital input
	Output mode	—	Enables analog output	—	Setting prohibited
			Disables analog output		Digital input
Analog I/O	Input mode	Enables D/A conversion operation	Enables analog output	Selects ANI	Setting prohibited
				Does not selects ANI	Analog output (D/A conversion output)
			Disables analog output	Selects ANI	Analog input (to be converted)
				Does not selects ANI	Analog input (not to be converted) Note
		Stops D/A conversion operation	Enables analog output	Selects ANI	Setting prohibited
				Does not selects ANI	Setting prohibited
			Disables analog output	Selects ANI	Analog input (to be converted)
				Does not selects ANI	Analog input (not to be converted)
	Output mode	—	—	—	Setting prohibited

Note This is a setting that the D/A converter is used for internal reference voltage of comparator. In this case, set CVRS1, CVRS0 bits of CMPSEL register to 10b (internal reference voltage (DAC output) is selected).

No.18 SERIAL ARRAY UNIT

Note of Tables “Group A, B, C-1, C-2, D-1, D-2 and E”

- Group A products

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I²C
0	0	CSI00 (supporting SPI function) Note 2	UART0 (supporting LIN-bus)	IIC00
	1	CSI01 (supporting SPI function) Note 2		IIC01

- Products of Groups C-1 and D-1

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I²C
0	0	CSI00 (supporting SPI function) Note 2	UART0 (supporting LIN-bus)	IIC00
	1	CSI01 (supporting SPI function) Note 2		IIC01
1	0	CSI10 (supporting SPI function) ~~Note~~ Note 1, 2	UART1	IIC10
	1	-		-

- Products of Groups B, C-2, D-2 and E

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I²C
0	0	CSI00 (supporting SPI function) Note 2	UART0 (supporting LIN-bus)	IIC00
	1	CSI01 (supporting SPI function) Note 2		IIC01
1	0	CSI00 (supporting SPI function) ~~Note~~ Note 1, 2	UART1	IIC10
	1	CSI01 (supporting SPI function) Note 2		IIC11

~~Note 48-pin products do not support the SPI function.~~

Notes 1. 48-pin, 32-pin and 30-pin products do not have $\overline{\text{SSI10}}$ pin.

2. Set CKPmn bit of SCRmn register to 1, when SSEmn = 1 (Enables $\overline{\text{SSImn}}$ pin input).
(m = 0, 1, n = 0, 1)

Remark Group A: RL78/F13 (LIN incorporated) products with 20, 30, 32, 48 or 64 pins and 16 Kbytes to 64 Kbytes of code flash memory

Group B: RL78/F13 (LIN incorporated) products with 48 or 64 pins and 96 Kbytes to 128 Kbytes of code flash memory or with 80 pins and 64 Kbytes to 128 Kbytes of code flash memory

Group C-1: RL78/F13 (CAN and LIN incorporated) products with 30 or 32 pins

Group C-2: RL78/F13 (CAN and LIN incorporated) products with 48, 64 or 80 pins

Group D-1: RL78/F14 products with 30 or 32 pins

Group D-2: RL78/F14 products with 48, 64 or 80 pins and 48 Kbytes to 96 Kbytes of code flash memory

Group E: RL78/F14 products with 48, 64 or 80 pins and 128 Kbytes to 256 Kbytes of code flash memory or with 100 pins and 64 Kbytes to 256 Kbytes of code flash memory

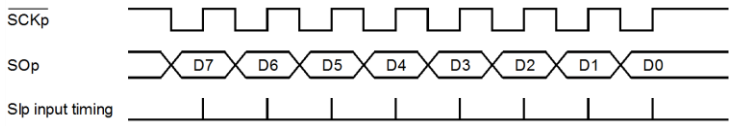
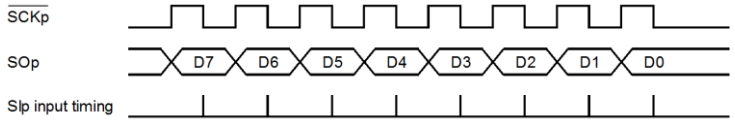
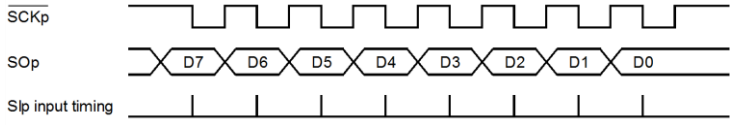
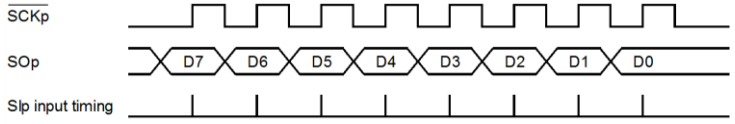
No.19 Figure 15-7. Format of Serial Communication Operation Setting Register mn (SCRmn)

Figure 15-7. Format of Serial Communication Operation Setting Register mn (SCRmn) (1/3)

Address: F010CH, F010DH (SCR00), F010EH, F010FH (SCR01), F014CH, F014DH (SCR10), F014EH, F014FH (SCR11) After reset: 0087H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRmn	TXE mn	RXE mn	DAP mn	CKP mn	0	0	PTC mn1	PTC mn0	DIR mn	0	SLC mn1	SLC mn0	DLS mn3	DLS mn2	DLS mn1	DLS mn0

TXEmn	RXEmn	Setting of operation mode of channel n
0	0	Disable communication
0	1	Reception only
1	0	Transmission only
1	1	Transmission / reception

DAPmn	CKPmn	Selection of data and clock phase in CSI mode	Type
0	0		1
0	1		2
1	0		3
1	1		4

Be sure to set DAPmn, CKPmn = 0, 0 in the UART mode and simplified I^2C mode.

Set CKPmn to 1, when SSEmn = 1 (Enables $\overline{\text{SSImn}}$ pin input).

No.20 Figure 15-17. Format of Serial Slave Select Enable Register m (SSEm)

Figure 15-17. Format of Serial Slave Select Enable Register m (SSEm)

Address: F0122H, F0123H (SSE0) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSE0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SSE 01	SSE 00

Address: F0162H, F0163H (SSE1) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSE1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SSE 11	SSE 10

SSEmn Note	Channel n $\overline{\text{SSImn}}$ input setting in CSI communication and slave mode
0	Disables $\overline{\text{SSImn}}$ pin input.
1	Enables $\overline{\text{SSImn}}$ pin input.

Note Set CKPmn bit of SCRmn register to 1, when SSEmn = 1.

No.21 LIN Clock Select Register (LINCKSEL)

17.2.1 LIN Registers for Master Mode, 17.2.2 LIN Registers for Slave Mode, and 17.2.3 Registers for UART

Address: F02C3H After reset: 00H R/W

Symbol	7	6	<5>	<4>	3	2	<1>	<0>
LINCKSEL	0	0	LIN1MCKE Note	LIN0MCKE	0	0	LIN1MCK Note	LIN0MCK

Cautions 1. Select the LINn operating clock with the LINnMCK bit before setting the LINnMCKE (n = 0, 1) bit to 1 (operating clock is supplied).

2. When operating LINn in SNOOZE mode, set the LINnMCK bit to 0.

3. In case of LINnMCK is set to 1, do not used the timeout error detection.
In that case, set at least 1.2 times the frequency of the LIN communication clock source to the f_{CLK} clock.

No.22 LIN/UART Error Detection Enable Register (LEDEn)

17.2.1 LIN Registers for Master Mode, 17.2.2 LIN Registers for Slave Mode

BERE bit (bit error detection enable bit)

The BERE bit enables or disables detection of the bit error.

~~With 0 set, the bit error is not detected.~~

~~With 1 set, the bit error is detected.~~

Set 1(the bit error detection enables) to this bit.

The bit error detection result of the bit error is indicated in the BER flag in the LESTn register.

For details of the bit error, refer to **17.4.6 Error Status.**

FERE bit (framing error detection enable bit)

The FERE bit enables or disables detection of the framing error.

~~With 0 set, the framing error is not detected.~~

~~With 1 set, the framing error is detected.~~

Set 1(the framing error detection enables) to this bit.

The framing error detection result is indicated in the FER flag in the LESTn register.

For details of the framing error, refer to **17.4.6 Error Status**.

No.23 LIN/UART Transmission Control Register (LTRCn)

FTS bit (LIN communication start bit)

Set the FTS bit to 1 to start header or wake-up reception (counting of the low width of the input signal).

Also set this bit to 1 to allow wake-up transmission.

Only 1 can be written to this bit; 0 cannot be written.

~~The LRXDn pin should be high when setting this bit to 1 in LIN operating mode while operating as a LIN slave (at a fixed baud rate).~~

No.24 17.2.2 LIN Registers for Slave Mode, (20) LIN/UART Data Field Configuration Register (LDFCn)

RFDL[3:0] bits (response field length select bits)

The RFDL bits set the length of the response field data.

The data length can be 0 to 8 bytes excluding the checksum size.

Set these bits when the RTS bit is 0 (response transmission/reception stopped).

When response data of 9 bytes or more is to be transmitted and received, only the last data group (the LSS bit is 0) includes the checksum, and no other groups (the LSS bit is 1) include the checksum.

No.25 17.2.3 Registers for UART, (11) LIN/UART Space Configuration Register (LSCn)

IBS[1:0] bits (Inter-byte space select bits)

The IBS bits set the width of the space between UART frames in transmission using UART buffer.

0 Tbit to 3 Tbits can be set.

When transmitting from the transmission buffer (LUTDRn register) and the wait transmission buffer (LUWTDRn register), set 00b to the IBS[1:0] bit.

No.26 17.2.3 Registers for UART, (16) LIN/UART Status Register (LSTn)

FTC flag (successful buffer transmission flag)

Only 0 can be written to the FTC flag; when 1 is written, the bit retains the value that has been retained before 1 is written.

Whether or not an error has occurred, this bit is set to 1 upon completion of transmission of data, which is equal to the number of data units set with the MDL bits in the LDFCn register, from UART buffer. Here, an interrupt is generated. ~~Note that when the response or wake-up transmission is completed with the FTC flag set to 1, an interrupt is not generated.~~

To clear the bit to 0, write 0 to the bit.

No.27 17.2.3 Registers for UART, (22) UART Operation Error Register (LUOERn)

UROE bit (reception enable bit)

The UROE bit enables or disables reception.

With 0 set, reception is disabled.

With 1 set, reception is enabled.

Do not clear this bit during reception. To cancel transfer while reception is in progress, place the module in the LIN reset mode by setting the OM0 bit in the LCUCn register to 0 (LIN reset mode). Note that this operation also cancels transmission.

This bit must be 0 during transmitting data from UART buffer.

No.28 Table 17-14. Types of Statuses in LIN Master Mode, Table 17-15. Types of Statuses in LIN Slave Mode

Table 17-14. Types of Statuses in LIN Master Mode

Notes 1. In LIN wake-up mode and LIN operation mode, the ERR flag in the LSTn register is cleared to 0 by writing 0 to the PRER flag, CSER flag, FER flag, FTER flag, PBER flag or BER flags in the LESTn register.

Table 17-15. Types of Statuses in LIN Slave Mode

Notes 1. In LIN wake-up mode and LIN operation mode, the ERR flag in the LSTn register is cleared to 0 by writing 0 to the PRER flag, IPER flag, CSER flag, SFER flag, FER flag, TER flag or BER flags in the LESTn register.

No.29 Table 17-16. Types of Error Statuses in LIN Master Mode

Table 17-16. Types of Error Statuses in LIN Master Mode

Notes 3. The timeout time depends on the response field data length (the RFDL[3:0] bits in the LDFCn register) and the checksum selection (the CSM bit in the LDFCn register), and this can be calculated according to the following formula:

Timeout time is 8 data bytes until setting of LTRCn register in frame separate mode (FSM bit of LDFCn register is set to 1).

[Frame timeout]

- On classic selection (when the CSM bit in the LDFCn register is 0):
  Timeout time = 49 + (number of data bytes + 1) × 14 [Tbit]
- On enhanced selection (when the CSM bit in the LDFCn register is 1):
  Timeout time = 48 + (number of data bytes + 1) × 14 [Tbit]

No.30 Table 17-16. Types of Error Statuses in LIN Master Mode, Table 17-17. Types of Error Statuses in LIN Slave Mode

Table 17-16. Types of Error Statuses in LIN Master Mode

Notes 1. If a bit error is detected, the process is canceled after a stop bit is sent. If a bit error is detected in a non-data area, such as an inter-byte space, the transmission is canceled immediately ~~after that area~~ after transmission of error bit. If a bit error is detected during the transmission of a wake-up, the transmission of the wake-up is canceled after the error-causing bit is sent.

Table 17-17. Types of Error Statuses in LIN Slave Mode

Notes 1. If a bit error is detected, the process is canceled after a stop bit is sent. If a bit error is detected in a non-data area, such as an inter-byte space, the transmission is canceled immediately ~~after that area~~ after transmission of error bit. If a bit error is detected during the transmission of a wake-up, the transmission of the wake-up is canceled after the error-causing bit is sent.

No.31 Figure 17-30. Expansion Bit Reception Example (with Data Comparison) (LSB First, UEBDL = 0)

Figure 17-30. Expansion Bit Reception Example (with Data Comparison) (LSB First, UEBDL = 0)

Caution If a reception error (parity error, framing error, or overrun error) occurs, a LINn reception status interrupt is generated, and the error flag is updated. In the case of an overrun error with matching of the compare result, EXBT and IDMT flags are also set to 1.

No.32 17.6.2 Transmission in LIN Master Self-Test Mode, 17.6.3 Reception in LIN Master Self-Test Mode, 17.6.4 Transmission in LIN Slave Self-Test Mode, and 17.6.5 Reception in LIN Slave Self-Test Mode

17.6.2 Transmission in LIN Master Self-Test Mode

- Start header transmission followed with response transmission
  LDFCn register = 00x1xxxxb
  Set the FTS bit in the LTRCn register to 1 (frame transmission or wake-up transmission/reception started).
  The LIN master self-test mode (transmission) is executed. In this mode, interrupts are generated, and status and error status are also updated appropriately. The checksum is automatically computed by the LIN/UART module. When the execution of LIN master self-test mode (transmission) is aborted, set OM0 bit of LCUCn register to 0 (LIN reset mode).

17.6.3 Reception in LIN Master Self-Test Mode

- Start header transmission followed with response reception
  The LIN master self-test mode (reception) is executed. In this mode, interrupts are generated, and status and error status are also updated appropriately. When the execution of LIN master self-test mode (reception) is aborted, set OM0 bit of LCUCn register to 0 (LIN reset mode).

17.6.4 Transmission in LIN Slave Self-Test Mode

- Start header reception followed with response transmission
  Set the FTS bit in the LTRCn register to 1 (header reception or wake-up transmission/reception started).
  (Without any operation involving the RTS bit in the LTRCn register, the reception of a header and the transmission of a response are executed, in the indicated order.)
  The LIN slave self-test mode (transmission) is executed. In this mode, interrupts are generated, and status and error status are also updated appropriately. The checksum is automatically computed by the LIN/UART module. When the execution of LIN master self-test mode (transmission) is aborted, set OM0 bit of LCUCn register to 0 (LIN reset mode).

17.6.5 Reception in LIN Slave Self-Test Mode

- Start header reception followed with response reception
  Set the FTS bit in the LTRCn register to 1 (header reception or wake-up transmission/reception started).
  (Without any operation involving the RTS bit in the LTRCn register, the reception of a header and the reception of a response are executed, in the indicated order.)
  The LIN slave self-test mode (reception) is executed. In this mode, interrupts are generated, and status and error status are also updated appropriately. When the execution of LIN master self-test mode (reception) is aborted, set OM0 bit of LCUCn register to 0 (LIN reset mode).

No.33 17.7 Baud Rate Generator, 17.7.1 LIN Master Mode, and 17.7.2 LIN Slave Mode

17.7.1 LIN Master Mode

17.7.2 LIN Slave Mode

Set the LIN communications clock source as follows.

- LIN communications clock source ~~≤~~ = f_{CLK}[Note1]
- In the range from 4 MHz to 32 MHz

Note 1. ~~If the high-speed system clock (f_{MX}) is to be selected as the LIN communications clock source, and the high-speed on-chip oscillator clock (f_{IH}) or the PLL clock with its source as the high-speed on-chip oscillator clock is to be selected as the source of the clock signal for f_{CLK}, make sure that the condition (LIN communications clock source) < f_{CLK} is satisfied.~~ When the timeout error detection is not used, the f_{MX} clock is selectable as the LIN communication clock source. In that case, set at least 1.2 times the frequency of the LIN communication clock source to the CPU/peripheral hardware clock (f_{CLK}).

No.34 17.7 Baud Rate Generator, 17.7.3 UART Mode

17.7.3 UART Mode

Set the LIN communications clock source as follows.

- LIN communications clock source ~~≤~~ = f_{CLK}[Note1]
- In the range from 4 MHz to 32 MHz

Note 1. ~~If the high-speed system clock (f_{MX}) is to be selected as the LIN communications clock source, and the high-speed on-chip oscillator clock (f_{IH}) or the PLL clock with its source as the high-speed on-chip oscillator clock is to be selected as the source of the clock signal for f_{CLK}, make sure that the condition (LIN communications clock source) < f_{CLK} is satisfied.~~ It is available to select the f_{MX} to the LIN communications clock source. In that case, set at least 1.2 times the frequency of the LIN communication clock source to the CPU/peripheral hardware clock (f_{CLK}).

No.35 18.3.7 CANi Error Flag Register L (CiERFLL), 18.3.35 CAN Receive FIFO Status Register m (RFSTSm), 18.3.47 CANi Transmit/Receive FIFO Status Register k (CFSTSk), and 18.3.75 CANi Transmit History Buffer Status Register (THLSTSi)

18.3.7 CANi Error Flag Register L (CiERFLL)

18.3.35 CAN Receive FIFO Status Register m (RFSTSm)

18.3.47 CANi Transmit/Receive FIFO Status Register k (CFSTSk)

18.3.75 CANi Transmit History Buffer Status Register (THLSTSi)

Note The only effective value for writing to this flag bit is 0, which clears the bit. Otherwise writing to the bit results in retention of its state. To write 0 to this flag bit, write by using an 8-bit data transfer instruction or a 16-bit data transfer instruction.

No.36 18.3.14 CAN Global Error Flag Register (GERFLL)

18.3.14 CAN Global Error Flag Register (GERFLL)

Note The only effective value for writing to this flag bit is 0, which clears the bit. Otherwise writing to the bit results in retention of its state. To write 0 to this flag bit, write by using an 8-bit data transfer instruction.

No.37 18.3.46 CANi Transmit/Receive FIFO Control Register kH (CFCCHk)

- CFITR Bit
  This bit is valid when the setting of the CFITSS bit is ~~1~~ 0.
- CFITSS Bit
  Setting this bit to 0 selects the clock selected by the CFITR bit as the clock source for counting by the interval timer.

No.38 19.4.3 DTC Pending Instruction

If a transfer request is generated from the DTC to the CPU, the DTC is not activated immediately after the following instructions. Also, the DTC is not activated between PREFIX instruction code and the instruction immediately after that code.

- Call/return instruction
- Unconditional branch instruction
- Conditional branch instruction
- Read access instruction for code flash memory
- Bit manipulation instructions for IFxx, MKxx, PRxx, and PSW, and an 8-bit manipulation instruction that has the ES register as operand
- Instruction for accessing the data flash memory
- Multiply, Divide, Multiply & accumulate instruction (exclude MULU instruction)

No.39 Table 21-1. Interrupt Source List (3/4)

Table 21-1. Interrupt Source List (3/4)

Interrupt Type	Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type Note 2	80, 100-pin	64-pin	48-pin	32-pin	30-pin	20-pin
		Name	Trigger									
Maskable	47	INTFL	Reserved Note 5	Internal	0062H	(A)	√	√	√	√	√	√

Notes 5. ~~Used only for the flash self-programming library and data flash library.~~ Do not use this interrupt.

No.40 21.4.4 Interrupt servicing during division instruction

Caution Disable interrupts when executing the DIVHU or DIVWU instruction in an interrupt servicing routine. Alternatively, unless they are executed in the RAM area, note that execution of a DIVHU or DIVWU instruction is possible even with interrupts enabled as long as a NOP instruction is added immediately after the DIVHU or DIVWU instruction in the assembly language source code. The following compilers automatically add a NOP instruction immediately after any DIVHU or DIVWU instruction output during the build process.

- V. 1.71 and later versions of the CA78K0R (Renesas Electronics compiler), for both C and assembly language source code
- Service pack 1.40.6 and later versions of the EWRL78 (IAR compiler), for C language source code
- GNURL78 (KPIT compiler), for C language source code

No.41 21.4.5 Interrupt request hold

21.4.5 Interrupt request hold

There are instructions where, even if an interrupt request is issued while the instructions are being executed, interrupt request acknowledgment is held pending until the end of execution of the next instruction. These instructions (interrupt request hold instructions) are listed below.

- MOV PSW, #byte
- MOV PSW, A

  :

  :
- MULHU
- MULH
- MACHU
- MACH
- Manipulation instructions for the IF0L, IF0H, IF1L, IF1H, IF2L, IF2H, IF3L, MK0L, MK0H, MK1L, MK1H, MK2L, MK2H, MK3L, PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR03L, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H, and PR13L registers

No.42 Figure 27-9. Format of 1-bit Error Detection Interrupt Enable Register (ECCIER)

Figure 27-9. Format of 1-bit Error Detection Interrupt Enable Register (ECCIER)

Address: F0202H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ECCIER	-	-	-	-	-	-	-	IEN

IEN	1-bit error detection interrupt enable bit
0	Interrupt disabled
1	Interrupt enabled

Cautions 1. Bits 1 to 7 of the ECCIER register are always read as 0. The write value should always be 0.

2. INTRAM interrupt request occurs regardless of the value of ECCIER on two bits error.

No.43 27.3.4 CPU stack pointer monitor function

27.3.4 CPU stack pointer monitor function

The CPU stack pointer monitor is used to detect overflows and underflows of the stack pointer and to generate interrupts in response.

Caution The CPU stack pointer monitor function is disabled during on-chip debugging.

No.44 Figure 27-20. Format of invalid Memory Access Detection Control Register (IAWCTL)

Figure 27-20. Format of Invalid Memory Access Detection Control Register (IAWCTL)

Address: F0078H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
IAWCTL	IAWEN	0	GRAM1	GRAM0	0	GPORT	GINT	GCSC

GCSC ~~Note 2~~	Control registers of clock control function and voltage detector guard
0	Disabled. Control registers of clock control function and voltage detector can be read or written to.
1	Enabled. Writing to control registers of clock control function and voltage detector is disabled. Reading is enabled. [Guarded SFR] CMC, CSC, OSTS, CKC, PERx, OSMC, LVIM, LVIS, CANCKSEL, LINCKSEL, CKSEL, PLLCTL, MDIV, RTCCL, POCRES, STPSTC

Note Pxx (Port register) is not guarded.

~~2. Clear GCSC bit to 0, during self programming.~~

No.45 Table 33-5. Operation List (12/18)

Table 33-5. Operation List (12/18)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
Multiply, Divide, Multiply & accumu-late	MULU	X	1	1	–	AX ← A × X			
	MULHU		3	2	–	BCAX ← AX × BC (unsigned)			
	MULH		3	2	–	BCAX ← AX × BC (signed)			
	DIVHU		3	9	–	AX (quotient), DE (remainder) ← AX ÷ DE (unsigned)			
	DIVWU		3	17	–	BCAX (quotient), HLDE (remainder) ← BCAX ÷ HLDE (unsigned)			
	MACHU		3	3	–	MACR ← MACR + AX × BC (unsigned)		×	×
	MACH		3	3	–	MACR ← MACR + AX × BC(signed)		×	×

Notes 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

2. Number of CPU clocks (f_{CLK}) when the program memory area is accessed.

Caution Disable interrupts when executing the DIVHU or DIVWU instruction in an interrupt servicing routine. Alternatively, unless they are executed in the RAM area, note that execution of a DIVHU or DIVWU instruction is possible even with interrupts enabled as long as a NOP instruction is added immediately after the DIVHU or DIVWU instruction in the assembly language source code. The following compilers automatically add a NOP instruction immediately after any DIVHU or DIVWU instruction output during the build process.

- V.1.71 and later versions of the CA78K0R (Renesas Electronics compiler), for both C and assembly language source code
- Service pack 1.40.6 and later versions of the EWRL78 (IAR compiler), for C language source code
- GNURL78 (KPIT compiler), for C language source code

No.46 34.3.1 Pin Characteristics, 35.3.1 Pin Characteristics, 36.3.1 Pin Characteristics

34.3.1 Pin Characteristics (1/4)

35.3.1 Pin Characteristics (1/4)

36.3.1 Pin Characteristics (1/4)

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from pins EV_{DD0}, EV_{DD1} and V_{DD} to an output pin.

No.47 34.3.1 Pin Characteristics, 35.3.1 Pin Characteristics, 36.3.1 Pin Characteristics

34.3.1 Pin Characteristics (2/4)

35.3.1 Pin Characteristics (2/4)

36.3.1 Pin Characteristics (2/4)

Notes 1. Value of current at which the device operation is guaranteed even if the current flows to the EV_{SS0}, EV_{SS1} and V_{SS} pins from an output pin.

No.48 34.4 AC Characteristics, 35.4 AC Characteristics, 36.4 AC Characteristics

34.4.1 Basic Operation (1/2)

35.4.1 Basic Operation (1/2)

36.4.1 Basic Operation (1/2)

Note Pins $\overline{\text{RESET}}$, INTP0 to INTP3, INTP12, and INTP13 have noise filters for transient levels lasting less than 100 ns.

No.49 34.5.1 Serial Array Unit, 35.5.1 Serial Array Unit, 36.5.1 Serial Array Unit

(7) During communication at same potential (simplified I^2C mode) (SDAr and ACLr: N-ch open-drain output (EV_{DD0} tolerance) mode)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}			400Note	kHz
Hold time when SCLr = "L"	t_{LOW}	4.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 1.7 kΩ	1300		ns
		2.7 V ≤ V_{DD} < 4.0 V, C_b = 100 pF, R_b = ~~5.7~~ 2.7 kΩ			
Hold time when SCLr = "H"	t_{HIGH}	4.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 1.7 kΩ	600		ns
		2.7 V ≤ V_{DD} < 4.0 V, C_b = 100 pF, R_b = ~~5.7~~ 2.7 kΩ			
Data setup time (reception)	$t_{SU:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 1.7 kΩ	1/f_{MCK} + 120		ns
		2.7 V ≤ V_{DD} < 4.0 V, C_b = 100 pF, R_b = ~~5.7~~ 2.7 kΩ	1/f_{MCK} + 270		ns
Data hold time (transmission)	$t_{HD:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 1.7 kΩ	0	300	ns
		2.7 V ≤ V_{DD} < 4.0 V, C_b = 100 pF, R_b = ~~5.7~~ 2.7 kΩ			

Note $f_{CLK} \leq f_{MCK}/4$ must also be satisfied.

No.50 34.9 Flash Memory Programming Characteristics, 35.9 Flash Memory Programming Characteristics, 36.9 Flash Memory Programming Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Erase time	T_{erasa}	~~Sector erase~~ Block erase	5			ms

No.51 36.1 Absolute Maximum Ratings

36.1 Absolute Maximum Ratings (2/2)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, low	I_{OL1}	Per pin	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P92 to P97Note 1, ~~P1060~~ P106, P107, P120, P125 to P127, P130, P140, P150 to P157	40	mA
		Total of all pins 170 mA	P01, P02, P40 to P47, P92 to P97Note 1, P120, P125 to P127, P150 to P153	70	mA
			P00, P03, P10 to P17, P30 to P32, P50 to P57, P60 to P67, P70 to P77, ~~P1060~~ P106, P107, P130, P140, P154 to P157	100	mA
	I_{OL2}	Per pin	P33, P34, P80 to P87, P90 to P97Note 1, P100 to P105	1	mA
		Total of all pins		5	mA

Note 1. For pin I/O buffer power supplies, refer to Table 4-1 Pin I/O Buffer Power Supplies.