Date: March. 13, 2012

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-V85-A002A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice V850ES/JG3-L(on-chip USB controller) Descriptions in the Hardware User's Manual Rev.2.00 Changed		Information Category	Technical Notification		
Applicable Product	V850ES/JG3-L (on-chip USB controller) μPD70F3794, μPD70F3795, μPD70F3796, μPD70F3843, μPD70F3844	Lot No. All Lot	Reference Document	V850ES/JG3-L (on-chip USB controller) User's Manual: Hardware R01UH0001EJ0200 (Rev.2.00)		

This document describes misstatements found in the V850ES/JG3-L (on-chip USB controller) hardware user's manual Rev.2.00 (R01UH0001EJ0200).

Cancelation line parts (ex. ~~separate bus/~~) are deleted and gray parts (ex. 6) are changed.

The above corrections will be made for the next revision of the hardware user's manual.

No. 1

Location: Table 1-1 on page 22

Incorrect:

Generic Name		V850ES/JG3-L				
Product Name		μPD70F3794	μPD70F3795	μPD70F3796	μPD70F3843	μPD70F3844
Internal memory	Flash memory	256 KB	384 KB	512 KB	768 KB	1 MB
	RAM	40 KB			80 KB Note1	
Memory Space	Logical space	64 MB				
	External memory area	13 MB				
External bus interface		Address buses: 22 Address data bus: 16 Separate bus/multiplexed bus mode selectable				

Correct:

Generic Name		V850ES/JG3-L				
Product Name		μPD70F3794	μPD70F3795	μPD70F3796	μPD70F3843	μPD70F3844
Internal memory	Flash memory	256 KB	384 KB	512 KB	768 KB	1 MB
	RAM	40 KB			80 KB Note1	
Memory Space	Logical space	64 MB				
	External memory area	13 MB				
External bus interface		Address buses: 6 Address data bus: 16 ~~Separate bus/~~multiplexed bus mode ~~selectable~~				

No. 2

Location: 1.2 on page 23

Incorrect:

O Memory space: 64 MB of linear address space (for programs and data)

External expansion: Up to 16 MB (including 1 MB used as internal ROM/RAM)

• Internal memory: RAM: 40 /80 KB (see **Table 1-1**)

Flash memory: 256 K/384 K/512 K/768 K/1 MB (see **Table 1-1**)

• External bus interface: • Multiplexed bus mode (capable of separate output)

Correct:

O Memory space: 64 MB of linear address space (for programs and data)

External expansion: Up to 16 MB (including 1 MB used as internal ROM/RAM)

• Internal memory: RAM: 40 /80 KB (see **Table 1-1**)

Flash memory: 256 K/384 K/512 K/768 K/1 MB (see **Table 1-1**)

• External bus interface: • Multiplexed bus mode ~~(capable of separate output)~~

No. 3

Location: 4.3.7 (4) on page 124

Incorrect:

Caution When performing separate address bus output (A0 to A15), set the PMC9 register to FFFFH for all 16 bits at once after clearing the PFC9 and PFCE9 registers to 0000H.

Correct:

~~**Caution When performing separate address bus output (A0 to A15), set the PMC9 register to FFFFH for all 16 bits at once after clearing the PFC9 and PFCE9 registers to 0000H.**~~

No. 4

Location: 4.3.7 (5) on page 124

Incorrect:

Caution When performing separate address bus output (A0 to A15), set the PMC9 register to FFFFH for all 16 bits at once after clearing the PFC9 and PFCE9 registers to 0000H.

Correct:

~~**Caution When performing separate address bus output (A0 to A15), set the PMC9 register to FFFFH for all 16 bits at once after clearing the PFC9 and PFCE9 registers to 0000H.**~~

No. 5

Location: 5.1 on page 182

Incorrect:

O A multiplexed bus with a minimum of 3 bus cycles and a separate bus output are available.

Correct:

O A multiplexed bus with a minimum of 3 bus cycles ~~and a separate bus output~~ is available.

No. 6

Location: Table 5-1 on page 183

Incorrect:

Bus Control Signal	I/O	Function	Alternate Function	Register to Switch Between Port Mode/Alternate-Function Mode
AD0 to AD15	I/O	Address/data bus	PDL0 to PDL15	PMCDL register
A0 to A15	Output	Address bus (capable of separate output)	P90 to P915	PMC9 register

Correct:

Bus Control Signal	I/O	Function	Alternate Function	Register to Switch Between Port Mode/Alternate-Function Mode
AD0 to AD15	I/O	Address/data bus	PDL0 to PDL15	PMCDL register
~~A0 to A15~~	~~Output~~	~~Address bus (capable of separate output)~~	~~P90 to P915~~	~~PMC9 register~~

No. 7

Location: Table 5-2 on page 183

Incorrect:

Bus Control Pin	Multiplexed Bus Mode			
	Internal ROM/RAM	Peripheral I/O	USB Function area	Expanded Internal RAM area[Note]
Address/data bus (AD15 to AD0)	Undefined	Undefined	Undefined	Undefined
Address bus (A21 to A16)	Low level	Undefined	Undefined	Undefined
Address bus (A15 to A0)	Undefined	Undefined	Undefined	Undefined
Control signal	Inactive	Inactive	Inactive	Inactive

Correct:

Bus Control Pin	Multiplexed Bus Mode			
	Internal ROM/RAM	Peripheral I/O	USB Function area	Expanded Internal RAM area[Note]
Address/data bus (AD15 to AD0)	Undefined	Undefined	Undefined	Undefined
Address bus (A21 to A16)	Low level	Undefined	Undefined	Undefined
~~Address bus (A15 to A0)~~	~~Undefined~~	~~Undefined~~	~~Undefined~~	~~Undefined~~
Control signal	Inactive	Inactive	Inactive	Inactive

No. 8

Location: 5.9 on page 202

Incorrect:

Typical bus timing diagrams are shown below.

When use a separate bus, refer to timing of multiplexed bus mode.

Incorrect:

Typical bus timing diagrams are shown below.

~~When use a separate bus, refer to timing of multiplexed bus mode.~~

No. 9

Location: Figure 5-4 on page 202

Incorrect:

Note A21 to A0 in the case of separate output.

Correct:

~~**Note** A21 to A0 in the case of separate output.~~

No. 10

Location: Figure 5-5 on page 203

Incorrect:

Note A21 to A0 in the case of separate output.

Correct:

~~**Note** A21 to A0 in the case of separate output.~~

No. 11

Location: Figure 5-6 on page 204

Incorrect:

Note A21 to A0 in the case of separate output.

Correct:

~~**Note** A21 to A0 in the case of separate output.~~

No. 12

Location: Figure 5-7 on page 204

Incorrect:

Note A21 to A0 in the case of separate output.

Correct:

~~**Note** A21 to A0 in the case of separate output.~~

No. 13

Location: Figure 5-8 on page 205

Incorrect:

Note1. This idle state (TI) does not depend on the BCC register settings.

2. A21 to A0 in the case of separate output.

Correct:

Note1. This idle state (TI) does not depend on the BCC register settings.

~~**2.** A21 to A0 in the case of separate output.~~

No. 14

Location: Figure 5-9 on page 205

Incorrect:

Note A21 to A0 in the case of separate output.

Correct:

~~**Note** A21 to A0 in the case of separate output.~~

No. 15

Location: 33.7.3 on page 1146

Incorrect:

The values for just the access method to be used (synchronous with or asynchronous to CLKOUT) must be satisfied. It is not necessary to satisfy the values for both methods. When using a separate bus, refer to the specification of multiplexed bus mode.

Correct:

The values for just the access method to be used (synchronous with or asynchronous to CLKOUT) must be satisfied. It is not necessary to satisfy the values for both methods. ~~When using a separate bus, refer to the specification of multiplexed bus mode.~~

No. 16

Location: 33.7.3 (1) (a) **Read Cycle (Asynchronous to CLKOUT): In Multiplexed Bus Mode** on page 1147

Incorrect:

Note When use a separate bus, A0 to A21.

Correct:

~~**Note** When use a separate bus, A0 to A21.~~

No. 17

Location: 33.7.3 (1) (a) **Write Cycle (Asynchronous to CLKOUT): In Multiplexed Bus Mode** on page 1148

Incorrect:

Note When use a separate bus, A0 to A21.

Correct:

~~**Note** When use a separate bus, A0 to A21.~~

No. 18

Location: 33.7.3 (1) (b) **Read Cycle (Synchronous with CLKOUT): In Multiplexed Bus Mode** on page 1149

Incorrect:

Note When use a separate bus, A0 to A21.

Correct:

~~**Note** When use a separate bus, A0 to A21.~~

No. 19

Location: 33.7.3 (1) (b) **Write Cycle (Synchronous with CLKOUT): In Multiplexed Bus Mode** on page 1150

Incorrect:

Note When use a separate bus, A0 to A21.

Correct:

~~**Note** When use a separate bus, A0 to A21.~~

No. 20

Location: 34.7.3 on page 1180

Incorrect:

The values for just the access method to be used (synchronous with or asynchronous to CLKOUT) must be satisfied. It is not necessary to satisfy the values for both methods. When using a separate bus, refer to the specification of multiplexed bus mode.

Correct:

The values for just the access method to be used (synchronous with or asynchronous to CLKOUT) must be satisfied. It is not necessary to satisfy the values for both methods. ~~When using a separate bus, refer to the specification of multiplexed bus mode.~~

No. 21

Location: 34.7.3 (1) (a) **Read Cycle (Asynchronous to CLKOUT): In Multiplexed Bus Mode** on page 1181

Incorrect:

Note When use a separate bus, A0 to A21.

Correct:

~~**Note** When use a separate bus, A0 to A21.~~

No. 22

Location: 34.7.3 (1) (a) **Write Cycle (Asynchronous to CLKOUT): In Multiplexed Bus Mode** on page 1182

Incorrect:

Note When use a separate bus, A0 to A21.

Correct:

~~**Note** When use a separate bus, A0 to A21.~~

No. 23

Location: 34.7.3 (1) (b) **Read Cycle (Synchronous with CLKOUT): In Multiplexed Bus Mode** on page 1183

Incorrect:

Note When use a separate bus, A0 to A21.

Correct:

~~**Note** When use a separate bus, A0 to A21.~~

No. 24

Location: 34.7.3 (1) (b) **Write Cycle (Synchronous with CLKOUT): In Multiplexed Bus Mode** on page 1184

Incorrect:

Note When use a separate bus, A0 to A21.

Correct:

~~**Note** When use a separate bus, A0 to A21.~~