To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A728A/E	Rev.	1.00
Title	Correction of Errors in SH7137 Group Hardware Manual		Information Category	Technical Notification		
Applicable Product	SH7137 Group	Lot No. All lots	Reference Document	SH7137 Group Hardware Manual Rev. 2.00 (REJ09B0402-0200)		

We would like to inform you of the correction of errors in the SH7137 Group Hardware Manual as shown below.

<Corrections>

20.1.4 Port B Control Registers L1, L2 (PBCRL1, PBCRL2)

SH7136:

[Before]

- Port B Control Register L2 (PBCRL2)

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14	PB7MD2	0	R/W	PB7 Mode
13	PB7MD1	0	R/W	Select the function of the PB7/CRx0 pin.
12	PB7MD0	0	R/W	000: PB7 I/O (port) 010: CRx0 input (RCAN-ET) Other than above: Setting prohibited
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10	PB6MD2	0	R/W	PB6 Mode
9	PB6MD1	0	R/W	Select the function of the PB6/CTx0 pin.
8	PB6MD0	0	R/W	000: PB6 I/O (port) 011: CTIx0 output (RCAN-ET) Other than above: Setting prohibited
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6	PB5MD2	0	R/W	PB5 Mode
5	PB5MD1	0	R/W	Select the function of the PB5/IRQ3/POE5/TIC5U pin.
4	PB5MD0	0	R/W	000: PB5 I/O (port) 001: IRQ3 input (INTC) 011: TIC5U input (MTU2) 101: A19 output (BSC)* 111: POE5 input (POE) Other than above: Setting prohibited
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	PB4MD2	0	R/W	PB4 Mode
1	PB4MD1	0	R/W	Select the function of the PB4/IRQ2/POE4/TIC5US pin.
0	PB4MD0	0	R/W	000: PB4 I/O (port) 001: IRQ2 input (INTC) 011: TIC5US input (MTU2S) 101: A18 output (BSC)* 111: POE4 input (POE) Other than above: Setting prohibited

Note: * This function is available only in the on-chip ROM enabled/disabled external-extension mode. Do not set to this value in single-chip mode.

[After]

- Port B Control Register L2 (PBCRL2)

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14	PB7MD2	0	R/W	PB7 Mode
13	PB7MD1	0	R/W	Select the function of the PB7/CRx0 pin.
12	PB7MD0	0	R/W	000: PB7 I/O (port) **110**: CRx0 input (RCAN-ET) Other than above: Setting prohibited
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10	PB6MD2	0	R/W	PB6 Mode
9	PB6MD1	0	R/W	Select the function of the PB6/CTx0 pin.
8	PB6MD0	0	R/W	000: PB6 I/O (port) **110: CTx0** output (RCAN-ET) Other than above: Setting prohibited
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6	PB5MD2	0	R/W	PB5 Mode
5	PB5MD1	0	R/W	Select the function of the PB5/IRQ3/POE5/TIC5U pin.
4	PB5MD0	0	R/W	000: PB5 I/O (port) 001: IRQ3 input (INTC) 011: TIC5U input (MTU2) 111: POE5 input (POE) Other than above: Setting prohibited
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	PB4MD2	0	R/W	PB4 Mode
1	PB4MD1	0	R/W	Select the function of the PB4/IRQ2/POE4/TIC5US pin.
0	PB4MD0	0	R/W	000: PB4 I/O (port) 001: IRQ2 input (INTC) 011: TIC5US input (MTU2S) 111: POE4 input (POE) Other than above: Setting prohibited

SH7137:

[Before]

- Port B Control Register L2 (PBCRL2)

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14	PB7MD2	0	R/W	PB7 Mode
13	PB7MD1	0	R/W	Select the function of the PB7/CS1/CRx0 pin.
12	PB7MD0	0	R/W	000: PB7 I/O (port) 101: CS1 output (BSC)* 010: CRx0 input (RCAN-ET) Other than above: Setting prohibited
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10	PB6MD2	0	R/W	PB6 Mode
9	PB6MD1	0	R/W	Select the function of the PB7/WAIT/CTx0 pin.
8	PB6MD0	0	R/W	000: PB6 I/O (port) 101: WAIT input (BSC)* 010: CTx0 output (RCAN-ET) Other than above: Setting prohibited

[After]

- Port B Control Register L2 (PBCRL2)

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14	PB7MD2	0	R/W	PB7 Mode
13	PB7MD1	0	R/W	Select the function of the PB7/CS1/CRx0 pin.
12	PB7MD0	0	R/W	000: PB7 I/O (port) 101: CS1 output (BSC)* **110**: CRx0 input (RCAN-ET) Other than above: Setting prohibited
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10	PB6MD2	0	R/W	PB6 Mode
9	PB6MD1	0	R/W	Select the function of the **PB6**/WAIT/CTx0 pin.
8	PB6MD0	0	R/W	000: PB6 I/O (port) 101: WAIT input (BSC)* **110**: CTx0 output (RCAN-ET) Other than above: Setting prohibited

[Before]

- Port B Control Register L1 (PBCRL1)

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14	PB3MD2	0*1	R/W	PB3 Mode
13	PB3MD1	0	R/W	Select the function of the PB3/A17/IRQ1/POE1/TIC5V pin.
12	PB3MD0	0*1	R/W	000: PB3 I/O (port) 001: IRQ1 input (INTC) 010: POE1 input (POE) 011: TIC5V input (MTU2) 101: A17 output (BSC)*2 Other than above: Setting prohibited

[After]

- Port B Control Register L1 (PBCRL1)

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14	PB3MD2	0*1	R/W	PB3 Mode
13	PB3MD1	0	R/W	Select the function of the
12	PB3MD0	0*1	R/W	PB3/A17/IRQ1/POE1/TIC5V/**SDA** pin. 000: PB3 I/O (port) 001: IRQ1 input (INTC) 010: POE1 input (POE) 011: TIC5V input (MTU2) **100: SDA I/O (IIC2)** 101: A17 output (BSC)*2 Other than above: Setting prohibited