Date: Nov. 22, 2022

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU	Document No.	TN-RA*-A0067A/E	Rev.	1.00
Title	Correction for “Clock Generation Circuit” in RA2L1/RA2E1 User’s Manual		Information Category	Technical Notification	
Applicable Product	RA Family RA2L1/RA2E1 Group	Lot No. All lots	Reference Document	Renesas RA2L1 Group User’s Manual: Hardware R01UH0853EJ0120 Rev.1.20 (May 20, 2022) Renesas RA2E1 Group User’s Manual: Hardware R01UH0852EJ0120 Rev.1.20 (Feb 4, 2022)	

Supplementary information is added in the Chapter 8 Clock Generation Circuit.

The details are shown from the next page.

Group: RA2L1

8. Clock Generation Circuit

Before)

Table 8.2 Clock generation circuit specifications for the internal clocks (1 of 2)

Item	Clock source	Clock supply	Specification
System clock (ICLK)	MOSC/SOSC/HOCO/MOCO/LOCO	CPU, DTC, Flash, Flash-IF, SRAM	Up to 48 MHz Division ratios: 1/2/4/8/16/32/64 1 MHz to 48 MHz (P/E)
Peripheral module clock B (PCLKB)	MOSC/SOSC/HOCO/MOCO/LOCO	Peripheral modules (CAC, ELC, I/O Ports, KINT, POEG, GPT, AGT, RTC, WDT, IWDT, SCI, IIC, SPI, CRC, ADC12, DAC12, ACMPLP, CTSU, DOC, AES, and TRNG)	Up to 32 MHz Division ratios:1/2/4/8/16/32/64
Peripheral module clock D (PCLKD)	MOSC/SOSC/HOCO/MOCO/LOCO	Peripheral modules (GPT count clock, ADC12 conversion clock)	Up to 64 MHz Division ratios: 1/2/4/8/16/32/64
CAN clock (CANMCLK)	MOSC	CAN	1 MHz to 20 MHz
AGT clock (AGTSCLK/AGTLCLK)	SOSC/LOCO	AGT	32.768 kHz
CAC Main clock (CACMCLK)	MOSC	CAC	Up to 20 MHz
CAC Sub clock (CACSCLK)	SOSC	CAC	32.768 kHz
CAC LOCO clock (CACLCLK)	LOCO	CAC	32.768 kHz
CAC MOCO clock (CACMOCLK)	MOCO	CAC	8 MHz

Table 8.2 Clock generation circuit specifications for the internal clocks (2 of 2)

Item	Clock source	Clock supply	Specification
CAC HOCO clock (CACHCLK)	HOCO	CAC	24/32/48/64 MHz
CAC IWDTLOCO clock (CACILCLK)	IWDTLOCO	CAC	15 kHz
RTC clock (RTCSCLK/RTCS128CLK/RTCLCLK)	SOSC/LOCO	RTC	32.768 kHz / 128 Hz
IWDT clock (IWDTCLK)	IWDTLOCO	IWDT	15 kHz
SysTick timer clock (SYSTICCLK)	LOCO	SysTick timer	32.768 kHz
Clock/buzzer output (CLKOUT)	MOSC/SOSC/LOCO/MOCO/HOCO	CLKOUT pin	Up to 16 MHz Division ratios: 1/2/4/8/16/32/64/128
Serial wire clock (SWCLK)	SWCLK pin	OCD	Up to 12.5 MHz

Note: Restrictions on setting clock frequency: ICLK ≥ PCLKB, PCLKD ≥ PCLKB
PCLKB Restrictions on clock frequency ratio: (N: integer, and up to 64)
ICLK:PCLKB = N:1, ICLK:PCLKD = N:1 or 1:N
Minimum ICLK frequency is 1 MHz in Programming/Erasure (P/E) mode.

After)

The following “Note 1” is added in Table 8.2.

Note 1. This clock is not supplied in Software Standby mode when the RCR4.ROPSEL bit is 1.

Table 8.2 Clock generation circuit specifications for the internal clocks (1 of 2)

Item	Clock source	Clock supply	Specification
System clock (ICLK)	MOSC/SOSC*1/HOCO/MOCO/LOCO	CPU, DTC, Flash, Flash-IF, SRAM	Up to 48 MHz Division ratios: 1/2/4/8/16/32/64 1 MHz to 48 MHz (P/E)
Peripheral module clock B (PCLKB)	MOSC/SOSC*1/HOCO/MOCO/LOCO	Peripheral modules (CAC, ELC, I/O Ports, KINT, POEG, GPT, AGT, RTC, WDT, IWDT, SCI, IIC, SPI, CRC, ADC12, DAC12, ACMPLP, CTSU, DOC, AES, and TRNG)	Up to 32 MHz Division ratios:1/2/4/8/16/32/64
Peripheral module clock D (PCLKD)	MOSC/SOSC*1/HOCO/MOCO/LOCO	Peripheral modules (GPT count clock, ADC12 conversion clock)	Up to 64 MHz Division ratios: 1/2/4/8/16/32/64
CAN clock (CANMCLK)	MOSC	CAN	1 MHz to 20 MHz
AGT clock (AGTSCLK/AGTLCLK)	SOSC*1/LOCO	AGT	32.768 kHz
CAC Main clock (CACMCLK)	MOSC	CAC	Up to 20 MHz
CAC Sub clock (CACSCLK)	SOSC*1	CAC	32.768 kHz
CAC LOCO clock (CACLCLK)	LOCO	CAC	32.768 kHz
CAC MOCO clock (CACMOCLK)	MOCO	CAC	8 MHz

Table 8.2 Clock generation circuit specifications for the internal clocks (2 of 2)

Item	Clock source	Clock supply	Specification
CAC HOCO clock (CACHCLK)	HOCO	CAC	24/32/48/64 MHz
CAC IWDTLOCO clock (CACILCLK)	IWDTLOCO	CAC	15 kHz
RTC clock (RTCSCLK*1/RTCS128CLK/RTCLCLK)	SOSC/LOCO	RTC	32.768 kHz / 128 Hz
IWDT clock (IWDTCLK)	IWDTLOCO	IWDT	15 kHz
SysTick timer clock (SYSTICCLK)	LOCO	SysTick timer	32.768 kHz
Clock/buzzer output (CLKOUT)	MOSC/SOSC*1/LOCO/MOCO/HOCO	CLKOUT pin	Up to 16 MHz Division ratios: 1/2/4/8/16/32/64/128
Serial wire clock (SWCLK)	SWCLK pin	OCD	Up to 12.5 MHz

Note: Restrictions on setting clock frequency: ICLK ≥ PCLKB, PCLKD ≥ PCLKB
PCLKB Restrictions on clock frequency ratio: (N: integer, and up to 64)
ICLK:PCLKB = N:1, ICLK:PCLKD = N:1 or 1:N
Minimum ICLK frequency is 1 MHz in Programming/Erasure (P/E) mode.
Note 1. This clock is not supplied in Software Standby mode when the RCR4.ROPSEL bit is 1.

Group: RA2E1

8. Clock Generation Circuit

Before）

Table 8.2 Clock generation circuit specifications for the internal clocks (1 of 2)

Item	Clock source	Clock supply	Specification
System clock (ICLK)	MOSC/SOSC/HOCO/MOCO/LOCO	CPU, DTC, Flash, Flash-IF, SRAM	Up to 48 MHz Division ratios: 1/2/4/8/16/32/64 1 MHz to 48 MHz (P/E)
Peripheral module clock B (PCLKB)	MOSC/SOSC/HOCO/MOCO/LOCO	Peripheral modules (CAC, ELC, I/O Ports, KINT, POEG, GPT, AGT, RTC, WDT, IWDT, SCI, IIC, SPI, CRC, ADC12, ACMPLP, CTSU, DOC, AES, and TRNG)	Up to 32 MHz Division ratios:1/2/4/8/16/32/64
Peripheral module clock D (PCLKD)	MOSC/SOSC/HOCO/MOCO/LOCO	Peripheral modules (GPT count clock, ADC12 conversion clock)	Up to 64 MHz Division ratios: 1/2/4/8/16/32/64
AGT clock (AGTSCLK/ AGTLCLK)	SOSC/LOCO	AGT	32.768 kHz
CAC Main clock (CACMCLK)	MOSC	CAC	Up to 20 MHz
CAC Sub clock (CACSCLK)	SOSC	CAC	32.768 kHz
CAC LOCO clock (CACLCLK)	LOCO	CAC	32.768 kHz
CAC MOCO clock (CACMOCLK)	MOCO	CAC	8 MHz

Table 8.2 Clock generation circuit specifications for the internal clocks (2 of 2)

Item	Clock source	Clock supply	Specification
CAC HOCO clock (CACHCLK)	HOCO	CAC	24/32/48/64 MHz
CAC IWDTLOCO clock (CACILCLK)	IWDTLOCO	CAC	15 kHz
RTC clock (RTCSCLK/ RTCS128CLK/RTCLCLK)	SOSC/LOCO	RTC	32.768 kHz / 128 Hz
IWDT clock (IWDTCLK)	IWDTLOCO	IWDT	15 kHz
SysTick timer clock (SYSTICCLK)	LOCO	SysTick timer	32.768 kHz
Clock/buzzer output (CLKOUT)	MOSC/SOSC/LOCO/MOCO/HOCO	CLKOUT pin	Up to 16 MHz Division ratios: 1/2/4/8/16/32/64/128
Serial wire clock (SWCLK)	SWCLK pin	OCD	Up to 12.5 MHz

Note: Restrictions on setting clock frequency: ICLK ≥ PCLKB, PCLKD ≥ PCLKB
PCLKB Restrictions on clock frequency ratio: (N: integer, and up to 64)
ICLK:PCLKB = N:1, ICLK:PCLKD = N:1 or 1:N
Minimum ICLK frequency is 1 MHz in Programming/Erasure (P/E) mode.

After）

The following “Note 1” is added in Table 8.2.

Note 1. This clock is not supplied in Software Standby mode when the RCR4.ROPSEL bit is 1.

Table 8.2 Clock generation circuit specifications for the internal clocks (1 of 2)

Item	Clock source	Clock supply	Specification
System clock (ICLK)	MOSC/SOSC*1/HOCO/MOCO/LOCO	CPU, DTC, Flash, Flash-IF, SRAM	Up to 48 MHz Division ratios: 1/2/4/8/16/32/64 1 MHz to 48 MHz (P/E)
Peripheral module clock B (PCLKB)	MOSC/SOSC*1/HOCO/MOCO/LOCO	Peripheral modules (CAC, ELC, I/O Ports, KINT, POEG, GPT, AGT, RTC, WDT, IWDT, SCI, IIC, SPI, CRC, ADC12, ACMPLP, CTSU, DOC, AES, and TRNG)	Up to 32 MHz Division ratios:1/2/4/8/16/32/64
Peripheral module clock D (PCLKD)	MOSC/SOSC*1/HOCO/MOCO/LOCO	Peripheral modules (GPT count clock, ADC12 conversion clock)	Up to 64 MHz Division ratios: 1/2/4/8/16/32/64
AGT clock (AGTSCLK/ AGTLCLK)	SOSC*1/LOCO	AGT	32.768 kHz
CAC Main clock (CACMCLK)	MOSC	CAC	Up to 20 MHz
CAC Sub clock (CACSCLK)	SOSC*1	CAC	32.768 kHz
CAC LOCO clock (CACLCLK)	LOCO	CAC	32.768 kHz
CAC MOCO clock (CACMOCLK)	MOCO	CAC	8 MHz

Table 8.2 Clock generation circuit specifications for the internal clocks (2 of 2)

Item	Clock source	Clock supply	Specification
CAC HOCO clock (CACHCLK)	HOCO	CAC	24/32/48/64 MHz
CAC IWDTLOCO clock (CACILCLK)	IWDTLOCO	CAC	15 kHz
RTC clock (RTCSCLK*1/ RTCS128CLK/RTCLCLK)	SOSC/LOCO	RTC	32.768 kHz / 128 Hz
IWDT clock (IWDTCLK)	IWDTLOCO	IWDT	15 kHz
SysTick timer clock (SYSTICCLK)	LOCO	SysTick timer	32.768 kHz
Clock/buzzer output (CLKOUT)	MOSC/SOSC*1/LOCO/MOCO/HOCO	CLKOUT pin	Up to 16 MHz Division ratios: 1/2/4/8/16/32/64/128
Serial wire clock (SWCLK)	SWCLK pin	OCD	Up to 12.5 MHz

Note: Restrictions on setting clock frequency: ICLK ≥ PCLKB, PCLKD ≥ PCLKB
PCLKB Restrictions on clock frequency ratio: (N: integer, and up to 64)
ICLK:PCLKB = N:1, ICLK:PCLKD = N:1 or 1:N
Minimum ICLK frequency is 1 MHz in Programming/Erasure (P/E) mode.
Note 1. This clock is not supplied in Software Standby mode when the RCR4.ROPSEL bit is 1.