Date: Mar. 17, 2023

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RA*-A0075A/E	Rev.	1.00
Title	Addition to the Electrical Characteristics for the IIC of the RA6T2 Group MCU Products		Information Category	Technical Notification		
Applicable Product	RA6T2 Group	Lot No. All	Reference Document	RA6T2 Group User's Manual : Hardware Rev.1.30		

This document describes addition of specifications for the electrical characteristics of the IIC in the RA6T2 Group User's Manual: Hardware, Rev.1.30.

The characteristics of SCL output minimum high/low pulse widths and START condition input hold time are added to Table 46.32, IIC Timing (2) as follows. Some terms are also corrected.

Before correction

Table 46.32 IIC Timing (2)

Setting of the SCL0_A, SDA0_A pins are not required with the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min.	Max.	Unit	Test Conditions
IIC (Hs-mode) BFCTL.HSME = 1	SCL input cycle time		t_{SCL}	10(12) × t_{IICcyc} + 80	—	ns	Figure 46.48
	SCL input high pulse width		t_{SCLH}	5(6) × t_{IICcyc}	—	ns	
	SCL input low pulse width		t_{SCLL}	5(6) × t_{IICcyc}	—	ns	
	SCL rise time	C_b = 400pF	t_{SrCL}	—	80	ns	
		C_b = 100pF		—	40		
	SDA rise time	C_b = 400pF	t_{SrDA}	—	160	ns	
		C_b = 100pF		—	80		
	SCL fall time	C_b = 400pF	t_{SfCL}	—	80	ns	
		C_b = 100pF		—	40		
	SDA fall time	C_b = 400pF	t_{SfDA}	—	160	ns	
		C_b = 100pF		—	80		
	SCL, SDA input spike pulse removal time		t_{SP}	0	1(1) × t_{IICcyc}	ns	
	Repeated START condition input setup time		t_{STAS}	40	—	ns	
	STOP condition input setup time		t_{STOS}	40	—	ns	
	Data input setup time		t_{SDAS}	10	—	ns	
	Data input hold time	C_b = 400pF	t_{SDAH}	0	150	ns	
		C_b = 100pF		0	70		
	SCL, SDA capacitive load		C_b*1	—	400	pF	

After correction

Table 46.32 IIC Timing (2)

Setting of the SCL0_A, SDA0_A pins are not required with the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
IIC (Hs-mode) BFCTL.HSME = 1	SCL input cycle time		t_{SCL}	10(12) × t_{IICcyc} + 80	—	—	ns	Figure 46.48
	SCL input high pulse width		t_{SCLH}	5(6) × t_{IICcyc}	—	—	ns	
	SCL input low pulse width		t_{SCLL}	5(6) × t_{IICcyc}	—	—	ns	
	SCL rise time	C_b = 400pF	t_{SrCL}	—	—	80	ns	
		C_b = 100pF		—	—	40		
	SDA rise time	C_b = 400pF	t_{SrDA}	—	—	160	ns	
		C_b = 100pF		—	—	80		
	SCL fall time	C_b = 400pF	t_{SfCL}	—	—	80	ns	
		C_b = 100pF		—	—	40		
	SDA fall time	C_b = 400pF	t_{SfDA}	—	—	160	ns	
		C_b = 100pF		—	—	80		
	SCL, SDA input spike pulse removal time		t_{SP}	0	—	1(1) × t_{IICcyc}	ns	
	START condition input hold time		t_{STAH}	t_{IICcyc} + 40	—	—	ns	
	Repeated START condition input setup time		t_{STAS}	40	—	—	ns	
	STOP condition input setup time		t_{STOS}	40	—	—	ns	
	Data input setup time		t_{SDAS}	10	—	—	ns	
	Data input hold time	C_b = 400pF	t_{SDAH}	0	—	150	ns	
		C_b = 100pF		0	—	70		
	SCL, SDA capacitive load		C_b*1	—	—	400	pF	
	SCL output minimum high pulse width	C_b = 400pF	t_{SCLH}	—	120	225	ns	
		C_b = 100pF		—	60	130		
	SCL output minimum low pulse width	C_b = 400pF	t_{SCLL}	—	—	320	ns	
		C_b = 100pF		—	—	160		