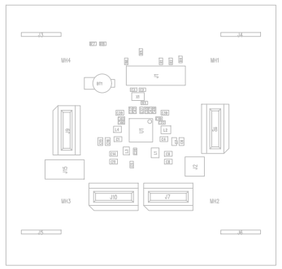
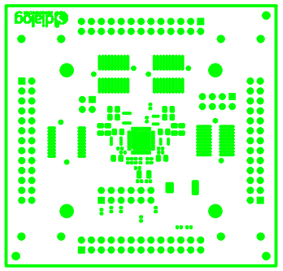


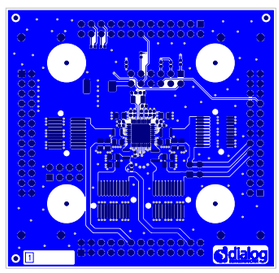
dialog SEMICONDUCTOR	PROJECT NUCLEUS-Perf. Board
DRAWING NUMBER	232-03-B- TA
LAYER	TOP ASSEMBLY DRAWING

dialog SEMICONDUCTOR	PROJECT NUCLEUS-Perf. Board
DRAWING NUMBER	232-03-B- TR
LAYER	TOP SOLDER RESIST

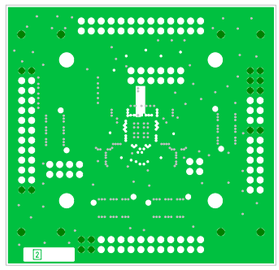


dialog SEMICONDUCTOR	PROJECT NUCLEUS-Perf. Board
DRAWING NUMBER	232-03-B-TP
LAYER	TOP SOLDER PASTE

dialog SEMICONDUCTOR	PROJECT NUCLEUS-Perf. Board
DRAWING NUMBER	232-03-B- TS
LAYER	TOP SILKSCREEN

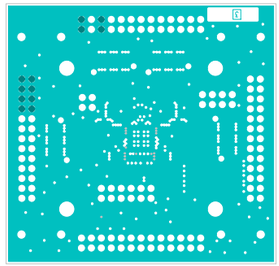


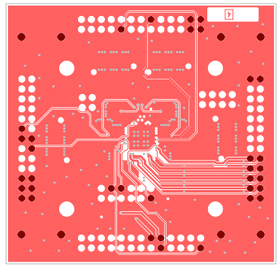
dialog SEMICONDUCTOR	PROJECT NUCLEUS-Perf. Board
DRAWING NUMBER	232-03-B-C1
LAYER	TOP SIDE TRACK



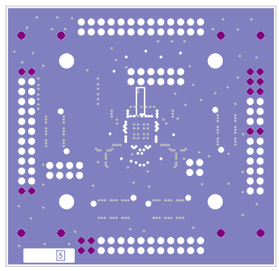
dialog SEMICONDUCTOR	PROJECT NUCLEUS-Perf. Board
DRAWING NUMBER	232-03-B- C2
LAYER	INNER LAYER 2

dialog SEMICONDUCTOR	PROJECT NUCLEUS-Perf. Board
DRAWING NUMBER	232-03-B- C3
LAYER	INNER LAYER 3



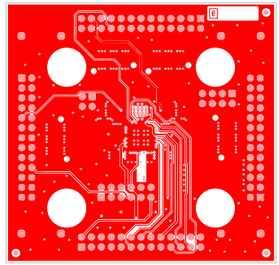


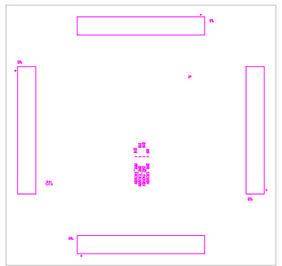
dialog SEMICONDUCTOR	PROJECT NUCLEUS-Perf. Board
DRAWING NUMBER	232-03-B- C4
LAYER	INNER LAYER 4



dialog SEMICONDUCTOR	PROJECT NUCLEUS-Perf. Board
DRAWING NUMBER	232-03-B- C5
LAYER	INNER LAYER 5

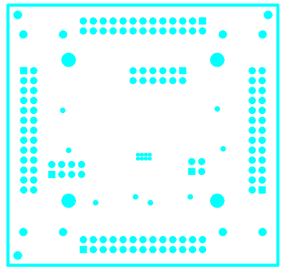
dialog SEMICONDUCTOR	PROJECT NUCLEUS-Perf. Board
DRAWING NUMBER	232-03-B-C6
LAYER	BOTTOM SIDE TRACK



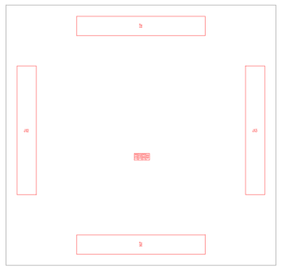


dialog SEMICONDUCTOR	PROJECT NUCLEUS-Perf. Board
DRAWING NUMBER	232-03-B-BS
LAYER	BOTTOM SILKSCREEN

dialog SEMICONDUCTOR	PROJECT NUCLEUS-Perf. Board
DRAWING NUMBER	232-03-B-BP
LAYER	BOTTOM SOLDER PASTE



dialog SEMICONDUCTOR	PROJECT NUCLEUS-Perf. Board
DRAWING NUMBER	232-03-B- BR
LAYER	BOTTOM SOLDER RESIST



dialog SEMICONDUCTOR	PROJECT NUCLEUS-Perf. Board
DRAWING NUMBER	232-03-B-BA
LAYER	BOTTOM ASSEMBLY DRAWING

1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11

IF IN DOUBT ASK!

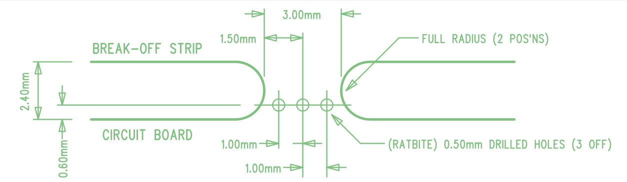
PREFERRED PANELISATION REQUIREMENTS

REFER TO THE PANEL DRAWING IF SUPPLIED OTHERWISE USE DETAILS BELOW

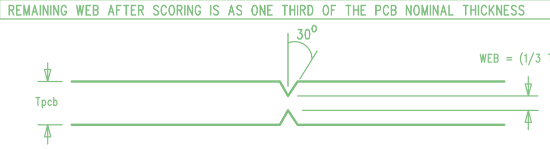
PRINTED CIRCUIT BOARDS THAT REQUIRE PANELISATION	
01	ANY PCB THAT DOES NOT HAVE A 5mm CLEARANCE FROM PCB EDGE TO COPPER/COMPONENTS ALONG THE LONGEST PARALLEL EDGES
02	ANY 'ODD' SHAPE PCB e.g. ROUND
PANEL SIZE, WASTE EDGE (BORDER) AND WEBBING	
01	ASSEMBLY PANEL TO BE A 2X2, 4 UP ARRAY
02	PANEL BORDER TO BE 10mm ON ALL SIDES, FULLY CROSS HATCHED IN COPPER ON BOTH SIDES
03	BOARD EDGE TO BOARD EDGE INTERNAL WEBBING TO BE 10mm
04	MAXIMUM PANEL SIZE NOT TO EXCEED 380mm X 440mm
TOOLING HOLES	
01	ADD 3 TOOLING HOLES 2.5mm +/-0.05 DIA. TO PANEL BORDER 5mm FROM BORDER EDGE
FIDUCIALS	
01	ADD 3 FIDUCIALS ON BOTH SIDES (1mm DIA./2mm DIA. CLEARANCE) 5mm FROM PANEL EDGE
BREAKOUTS (FOR REFERENCE SEE ROUTING DETAIL BELOW)	
01	ADD BREAKOUTS IN SAFE AREAS AWAY FROM TRACKS, TOOLING HOLES, SM PADS, VIAS, TEST PADS, GROUND PLANES, VITAL SILKSCREEN, THROUGH HOLES, OVERHANGING COMPONENTS ETC.
02	USE LOCATIONS SHOWN BY '**' IF PRESENT
03	AT LEAST TWO BREAKOUTS MUST BE ADDED ALONG THE EDGE OF A CIRCUIT IF GREATER THAN 75MM IN LENGTH
04	AT LEAST ONE BREAKOUT MUST BE ADDED ALONG THE EDGE OF A CIRCUIT IF LESS THAN 75MM IN LENGTH
05	THE SPACING BETWEEN BREAKOUTS SHOULD BE BETWEEN 40mm TO 50mm
06	BREAKOUTS TO BE POSITIONED AT LEAST 12MM FROM CIRCUIT CORNER TO ALLOW CUTOUT ACCESS
07	STEPPED GERBERS MUST BE SENT TO THE PCB DESIGNER FOR VERIFICATION BEFORE MANUFACTURE COMMENCES
08	IF ANY OF THIS SECTION CANNOT BE ADHERED TO THEN PLEASE CONSULT THE PCB DESIGNER

PREFERRED ROUTING / V-SCORING REQUIREMENTS

ROUTING	REQUIRED
01	USE A 2.40mm (+/-0.1mm) ROUT



V-SCORING	NOT REQUIRED
WHEN V-SCORING IS APPLIED TO THE BOARD AS A METHOD OF REMOVING THE BREAK-OFF STRIPS THE THE FOLLOWING RULES ARE TO BE APPLIED	
01	SOLDER MASK TO EDGE CLEARANCE = 0.50mm (20thou)
02	COPPER TO EDGE CLEARANCE (ON ALL LAYERS) = 1.00mm (40thou)
03	SCORE ANGLE = 30 deg
04	REMAINING WEB AFTER SCORING IS AS ONE THIRD OF THE PCB NOMINAL THICKNESS



NOTES

01	BOARD TO BE MANUFACTURED TO IPC-A-600 CLASS 2
02	BOARD IS TO MEET UL94V0 APPROVAL
03	ALL BOARD'S MUST BE 100% TESTED FOR ELECTRICAL CONTINUITY AND ISOLATION
04	NO REPAIRS MAY BE PERFORMED ON ANY IMPEDANCE CRITICAL TRACKS (WHERE APPLICABLE)
05	ALIGNMENT OF ALL LAYERS TO BE SUCH THAT NO BREAKOUT OCCURS
06	SUPPLIER'S UL IDENTIFICATION MARK, FLAMMABILITY RATING AND DATECODE MUST BE APPLIED TO THE BOARD - BOTTOM SIDE
07	VARIATION IN TRACK WIDTH AND GAP TO MEET IMPEDANCE REQUIREMENTS ARE PERMISSABLE, SO LONG AS THESE ARE MINIMAL, AND THE OVERALL BOARD THICKNESS IS NOT COMPROMISED.
08	MATERIAL- RoHS COMPLIANT HIGH Tg FR4 (VT47, TU768, 370HR, R1755V/1650V OR EQUIVALENT)
09	BOW AND TWIST TO BE NO GREATER THAN 0.75% ACROSS DIAGONALS
10	NON-FUNCTIONAL PADS MAY BE REMOVED FROM INTERNAL LAYERS (WHERE APPLICABLE)
11	ALL STUBS MAY BE REMOVED
12	SILKSCREEN SHOULD NOT BE ALTERED WITHOUT THE PCB DESIGNERS APPROVAL
13	CHECK BUILD ORDER AGAINST PLOTS
14	ALL DIMENSIONS IN mm (UNLESS STATED)

15	FINISHED BOARD THICKNESS	1.60mm +/-10%
16	SURFACE FINISH	ELECTROLESS NICKEL/IMMERSION GOLD
17	SOLDER RESIST	GREEN PHOTO-IMAGABLE
18	SILKSCREEN COLOUR	WHITE
19	MINIMUM TRACK WIDTH	0.20mm
20	MINIMUM GAP	0.15mm
21	MINIMUM P.T.H. PAD SIZE	0.4mm
22	MINIMUM PITCH OF SURFACE MOUNT PADS	0.50mm
23	No. TOP SIDE SURFACE MOUNT PADS	204
24	No. BOTTOM SIDE SURFACE MOUNT PADS	11

ADDITIONAL NOTES

25	VIAS UNDER U1 EXPOSED PAD NEED TO BE VIA PLUG TECHNOLOGY
26	.
27	.
28	.

PCB LAYER	MANUFACTURING DETAIL	GERBER FILES
	TOP SILKSCREEN	232-03-B_TS.GER
	TOP RESIST	232-03-B_TR.GER
LAYER 1	TOP SIDE TRACK	232-03-B_C1.GER
LAYER 2	INNER LAYER 2	232-03-B_C2.GER
LAYER 3	INNER LAYER 3	232-03-B_C3.GER
LAYER 4	INNER LAYER 4	232-03-B_C4.GER
LAYER 5	INNER LAYER 5	232-03-B_C5.GER
LAYER 6	BOTTOM SIDE TRACK	232-03-B_C6.GER
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	BOTTOM RESIST	232-03-B_BR.GER
	BOTTOM SILKSCREEN	232-03-B_BS.GER
	MANUFACTURE DETAIL	232-03-B_MC.GER
	.	.
	CNC DRILL FILE (PLATED/NON-PLATED THROUGH HOLE)	232-03-B.DRT
	CNC DRILL TOOLING (PLATED/NON-PLATED THR'H HOLE)	232-03-B.REP
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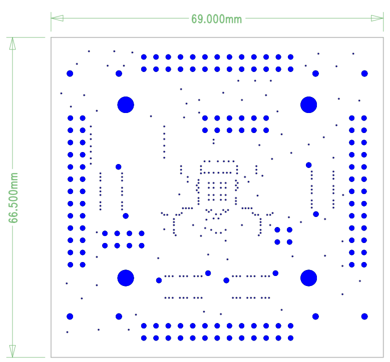
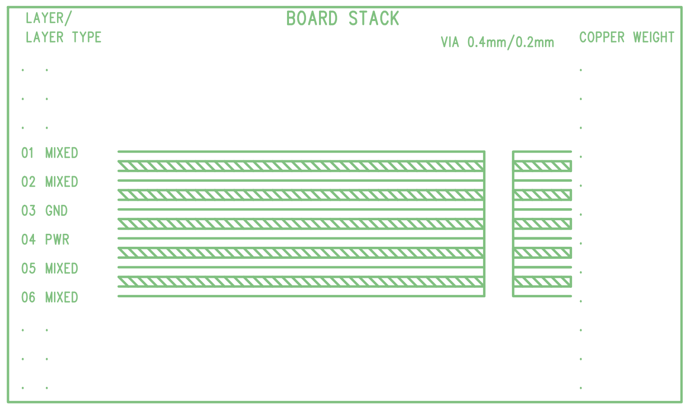
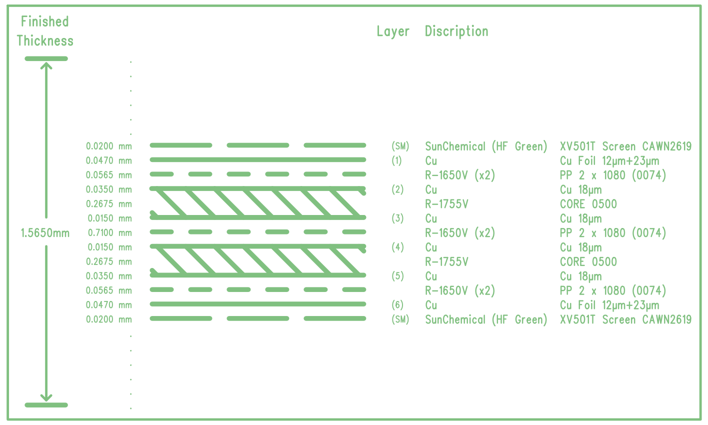


dialog SEMICONDUCTOR	PROJECT NUCLEUS-Perf. Board
DRAWING NUMBER	232-03-B- MC
LAYER	MANUFACTURE DETAIL

BOARD STACK





IMPEDANCE REQUIREMENTS (NO REQUIREMENT)

REQ NO	Zo	TOLERANCE	LAYERS	TRACE WIDTH	TRACE SEPARATION	PLANE SEPARATION	REFERENCE LAYERS	METHOD	TEST COUPON REQUIRED	SEE NOTES

A | B | C | D | E | F | G

Pb Free

COMPANY CONFIDENTIAL

DRILL DETAIL NOTES	
ALL PLATED HOLES ARE FINISHED SIZES WITH +/-0.075mm TOLERANCE	
ALL NON-PLATED HOLES ARE FINISHED SIZES WITH +/-0.050mm TOLERANCE	
ALL VIAS ARE DRILLED SIZES WITH +0/-DRILL TOLERANCE	
TOTAL PLATED HOLE QTY	148
TOTAL NON-PLATED HOLE QTY	12

TOLERANCES UNLESS OTHERWISE STATED
0 PLACE DECIMALS +/- 1
1 PLACE DECIMALS +/- 0.5
2 PLACE DECIMALS +/- 0.1

DRAWN BY	DATE
Daniel Ferreira .	15-12-2014
CHK'D BY	DATE
Klaus Handke	15-12-2014

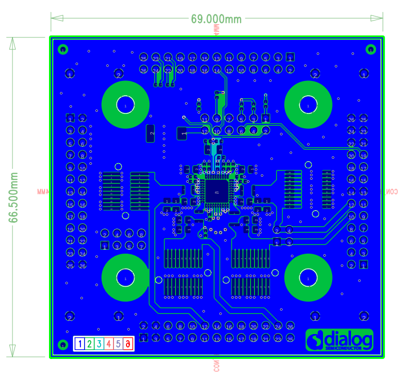
DIALOG SEMICONDUCTOR GmbH
Neue Straße 95
73230 Kirchheim Unter Teck (Nabern)
Deutschland

TITLE MANUFACTURE DETAIL
NUCLEUS Performance Board

DRAWING NUMBER
232-03-B

1	2	3	4	5	6	7	8	9	10	11

IF IN DOUBT ASK!



PROJECT	NUCLEUS-Perf. Board
DRAWING NUMBER	232-03-B- C1
LAYER	TOP SIDE TRACK

PREFERRED PANELISATION REQUIREMENTS

REFER TO THE PANEL DRAWING IF SUPPLIED OTHERWISE USE DETAILS BELOW

PRINTED CIRCUIT BOARDS THAT REQUIRE PANELISATION	
01	ANY PCB THAT DOES NOT HAVE A 5mm CLEARANCE FROM PCB EDGE TO COPPER/COMPONENTS ALONG THE LONGEST PARALLEL EDGES
02	ANY 'ODD' SHAPE PCB e.g. ROUND
PANEL SIZE, WASTE EDGE (BORDER) AND WEBBING	
01	ASSEMBLY PANEL TO BE A 2X2, 4 UP ARRAY
02	PANEL BORDER TO BE 10mm ON ALL SIDES, FULLY CROSS HATCHED IN COPPER ON BOTH SIDES
03	BOARD EDGE TO BOARD EDGE INTERNAL WEBBING TO BE 10mm
04	MAXIMUM PANEL SIZE NOT TO EXCEED 380mm X 440mm
TOOLING HOLES	
01	ADD 3 TOOLING HOLES 2.5mm +/-0.05 DIA. TO PANEL BORDER 5mm FROM BORDER EDGE
FIDUCIALS	
01	ADD 3 FIDUCIALS ON BOTH SIDES (1mm DIA./2mm DIA. CLEARANCE) 5mm FROM PANEL EDGE
BREAKOUTS (FOR REFERENCE SEE ROUTING DETAIL BELOW)	
01	ADD BREAKOUTS IN SAFE AREAS AWAY FROM TRACKS, TOOLING HOLES, SM PADS, VIAS, TEST PADS, GROUND PLANES, VITAL SILKSCREEN, THROUGH HOLES, OVERHANGING COMPONENTS ETC.
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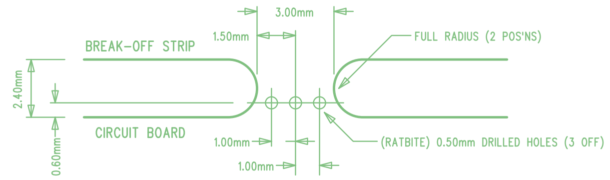
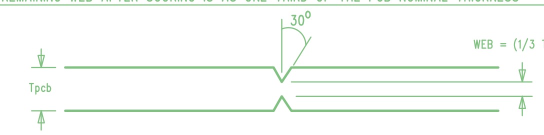
07	STEPPED GERBERS MUST BE SENT TO THE PCB DESIGNER FOR VERIFICATION BEFORE MANUFACTURE COMMENCES
08	IF ANY OF THIS SECTION CANNOT BE ADHERED TO THEN PLEASE CONSULT THE PCB DESIGNER

PREFERRED ROUTING / V-SCORING REQUIREMENTS

ROUTING	REQUIRED
01	USE A 2.40mm (+/-0.1mm) ROUT



V-SCORING	NOT REQUIRED
WHEN V-SCORING IS APPLIED TO THE BOARD AS A METHOD OF REMOVING THE BREAK-OFF STRIPS THE THE FOLLOWING RULES ARE TO BE APPLIED	
01	SOLDER MASK TO EDGE CLEARANCE = 0.50mm (20thou)
02	COPPER TO EDGE CLEARANCE (ON ALL LAYERS) = 1.00mm (40thou)
03	SCORE ANGLE = 30 deg
04	REMAINING WEB AFTER SCORING IS AS ONE THIRD OF THE PCB NOMINAL THICKNESS



NOTES

01	BOARD TO BE MANUFACTURED TO IPC-A-600 CLASS 2
02	BOARD IS TO MEET UL94V0 APPROVAL
03	ALL BOARD'S MUST BE 100% TESTED FOR ELECTRICAL CONTINUITY AND ISOLATION
04	NO REPAIRS MAY BE PERFORMED ON ANY IMPEDANCE CRITICAL TRACKS (WHERE APPLICABLE)
05	ALIGNMENT OF ALL LAYERS TO BE SUCH THAT NO BREAKOUT OCCURS
06	SUPPLIER'S UL IDENTIFICATION MARK, FLAMMABILITY RATING AND DATECODE MUST BE APPLIED TO THE BOARD - BOTTOM SIDE
07	VARIATION IN TRACK WIDTH AND GAP TO MEET IMPEDANCE REQUIREMENTS ARE PERMISSABLE, SO LONG AS THESE ARE MINIMAL, AND THE OVERALL BOARD THICKNESS IS NOT COMPROMISED.
08	MATERIAL- RoHS COMPLIANT HIGH Tg FR4 (VT47, TU768, 370HR, R1755V/1650V OR EQUIVALENT)
09	BOW AND TWIST TO BE NO GREATER THAN 0.75% ACROSS DIAGONALS
10	NON-FUNCTIONAL PADS MAY BE REMOVED FROM INTERNAL LAYERS (WHERE APPLICABLE)
11	ALL STUBS MAY BE REMOVED
12	SILKSCREEN SHOULD NOT BE ALTERED WITHOUT THE PCB DESIGNERS APPROVAL
13	CHECK BUILD ORDER AGAINST PLOTS
14	ALL DIMENSIONS IN mm (UNLESS STATED)

15	FINISHED BOARD THICKNESS	1.60mm +/-10%
16	SURFACE FINISH	ELECTROLESS NICKEL/IMMERSION GOLD
17	SOLDER RESIST	GREEN PHOTO-IMAGABLE
18	SILKSCREEN COLOUR	WHITE
19	MINIMUM TRACK WIDTH	0.20mm
20	MINIMUM GAP	0.15mm
21	MINIMUM P.T.H. PAD SIZE	0.4mm
22	MINIMUM PITCH OF SURFACE MOUNT PADS	0.50mm
23	No. TOP SIDE SURFACE MOUNT PADS	204
24	No. BOTTOM SIDE SURFACE MOUNT PADS	11

ADDITIONAL NOTES

25	VIAS UNDER U1 EXPOSED PAD NEED TO BE VIA PLUG TECHNOLOGY
26	.
27	.
28	.

PCB LAYER	MANUFACTURING DETAIL	GERBER FILES
	TOP SILKSCREEN	232-03-B_TS.GER
	TOP RESIST	232-03-B_TR.GER
LAYER 1	TOP SIDE TRACK	232-03-B_C1.GER
LAYER 2	INNER LAYER 2	232-03-B_C2.GER
LAYER 3	INNER LAYER 3	232-03-B_C3.GER
LAYER 4	INNER LAYER 4	232-03-B_C4.GER
LAYER 5	INNER LAYER 5	232-03-B_C5.GER
LAYER 6	BOTTOM SIDE TRACK	232-03-B_C6.GER
.	.	.
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	BOTTOM RESIST	232-03-B_BR.GER
	BOTTOM SILKSCREEN	232-03-B_BS.GER
	MANUFACTURE DETAIL	232-03-B_MC.GER
	.	.
	CNC DRILL FILE (PLATED/NON-PLATED THROUGH HOLE)	232-03-B.DRT
	CNC DRILL TOOLING (PLATED/NON-PLATED THR'H HOLE)	232-03-B.REP
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BOARD STACK

LAYER/ LAYER TYPE	VIA 0.4mm/0.2mm	COPPER WEIGHT
. .		.
. .		.
. .		.
01 MIXED		.
02 MIXED		.
03 GND		.
04 PWR		.
05 MIXED		.
06 MIXED		.
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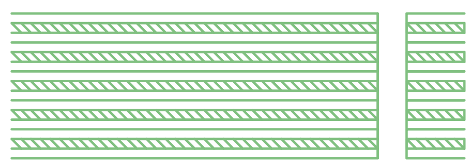
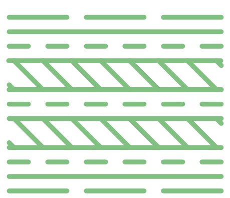


Finished Thickness: 1.5650mm



Thickness	Layer	Discription	
0.0200 mm	(SM)	SunChemical (HF Green)	XV501T Screen CAWN2619
0.0470 mm	(1)	Cu	Cu Foil 12µm+23µm
0.0565 mm		R-1650V (x2)	PP 2 x 1080 (0074)
0.0350 mm	(2)	Cu	Cu 18µm
0.2675 mm		R-1755V	CORE 0500
0.0150 mm	(3)	Cu	Cu 18µm
0.7100 mm		R-1650V (x2)	PP 2 x 1080 (0074)
0.0150 mm	(4)	Cu	Cu 18µm
0.2675 mm		R-1755V	CORE 0500
0.0350 mm	(5)	Cu	Cu 18µm
0.0565 mm		R-1650V (x2)	PP 2 x 1080 (0074)
0.0470 mm	(6)	Cu	Cu Foil 12µm+23µm
0.0200 mm	(SM)	SunChemical (HF Green)	XV501T Screen CAWN2619

IMPEDANCE REQUIREMENTS (NO REQUIREMENT)

REQ NO	Zo	TOLERANCE	LAYERS	TRACE WIDTH	TRACE SEPARATION	PLANE SEPARATION	REFERENCE LAYERS	METHOD	TEST COUPON REQUIRED	SEE NOTES

DRILL DETAIL NOTES	
ALL PLATED HOLES ARE FINISHED SIZES WITH +/-0.075mm TOLERANCE	
ALL NON-PLATED HOLES ARE FINISHED SIZES WITH +/-0.050mm TOLERANCE	
ALL VIAS ARE DRILLED SIZES WITH +0/-DRILL TOLERANCE	
TOTAL PLATED HOLE QTY	148
TOTAL NON-PLATED HOLE QTY	12

Pb Free

COMPANY CONFIDENTIAL

TOLERANCES UNLESS OTHERWISE STATED
0 PLACE DECIMALS +/- 1
1 PLACE DECIMALS +/- 0.5
2 PLACE DECIMALS +/- 0.1

DRAWN BY	DATE
Daniel Ferreira .	15-12-2014
CHK'D BY	DATE
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TITLE MANUFACTURE DETAIL
NUCLEUS Performance Board

DRAWING NUMBER 232-03-B

A	B	C	D	E	F	G