

# Smart Configurator for RL78 Plug-in in e<sup>2</sup> studio 2022-10

## Smart Configurator for RL78 V1.4.0

### Release Note

#### Introduction

Thank you for using the Smart Configurator for RL78.

This document describes the restrictions and points for caution. Read this document before using the product.

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## 1. Introduction

Smart Configurator is a utility for combining software to meet your needs. It supports the following three functions related to the embedding of Renesas drivers in your systems: importing middleware, generating driver code, and setting pins.

Smart Configurator for RL78 V1.4.0 is equivalent to Smart Configurator for RL78 plugin in e<sup>2</sup> studio 2022-10.

### 1.1 System requirements

The operating environment is as follows.

#### 1.1.1 PC

- System: x64/x86 based processor
  - Windows® 11
  - Windows® 10 (64-bit version)
  - Windows® 8.1 (64-bit version)
- Memory capacity: We recommend 4 GB or more
- Capacity of hard disk: At least 300 MB of free space.
- Display: Graphics resolution should be at least 1024 x 768, and the mode should display at least 65,536 colors.
- Processor: 1 GHz or higher (must support hyper-threading, multi-core CPUs)

#### 1.1.2 Development Environments

- Renesas Electronics Compiler for RL78 [CC-RL] V1.11 or later
- LLVM for Renesas RL78 10.0.0.202207 or later
- IAR Embedded Workbench for Renesas RL78 V4.21.3 or later
- SMS Assembler <sup>Note</sup> V1.00.00 or later

Note:

If you want to add SMS Assembler to e<sup>2</sup> studio, install it from the integrated installer of e<sup>2</sup> studio 21-04 or later. ([e<sup>2</sup> studio](#))

As with other compilers, select and install from the [Additional Software] - [Renesas Toolchains & Utilities] tab of the e<sup>2</sup> studio setup wizard.

## 2. Support List

### 2.1 Support Devices List

Below is a list of devices supported by the Smart Configurator for RL78 V1.4.0.

**Table 2-1 Support Devices**

Group (HW Manual number)	PIN	Device name
RL78/G23 Group (R01UH0896EJ0120)	30pin	R7F100GAFxSP, R7F100GAGxSP, R7F100GAHxSP, R7F100GAJxSP
	32pin	R7F100GBFxNP, R7F100GBGxNP, R7F100GBHxNP, R7F100GBJxNP, R7F100GBFxFP, R7F100GBGxFP, R7F100GBHxFP, R7F100GBJxFP
	36pin	R7F100GCFxLA, R7F100GCGxLA, R7F100GCHxLA, R7F100GCJxLA
	40pin	R7F100GEFxNP, R7F100GEGxNP, R7F100GEHxNP, R7F100GEJxNP
	44pin	R7F100GFFxFP, R7F100GFGxFP, R7F100GFHxFP, R7F100GFJxFP, R7F100GFKxFP, R7F100GFLxFP, R7F100GFNxFP
	48pin	R7F100GGFxFB, R7F100GGGxFB, R7F100GGHxFB, R7F100GGJxFB, R7F100GGKxFB, R7F100GGLxFB, R7F100GGNxFB, R7F100GGFxNP, R7F100GGGxNP, R7F100GGHxNP, R7F100GGJxNP, R7F100GGKxNP, R7F100GGLxNP, R7F100GGNxNP
	52pin	R7F100GJFxFA, R7F100GJGxFA, R7F100GJHxFA, R7F100GJJxFA, R7F100GJKxFA, R7F100GJLxFA, R7F100GJNxFA
	64pin	R7F100GLFxFA, R7F100GLGxFA, R7F100GLHxFA, R7F100GLJxFA, R7F100GLKxFA, R7F100GLLxFA, R7F100GLNxFA, R7F100GLFxFB, R7F100GLGxFB, R7F100GLHxFB, R7F100GLJxFB, R7F100GLKxFB, R7F100GLLxFB, R7F100GLNxFB, R7F100GLFxLA, R7F100GLGxLA, R7F100GLHxLA, R7F100GLJxLA, R7F100GLKxLA, R7F100GLLxLA, R7F100GLNxLA
	80pin	R7F100GMGxFA, R7F100GMHxFA, R7F100GMJxFA, R7F100GMKxFA, R7F100GMLxFA, R7F100GMNxFA, R7F100GMGxFB, R7F100GMHxFB, R7F100GMJxFB, R7F100GMKxFB, R7F100GMLxFB, R7F100GMNxFB
	100pin	R7F100GPGxFB, R7F100GPHxFB, R7F100GPJxFB, R7F100GPKxFB, R7F100GPLxFB, R7F100GPNxFB, R7F100GPGxFA, R7F100GPHxFA, R7F100GPJxFA, R7F100GPKxFA, R7F100GPLxFA, R7F100GPNxFA
	128pin	R7F100GSJxFB, R7F100GSKxFB, R7F100GSLxFB, R7F100GSNxFB
RL78/F24 Group (R01UH0944EJ0050)	32pin	R7F124FBJ3xNP, R7F124FBJ4xNP, R7F124FBJ5xNP
	48pin	R7F124FGJ3xFB, R7F124FGJ4xFB, R7F124FGJ5xFB
	64pin	R7F124FLJ3xFB, R7F124FLJ4xFB, R7F124FLJ5xFB
	80pin	R7F124FMJ3xFB, R7F124FMJ4xFB, R7F124FMJ5xFB
	100pin	R7F124FPJ3xFB, R7F124FPJ4xFB, R7F124FPJ5xFB
RL78/G15 Group (R01UH0959EJ0100)	8pin	R5F12008xNS, R5F12007xNS
	10pin	R5F12018xSP, R5F12017xSP
	16pin	R5F12048xNA, R5F12047xNA, R5F12048xSP, R5F12047xSP
	20pin	R5F12068xSP, R5F12067xSP

## 2.2 Support Components List

Below is a list of Components supported by the Smart Configurator for RL78 V1.4.0.

**Table 2-2 Support Components (1/2)**

✓: Support, -: Non-support

No	Components	Mode	RL78/G23	RL78/F24	RL78/G15	Remarks
1	12 Bit A/D Single Scan	-	-	✓	-	
2	12 Bit A/D Continuous Scan	-	-	✓	-	
3	12 Bit A/D Group Scan	-	-	✓	-	
4	A/D Converter	Normal mode	✓	-	✓	
5	Clock Output/Buzzer Output Controller	-	✓	✓	✓	
6	Comparator	-	✓	✓	✓	
7	D/A Converter	-	✓	✓	-	
8	Data Transfer Controller	-	✓	✓	-	
9	Delay Counter	-	✓	✓	✓	
10	Divider Function	-	✓	✓	✓	
11	Event Link Controller	-	-	✓	-	
12	External Event Counter	-	✓	✓	✓	
13	IIC Communication (Master mode)	-	✓	✓	✓	
14	IIC Communication (Slave mode)	-	✓	✓	✓	
15	Input Capture Function	-	-	✓	-	
16	Input Pulse Interval/Period Measurement	-	✓	✓	✓	
17	Input Signal High-/Low-Level Width Measurement	-	✓	✓	✓	
18	Interrupt Controller	-	✓	✓	✓	
19	Interval Timer	8 bit count mode	✓	✓	✓	
		12 bit count mode	-	-	✓	
		16 bit count mode	✓	✓	✓	
		16 bit capture mode	✓	-	-	
		32 bit count mode	✓	-	-	
20	Key Interrupt	-	✓	✓	-	
21	One-Shot Pulse Output	One-Shot Pulse Output	✓	✓	✓	
		Two-Channel Input with One-Shot Pulse Output	-	-	✓	
22	Output Compare Function	-	-	✓	-	
23	Ports	-	✓	✓	✓	

Table 2-3 Support Components (2/2)

✓ : Support, -: Non-support

No	Components	Mode	RL78/G23	RL78/F24	RL78/G15	Remarks
24	PWM Option Unit A	-	-	✓	-	
25	PWM Output	PWM mode	✓	✓	✓	
		PWM3 mode	-	✓	-	
		Extended PWM mode	-	✓	-	
26	Real-Time Clock	-	✓	✓	-	
27	Remote Control Signal Receiver	-	✓	-	-	
28	SNOOZE Mode Sequencer	-	✓	-	-	
29	SPI (CSI) Communication	Transmission	✓	✓	✓	
		Reception	✓	✓	✓	
		Transmission/reception	✓	✓	✓	
30	Square Wave Output	-	✓	✓	✓	
31	Three-phase PWM Output	Reset Synchronous PWM Mode	-	✓	-	
		Complementary PWM Mode	-	✓	-	
		Extended Complementary PWM Mode	-	✓	-	
32	UART Communication	Transmission	✓	✓	✓	
		Reception	✓	✓	✓	
		Transmission/reception	✓	✓	✓	
33	Voltage Detector	-	✓	✓	-	
34	Watchdog Timer	-	✓	✓	✓	
35	Logic & Event Link Controller	-	✓	-	-	Need download in Smart Configurator RL78

## 2.3 New support

### 2.3.1 Support RL78/G15 devices

See 2.1 Support Devices List for details on supported packages.

### 2.3.2 BSP (Board Support Package) revision update

BSP rev1.30 is supported and will be added as default BSP when creating Smart Configurator project.

### 2.3.3 Output only initialization API feature has been improved for individual configuration

From Smart Configurator for RL78 V1.4.0, output only initialization API feature can be applied for individual configuration (Code Generator component). You can right-click the selected component and select the "Output only initialization API" from the context menu.

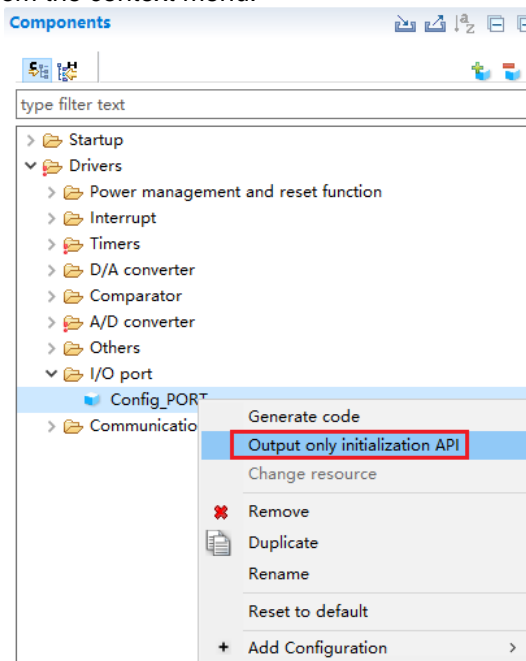


Figure 2-1 Context menu "Output only initialization API" for each configuration

### 2.3.4 Output files for IAR Embedded workbench of standalone version Smart Configurator

From Smart Configurator for RL78 V1.4.0, IAR Embedded workbench files (.ewp, .ewd, .eww), main.c and buildinfo.ipcf files can be generated after first clicking the "Generate Code" button. User no longer need to create these files manually.

### 2.3.5 Support raw (HEX) codes generation for components

From Smart Configurator for RL78 V1.4.0, a “Preferences” option is provided to allow users select “API code style”, which determines whether macro description or HEX value to be generated. By default, the “Value with macro description” is chosen which will generate macro description code as previous Smart Configurator versions. If user choose “Value without macro description (raw Hex)”, raw hex value can be generated instead of macro description.

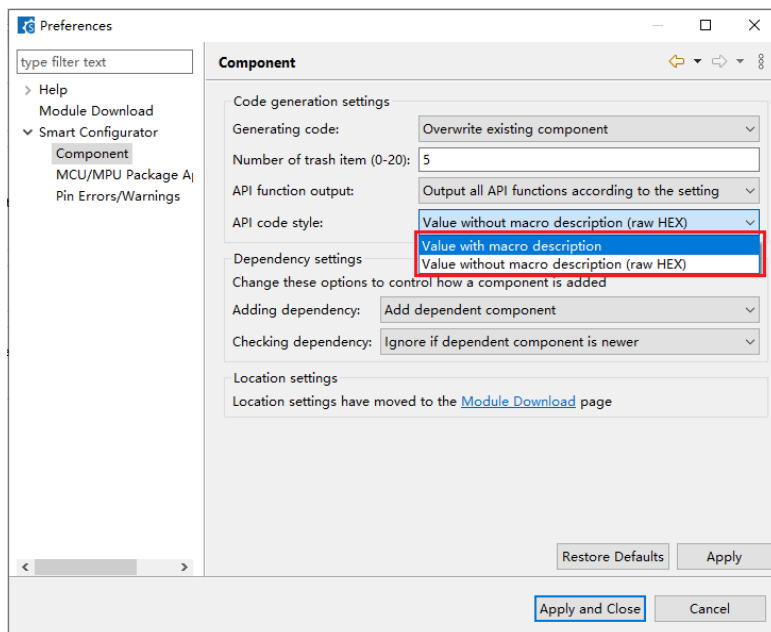


Figure 2-2 API code style setting

```
void R_Config_ADC_Create(void)
{
    ...
    ADM0 = 0x00U;
    ADM1 = 0x00U;
    ADM2 = 0x00U;
    ADUL = 0xFFU;
    ADLL = 0x00U;
    ADS = 0x00U;
    ADM2 = 0x3FU; /* clear ADREFP1 and ADREFP0 */
    ADM2 = 0x00U; /* set the reference voltage */
    ...
}
```

Figure 2-3 Code style of value without macro description



### 3. Changes

This chapter describes changes to the Smart Configurator for RL78 V1.4.0.

#### 3.1 Correction of issues/limitations

**Table 3-1 List of Correction of issues/limitations**

✓: Applicable, -: Not Applicable

No	Description	RL78/G23	RL78/F24	RL78/G15	Remarks
1	Fixed the issue of the unit selection when using “Event input from ELC” clock source in Timer RJ interval timer function	-	✓	-	
2	Fixed the issue of redundant local variables in ELCL generation code	✓	-	-	

##### 3.1.1 Fixed the issue of the unit selection when using “Event input from ELC” clock source in Timer RJ interval timer function

When using Timer RJ interval timer function and selecting “Clock source” as “Event input from ELC”, only “count” can be selected as the “Timer value” unit. Other unit options, such as ms, us, ns, have been removed from Smart Configurator for RL78 V1.4.0.

The screenshot shows two configuration sections. The first section, 'Clock source setting', has a 'Clock source' dropdown menu set to 'Event input from ELC' with a '(Please set ELC)' note. The second section, 'Timer value setting', has a 'Timer value' input field containing '100' and a dropdown menu set to 'count'. The 'count' option in the dropdown is highlighted with a red box, and a note '(Actual value: 100)' is visible to the right.

**Figure 3-1 The unit when selecting “Event input from ELC”**

##### 3.1.2 Fixed the issue of redundant local variables in ELCL generation code

In the Create () function of following ELCL components, redundant code is generated via local variables assignment when setting a value to a register.

- ELCL edge detection thinning function
- ELCL chattering prevention
- ELCL manchester decoder
- ELCL multiple parameter monitor
- ELCL AND
- ELCL D flip flop
- ELCL EXOR
- ELCL selector
- ELCL Through

These local variables are deleted from Smart Configurator for RL78 V1.4.0.

## 3.2 Specification changes

**Table 3-2 List of Specification changes**

✓ : Applicable, - : Not Applicable

No	Description	RL78/G23	RL78/F24	RL78/G15	Remarks
1	Improvement for the specification according to RL78/G23 User's Manual Hardware V1.20	✓	-	-	
2	Improvement for input signal selection of TAU input pulse interval/period measurement function	✓	-	-	
3	Improvement for IICA slave interrupt handle code	✓	✓	✓	
4	Improvement for adding "fHOCO start setting" on Clock page	✓	-	-	
5	Improvement for clearing error detected flag in RLIN3 UART error interrupt	-	✓	-	
6	Improvement for user can manually enable/disable Timer RD forced output function	-	✓	-	
7	Removing "Stop bit length setting" from UARTA reception mode	✓	-	-	
8	Improvement for "Input buffer OFF" specification in PORT	✓	-	-	
9	Improvement for the interrupt code when using ITL capture function	✓	-	-	
10	Improvement for migration DTC "Activation source" when changing device	✓	✓	-	

### 3.2.1 Improvement for the specification according to RL78/G23 User's Manual Hardware V1.20

Improved the specification according to RL78/G23 User's Manual Hardware V1.10 and V1.20. Please refer to chapter "REVISION HISTORY" in each User's Manual Hardware for detail.

### 3.2.2 Improvement for input signal selection of TAU input pulse interval/period measurement function

The period of input signals should be more than  $1/fMCK+10ns$ . fIMP, fSUB and fIL can't be selected as input source when fCLK is selected fSUB or fIL. If user selects fIMP, fSUB or fIL at this time, it can't measure interval/period exactly and an error icon will display to prevent the user from selecting the period of input signals less than  $1/fMCK+10ns$ .

### 3.2.3 Improvement for IICA slave interrupt handle code

IICA slave interrupt handler (`r_{Config_IICAn}_slave_handler()`) code isn't readable for user and can't support abnormal case when master sends data count is more than slave receives data count. So, it was improved from Smart Configurator for RL78 V1.4.0.

### 3.2.4 Improvement for adding “fHOCO start setting” on Clock page

From Smart Configurator for RL78 V1.4.0, BSP API can't set the starting of high-speed on-chip oscillator at the times of release from STOP mode and of transitions to SNOOZE mode any longer. The related setting is moved to Smart Configurator [Clock] page. In generation code, BSP\_CFG\_WAKEUP\_MODE value will be changed according to “fHOCO start setting”.

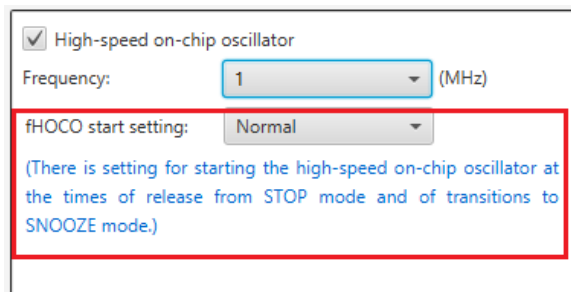


Figure 3-2 “fHOCO start setting” in [Clock] page

### 3.2.5 Improvement for clearing error detected flag in RLIN3 UART error interrupt

The error detected flag (LESTn.BER bit) is cleared in Smart Configurator generation code, so that user do not need to add code to clear it manually.

In Config\_RLIN3n\_user.c

```
void r_Config_RLIN30_interrupt_error(void)
{
    ...
    LEST0 &= (uint8_t) ~(_7D_RLIN3_CLEAR_ERROR_FLAG);
    ...
}
```

### 3.2.6 Improvement for user can manually enable/disable Timer RD forced output function

The following 2 APIs are generated in r\_cg\_trd\_common.c file.

- void R\_TRD\_ForcedOutput\_Enable (void)
- void R\_TRD\_ForcedOutput\_Disable (void)

By calling these APIs, user can enable or disable Timer RD forced output function manually.

### 3.2.7 Removing “Stop bit length setting” from UARTA reception mode

UARTA reception mode is always handled as including 1 stop bit. So, “Stop bit length setting” on GUI is useless and was removed.



Figure 3-3 Remove “Stop bit length setting”

### 3.2.8 Improvement for “Input buffer OFF” specification in PORT

For easily usage and understanding, the “Input buffer OFF” GUI is improved:

- Add “Input buffer OFF” option for P137.
- Add message on top of Port page (which has ‘Input buffer OFF’ function) to guide users how to use “Input buffer OFF” function.

### 3.2.9 Improvement for the interrupt code when using ITL capture function

The ITF00 bit should be cleared before the capture trigger is input. The interrupt code is updated to clear it. So, user needn't to add code to clear it manually.

In r\_cg\_itl\_common\_user.c

```
static void __near r_itl_interrupt(void)
{
    if (_10_ITL_CAPTURE_COMPLETE_DETECTE == (ITLS0 &
        _10_ITL_CAPTURE_COMPLETE_DETECTE))
    {
        ITLS0 &= (uint8_t)~_10_ITL_CAPTURE_COMPLETE_DETECTE;
        R_ITL000_ITL0011_capture_Callback_Shared_Interrupt();
    }

    ITLS0 &= (uint8_t)~_01_ITL_CHANNEL0_COUNT_MATCH_DETECTE;    <- Add it
}
```

### 3.2.10 Improvement for migration DTC “Activation source” when changing device

Some “Activation source” can't be portable correctly when changing device. For example, “Activation source (DTCD0)” selects “Comparator detection 0” in RL78/G23 project. Then changing device to RL78/F24, the “Activation source (DTCD0)” changes to “INTP0” although RL78/F24 supports “Comparator detection 0”. This issue is checked and improved from Smart Configurator for RL78 V1.4.0

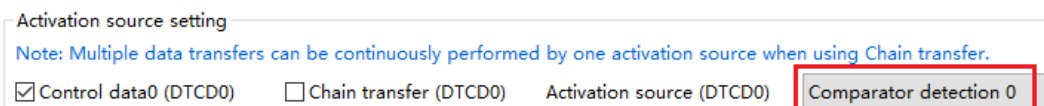


Figure 3-4 The activation source selects “Comparator detection 0” in RL78/G23 project

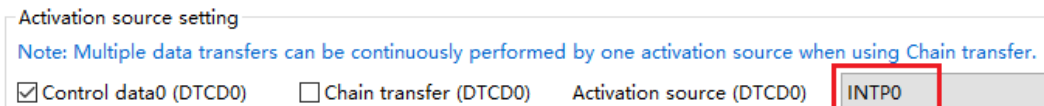


Figure 3-5 The activation source changes to “INTP0” after changing device to RL78/F24

#### 4. List of RENESAS TOOL NEWS AND TECHNICAL UPDATE

Below is a list of notifications delivered by RENESAS TOOL NEWS and TECHNICAL UPDATE.

Issue date	Document No.	Description	Applicable MCUs	Fixed version
Oct. 01, 2021	R20TS0757	1. Notes on creating LLVM for Renesas RL78 C/C++ Executable Project 2. Notes on using Port Input buffer function <a href="https://www.renesas.com/document/tnn/notes-e-studio-smart-configurator-plug-smart-configurator-rl78">https://www.renesas.com/document/tnn/notes-e-studio-smart-configurator-plug-smart-configurator-rl78</a>	RL78/G23	V1.2.0
Mar. 16, 2022	R20TS0822	1. Notes when build or clean e <sup>2</sup> studio Smart Configurator project <a href="https://www.renesas.com/document/tnn/notes-e-studio-smart-configurator-plug-smart-configurator-rl78-0">https://www.renesas.com/document/tnn/notes-e-studio-smart-configurator-plug-smart-configurator-rl78-0</a>	RL78/G23	V1.3.0

## 5. Points for Limitation

This section describes points for limitation regarding the Smart Configurator for RL78 V1.4.0.

### 5.1 List of Limitation

**Table 5-1 List of Limitation**

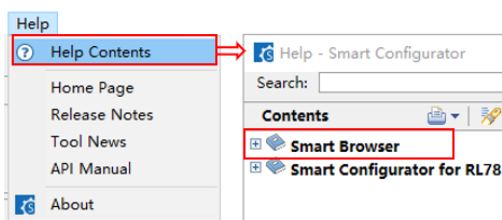
✓: Applicable, -: Not Applicable

No	Description	RL78/G23	RL78/F24	RL78/G15	Remarks
1	Note on extra help document issue	✓	✓	✓	
2	Note on ELCL D flip flop component GUI warning display incorrectly	✓	-	-	
3	Note on the unsupported setting items for some ELCL components	✓	-	-	
4	Note on UARTA reception error interrupt generation	✓	-	-	
5	Note on ROM overflow build error for LLVM project without any component added	-	-	✓	

### 5.2 Details of Limitation

#### 5.2.1 Note on extra help document issue

For Smart Configurator, there is an extra help "Smart Browser" under "[Help] > [Help Contents]". Please ignore it.



**Figure 5-1 Extra help issue**

### 5.2.2 Note on ELCL D flip flop component GUI warning display incorrectly

When selecting the event signal in ELCL D flip flop component, even if the selected signal consist with the hardware specification, there still displays the warning on the GUI.

[Avoidance measure]

Make reference to the hardware manual and set the selectable event signal though warning appeared in GUI, the waring is no impact for the code generation.

The following is example of using flip-flop 0 and flip-flop 1 in ELCL logic cell block L1.

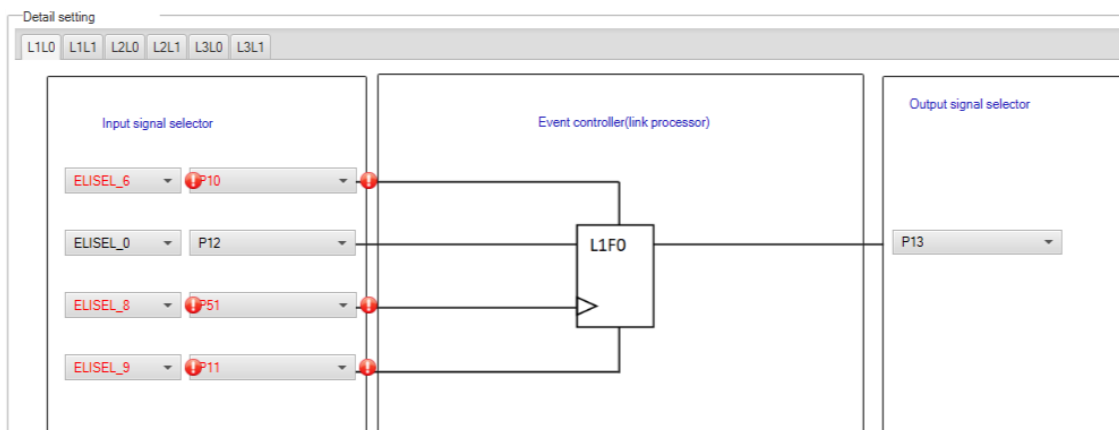


Figure 5-2 The flip-flop 0 in ELCL logic cell block L1 usage example

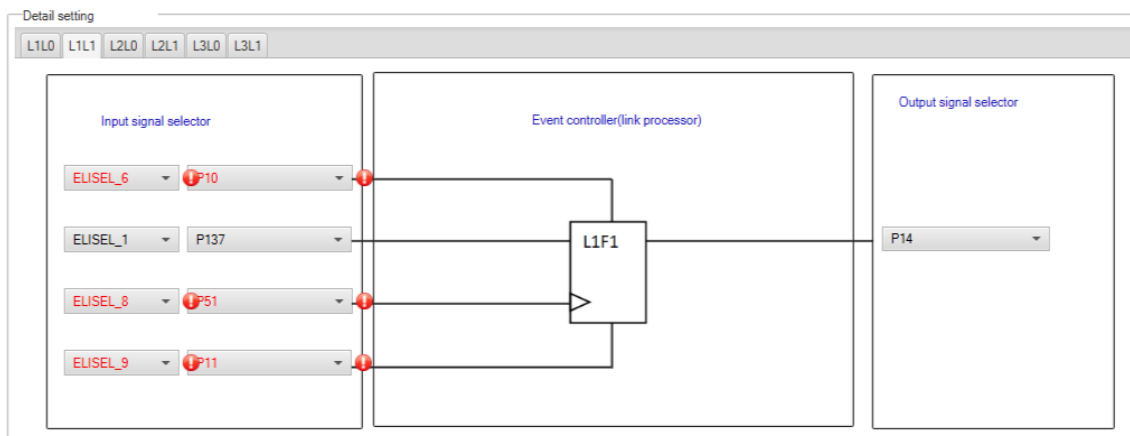


Figure 5-3 The flip-flop 1 in ELCL logic cell block L1 usage example

### 5.2.3 Note on the unsupported setting items for some ELCL components

In the following ELCL modules, it is not possible to set "no selection (fixed to 0)" as the input signal of the logic cell block and "negative logic output (inverted)" as the output level of the event signal.

- ELCL AND
- ELCL D flip flop
- ELCL EXOR
- ELCL selector
- ELCL Through

[Avoidance measure] None

### 5.2.4 Note on UARTA reception error interrupt generation

Smart Configuration generation code only supports to handle INTUREn (n = 0, 1) interrupt when a reception error occurs. Even if you select "INTUR interrupt occurs", the generation code still only handle INTUREn (n = 0, 1) interrupt. So please make sure to select "INTURE interrupt occurs" and ignore "INTUR interrupt occurs" selection on GUI.

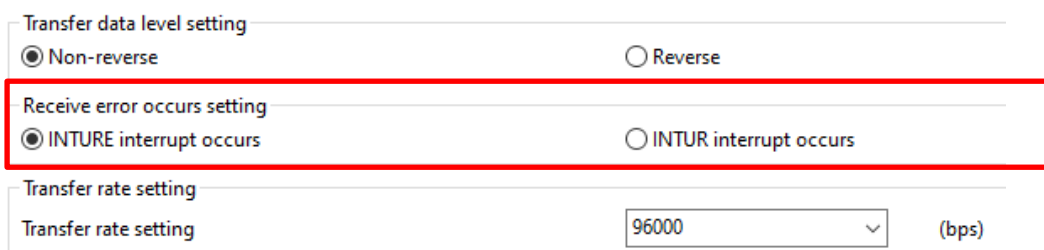


Figure 5-4 Ignore "INTUR interrupt occurs" selection

### 5.2.5 Note on ROM overflow build error for LLVM project without any component added

In case of a LLVM project without adding any component has ROM overflow build error, the cause is the BSP size is too large. So please consider disabling some BSP API function to reduce the BSP code size.

Property	Value
Configurations	
# Start up select	Enable (use BSP startup)
# Control of invalid memory access detection	Disable
# RAM guard space(GRAM0-1)	Disabled
# Guard of control registers of port function(GPORT)	Disabled
# Guard of registers of interrupt function(GINT)	Disabled
# Guard of control registers of clock control function, voltage detector, and RAM parity error detection function(GCSC)	Disabled
# Data flash access control(DFLEN)	Disables
# Initialization of peripheral functions by Code Generator/Smart Configurator	Enable
# API functions disable(R_BSP_StartClock, R_BSP_StopClock)	Disable
# API functions disable(R_BSP_GetFclkFreqHz)	Disable
# API functions disable(R_BSP_SetClockSource)	Disable
# API functions disable(R_BSP_ChangeClockSetting)	Disable
# API functions disable(R_BSP_SoftwareDelay)	Disable
# Parameter check enable	Enable

Figure 5-5 BSP API functions can be disabled



## 6. Points for Caution

This section describes points for caution regarding the Smart Configurator for RL78 V1.4.0.

### 6.1 List of Caution

Table 6-1 List of Caution

✓ : Applicable, - : Not Applicable

No	Description	RL78/G23	RL78/F24	RL78/G15	Remarks
1	Note on the build error message such as "section .bss virtual address range overlaps with .dsc_vectortable"	✓	✓	-	
2	Note on the installation of the Smart Configurator	✓	✓	✓	
3	Note on using TRDIOA0 for Input capture and TRDIOB0 for Output compare at same time	-	✓	-	
4	Note on pulse width calculation of Timer RD input capture function	-	✓	-	
5	Note on using Touch middleware and UART communication components	✓	-	-	
6	Note on running R_Config_RTC_Set_CounterValue() always returns MD_BUSY1	✓	✓	-	
7	Note on the include path update issue when renaming the component's configuration name	✓	✓	✓	

## 6.2 Details of Caution

### 6.2.1 Note on the build error message such as “section .bss virtual address range overlaps with .dtc\_vectortable”

When user use many components and DTC component together, the generated code build might fail due to some section address overlaps.

```

CDT Build Console [LLVM_R7F100GCJxLA_case1]
ld.lld: error: section .bss virtual address range overlaps with .dtc_vectortable
>>> .bss range is [0xF9F00, 0xF9F31]
>>> .dtc_vectortable range is [0xF9F00, 0xF9F27]

ld.lld: error: section .bssf virtual address range overlaps with .dtc_controldata_0
>>> .bssf range is [0xF9F32, 0xF9F7F]
>>> .dtc_controldata_0 range is [0xF9F40, 0xF9F47]

ld.lld: error: section .bss load address range overlaps with .dtc_vectortable
>>> .bss range is [0xF9F00, 0xF9F31]
>>> .dtc_vectortable range is [0xF9F00, 0xF9F27]

ld.lld: error: section .bssf load address range overlaps with .dtc_controldata_0
>>> .bssf range is [0xF9F32, 0xF9F7F]
>>> .dtc_controldata_0 range is [0xF9F40, 0xF9F47]
clang: error: ld.lld command failed with exit code 1 (use -v to see invocation)
makefile:110: recipe for target 'LLVM_R7F100GCJxLA_case1.elf' failed
make: *** [LLVM_R7F100GCJxLA_case1.elf] Error 1
'make -j8 all' terminated with exit code 2. Build might be incomplete.

18:09:07 Build Failed. 2 errors, 0 warnings. (took 1s.846ms)

```

Figure 6-1 Build error message

#### [Workaround]

The Smart Configurator cannot set “.bss” and “.bssf” section address. So user should consider to modify “.bss” and “.bssf” section address manually in “linker\_script.ld” file or change the DTC base address to avoid such section overlap error.

**Configure**

Base setting

DTC base address

Figure 6-2 DTC base address setting

## 6.2.2 Note on the installation of the Smart Configurator

Do not set more than 64 characters for the installation directory.

You might see an error message "The specified path is too long" and will not be able to install Smart Configurator.

## 6.2.3 Note on using TRDIOA0 for Input capture and TRDIOB0 for Output compare at same time

If user sets up TRDIOA0 for Input capture and TRDIOB0 for Output compare at the same time. Smart Configurator will output a Peripheral conflict error.

User can ignore this Smart Configurator error message and use these two functions at the same time.

## 6.2.4 Note on pulse width calculation of Timer RD input capture function

The pulse width calculation code is with the assumption that the counter is not cleared between two interrupts occurrence, except the input pulse width which is selected as counter clear trigger on GUI.

For example, when "Clear by TRDGRA0 input capture" is selected, only TRDIOA0 pulse width calculation handle counter clear, other input pulse width calculation doesn't handle counter clear.

Counter setting

Counter clear Clear by TRDGRA0 input capture

```

static void __near r_Config_TRD0_trd0_interrupt(void)
{
    uint16_t tmr_d_pul_a_cur = TRDGRA0;
    uint16_t tmr_d_pul_b_cur = TRDGRB0;
    uint16_t tmr_d_pul_c_cur = TRDGRD0;
    uint16_t tmr_d_pul_d_cur = TRDGRD0;
    uint8_t trdier0_temp = TRDIER0;

    TRDIER0 = 0x00U;

    /* overflow process */
    if ((TRDSR0 & _10_TRD_INTOV_GENERATE_FLAG) == _10_TRD_INTOV_GENERATE_FLAG)
    {
        TRDSR0 &= (uint8_t)~_10_TRD_INTOV_GENERATE_FLAG;
        g_tmr_d_ovf_a += 10;
        g_tmr_d_ovf_b += 10;
        g_tmr_d_ovf_c += 10;
        g_tmr_d_ovf_d += 10;
    }

    /* TRDGRA0 input capture interrupt */
    if ((TRDSR0 & _01_TRD_INTA_GENERATE_FLAG) == _01_TRD_INTA_GENERATE_FLAG)
    {
        TRDSR0 &= (uint8_t)~_01_TRD_INTA_GENERATE_FLAG;
        if (OU == g_tmr_d_ovf_a)
        {
            g_tmr_d_active_width_a = (uint32_t)tmr_d_pul_a_cur;
        }
        else
        {
            g_tmr_d_active_width_a = (uint32_t)((0x10000UL * (uint32_t)g_tmr_d_ovf_a) + (uint32_t)tmr_d_pul_a_cur);
            g_tmr_d_ovf_a = 0U;
        }
        g_tmr_d_inactive_width_a = 0UL;
    }

    /* TRDGRB0 input capture interrupt */
    if ((TRDSR0 & _02_TRD_INTB_GENERATE_FLAG) == _02_TRD_INTB_GENERATE_FLAG)
    {
        TRDSR0 &= (uint8_t)~_02_TRD_INTB_GENERATE_FLAG;
        if (OU == g_tmr_d_ovf_b)
        {
            g_tmr_d_active_width_b = (uint32_t)((uint32_t)tmr_d_pul_b_cur - (uint32_t)g_tmr_d_trdgrb_old);
        }
        else
        {
            g_tmr_d_active_width_b = (uint32_t)((0x10000UL * (uint32_t)g_tmr_d_ovf_b) + (uint32_t)tmr_d_pul_b_cur) - (uint32_t)g_tmr_d_trdgrb_old;
            g_tmr_d_ovf_b = 0U;
        }
        g_tmr_d_inactive_width_b = 0UL;
        g_tmr_d_trdgrb_old = tmr_d_pul_b_cur;
    }
}

```

The pulse width calculation handle counter clear.

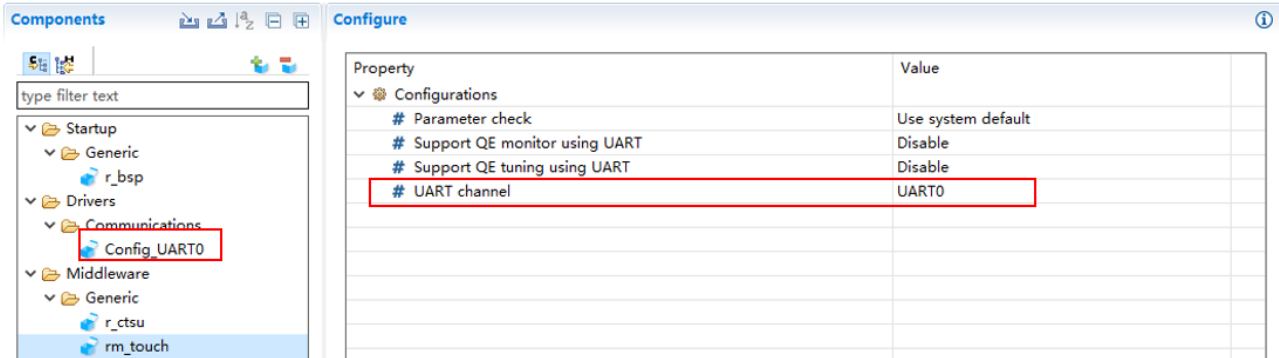
The pulse width calculation doesn't handle counter clear.

Figure 6-3 Counter clear setting in Input capture function

**6.2.5 Note on using Touch middleware and UART communication components**

When use Touch middleware, please do not change the name of UART components. Otherwise, due the file name mismatch will bring build error.

For example, in touch middleware select UART0 as UART channel, for UART0 component please use Config\_UART0.



**Figure 6-4 Touch middleware and UART communication components**

**6.2.6 Note on R\_Config\_RTC\_Set\_CounterValue() returns MD\_BUSY1**

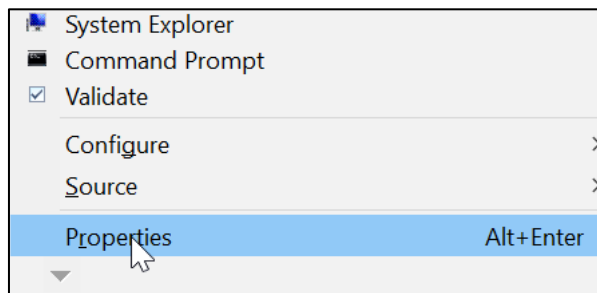
If this case happens, it means the wait time is not enough. As a workaround, user should manually modify the macro "RTC\_WAITTIME\_2CYCLE" value to a larger one in "Config\_RTC.h" file.

```

/*****
Macro definitions
*****/
...
#define RTC_WAITTIME_2CYCLE                (163U)
    
```

Note:

- 1) If code is generated again, the previous value will be restored. Modification is necessary each time after performing code generation.
- 2) Please use the following procedure to disable code re-generation when building project in e<sup>2</sup> studio. Otherwise, the previous value will be restored when the project build.
  - Right click the project on the project tree and click "Properties" from the popup menu.



**Figure 6-5 To open the properties window**

- Choose the “Builders” item on the left of the property window, then select the “SC Code Generation Builder” on the right, click “Edit...” button

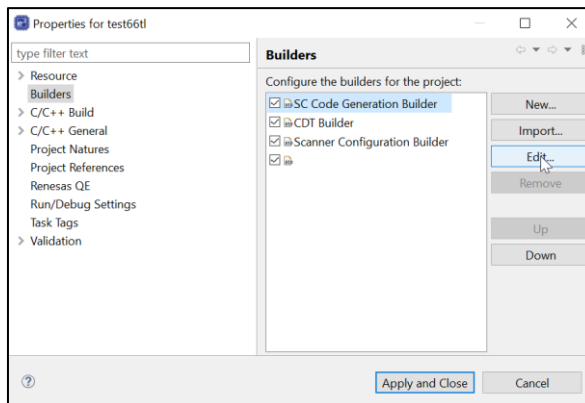


Figure 6-6 Builder configure window

- Deselect all the checkbox selections on the popup configure window and then click “OK”

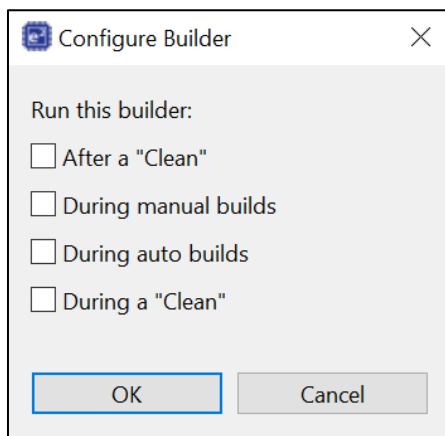


Figure 6-7 SC Code Generation Builder configure window

### 6.2.7 Note on the include path update issue when renaming the component's configuration name

When renaming the added component's configuration in e<sup>2</sup> studio Smart Configurator project that has self-defined include path setting for any folder or file, include path setting for that folder or file will keep the old name setting after code generation. This will cause build error when compiling the newly generated codes so please manually update the include path.

The folder or file which has self-defined include path setting can be recognized by checking the overlay icon (📁) on that folder or file. Below is an example on how to handle the include path update after renaming Compare Match Timer component configuration.

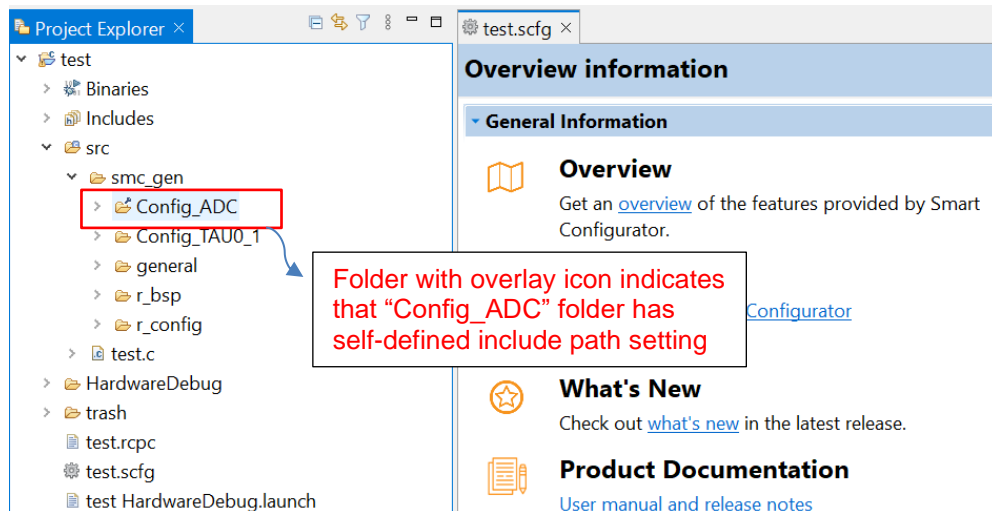


Figure 6-8 Interval Timer component configuration before renaming

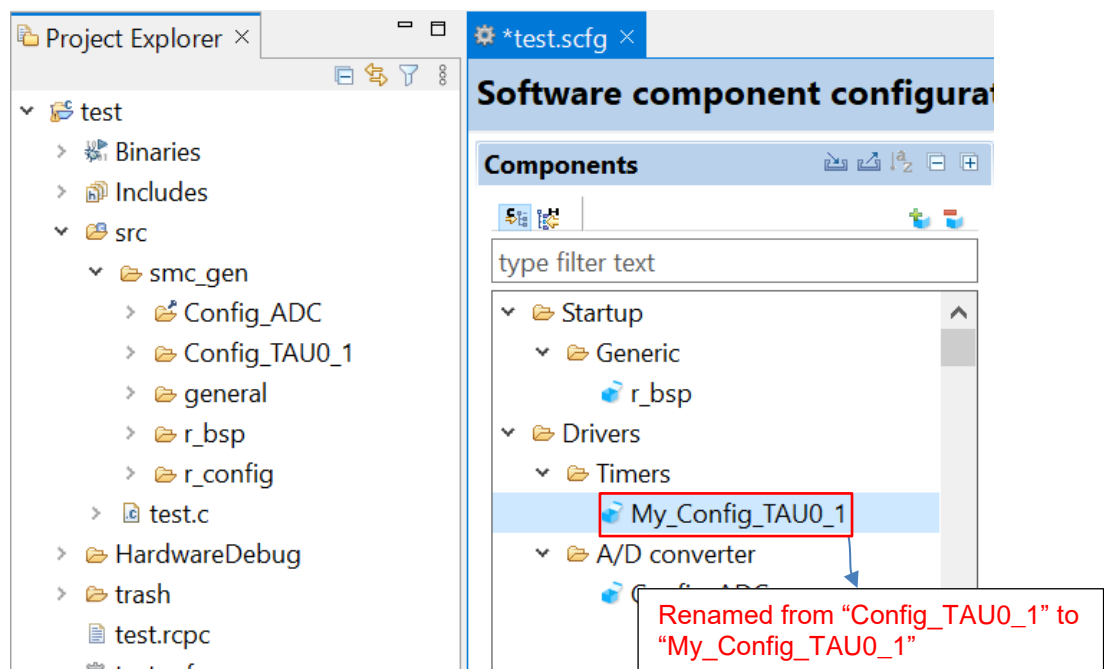


Figure 6-9 The Interval Timer component configuration after renaming

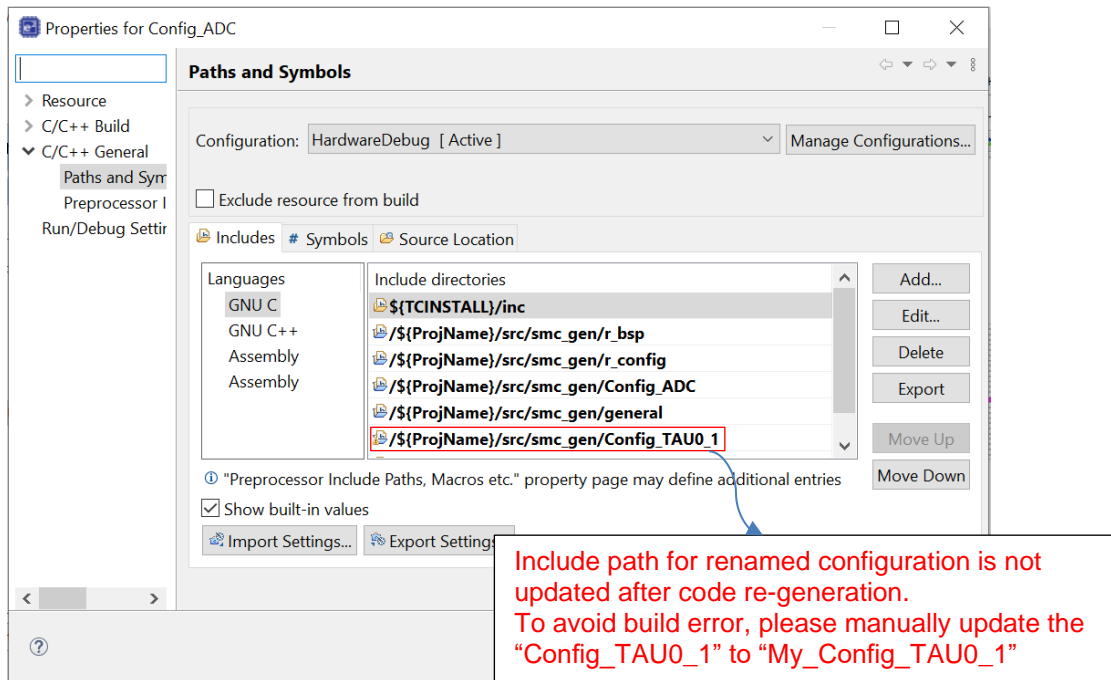


Figure 6-10 Include path setting for the "Config\_ADC" configuration

### Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Oct 20, 2022	-	First edition issued



## General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

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### 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

### 2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

### 3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

### 4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

### 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

### 6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).

### 7. Prohibition of access to reserved addresses

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