

Report No. MCR-22-0829

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RENESAS SEMICONDUCTOR RELIABILITY REPORT

SERIES : RH850/F1K

DEVICE : R7F7015874AFP-C

APPLICATION: Automobile

Quality Assurance Div. Renesas Electronics Corporation

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Q100 Qualification Test Results for R7F7015874AFP-C

[Note: Basically qualification tests were performed using a representative product with the same wafer process and the same package structure.]

Test	#	Reference	Test Condition	Lots	S.S.	Total	Results	Comments:	
1656		THE TENED						(Fail of Total)	(N/A =Not Applicable)
			TEST GRO	OUP A – ACCELERAT	ED ENVIR	ONMENT	STRESS TE	ESTS	
PC	A1	JESD22 A113 J-STD-020	Preconditioning: (Test @ Rm) SMD only; Moisture Preconditioning for TH &PTC Peak Reflow Temp=260°C		Min.MSL=3		MSL=3	-	
THB or HAST	A2	JESD22 A101	Temperature Humidity Bias: (Test @ Rm/Ho Ta=85°C, RH=85%, 1000hrs	3	77	231	0 of 231	-	
AC or UHST or TH	A3	JESD22 A118	Unbiased Highly Accelerated Stree Test: (Te 110°C, 85% RH, 264h	3	77	231	0 of 231	-	
TC	A4	JESD22 A104	Temperature Cycle: (Test @ Hot) Ta=-65°C to 150°C, 500cyc	3	77	231	0 of 231 0 Fails after TC (WBP)	-	
PTC	A5	JESD22 A105	Power Temperature Cycle: (Test @ Rm/Hot)	-	-	-	-	N/A	
HTSL	A6	JESD22 A103	High Temperature Storage Life: (Test @ Rm Ta=150°C, 1000hrs	1	45	45	0 of 45	-	
			TEST GRO	OUP B – ACCELERAT	ED LIFET	IME SIMUI	LATION TI	ESTS	
HTOL	В1	JESD22 A108	High Temp Operating Life: (Test @ Rm/Col Ta=150°C, 1000hrs	3	77	231	0 of 231	-	
ELFR	В2	AEC-Q100-008	Early Life Failure Rate: (Test @ Rm/Hot) Ta=125°C, 48hrs	3	800	2400	0 of 2400	-	
EDR	В3	AEC-Q100-005	NVM Endurance & Data Retention Test:	For HTOL	3	77	231	0 of 231	-
LDK	ВЭ	11DC-Q100-003	(Test @ Rm/Hot)	For HTSL	1	45	45	0 of 45	-

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Test	#	Reference	Test Conditions		S.S.	Total	Results (Fail of Total)	Comments: (N/A =Not Applicable)				
	TEST GROUP C – PACKAGE ASSEMBLY INTEGRITY TESTS											
WBS	C1	AEC-Q100-001 AEC-Q003	Wire Bond Shear Test: (Cpk > 1.67)		5 parts Min.	30 bonds	0 of 30bonds	Cpk>1.67				
WBP	C2	Mil-STD-883 Method 2011 AEC-Q003	Wire Bond Pull: (Cpk > 1.67); Each bonder used	30 bonds	5 parts Min.	30 bonds	0 of 30bonds	Cpk>1.67				
SD	C3	JESD22 B102 JSTD-002D	Solderability: (>95% coverage) 8 hr steam aging prior to testing	1	15	15	0 of 15					
PD	C4	JESD22 B100, JESD22 B108 AEC-Q003	Physical Dimensions: (Cpk > 1.67)	3	10	30	0 of 30	Cpk>1.67				
SBS	C5	AEC-Q100-010 AEC-Q003	Solder Ball Shear: (Cpk > 1.67); 5 balls from min. of 10 devices	-	-	-	-	N/A				
LI	C6	JESD22 B105	Lead Integrity: (No lead cracking or breaking); Through-hole only; 10 leads from each of 5 devices		-	-	-	N/A				
			TEST GROUP D – DIE FAB	RICATION	RELIABIL	ITY TESTS	S					
EM	D1	JESD61	Electromigration:	-	-	-	Pass	Confirmed by process TEG				
TDDB	D2	JESD35	Time Dependant Dielectric Breakdown:	-	-	-	Pass	Confirmed by process TEG				
HCI	D3	JESD60 & 28	Hot Carrier Injection:	-	-	-	Pass	Confirmed by process TEG				
NBTI	D4	JESD90	Negative Bias Temperature Instability:	-	-	-	Pass	Confirmed by process TEG				
SM	D5	JESD61,87 & 202	Stress Migration:	-	-	-	Pass	Confirmed by process TEG				

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Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results (Fail of Total)	Comments: (N/A =Not Applicable)
			TEST GROUP E- ELE	CTRICAL	VERIFICA	TION		
TEST	E1	User/Supplier Specification	Pre and Post Stress Electrical Test:	All	All	All	0 of All	-
НВМ	E2	AEC-Q100-002	Electrostatic Discharge, Human Body Model: (Test @ Rm/Hot); (2KV HBM / Class 2 or better)	1	3	3	0 of 3 ESD Level= HBM:2	HBM>2KV
CDM	E3	AEC-Q100-011	Electrostatic Discharge, Charged Device Model: (Test @ Rm/Hot); (750V corner leads, 500V all other leads / Class C4B or better)	1	3	3	0 of 3 ESD Level= CDM:C4B	Corner leads: 750V Pass All other leads:500V Pass
LU	E4	AEC-Q100-004	Latch-Up: (Test @ Rm/Hot)	1	6	6	0 of 6	-
ED	E5	AEC-Q100-009 AEC-Q003	Electrical Distributions: (Test @ Rm/Hot/Cold) (where applicable, Cpk>1.67)	3	30	90	Cpk>1.67	-
FG	E6	AEC-Q100-007	Fault Grading:	1	-	-	>98%	-
CHAR	E7	AEC-Q003	Characterization: (Test @ Rm/Hot/Cold)	1	-	-	Pass	According to Renesas standard procedure
EMC	E9	SAE J1752/3	Electromagnetic Compatibility (Radiated Emissions)	1	1	1	0 of 1	-
SC	E10	AEC Q100-012	Short Circuit Characterization	-	-	-	-	N/A
SER	E11	JESD89-1 JESD89-2 JESD89-3	Soft Error Rate	1	3	3	Pass	-
LF	E12	AEC-Q005	Lead (Pb) Free: (see AEC-Q005)	-	-	-	Pass	Solderability: See SD (C3) result. Solder heat resistance: N/A (Wave Solder is Not recommended.) Whisker: Performed on product TEG with test method based on JESD201.

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Test	#	Reference	Test Conditions		S.S.	Total	Results (Fail of Total)	Comments: (N/A =Not Applicable)				
	TEST GROUP F – DEFECT SCREENING TESTS											
PAT	F1	AEC-Q001	Process Average Testing: (see AEC-Q001)		All	All	Reject units outside PAT limits	Apply to mass production according to Renesas standard procedure				
SBA	F2	AEC-Q002	Statistical Bin/Yield Analysis: (see AEC-Q002)	All	All	All	Reject units outside criteria	Apply to mass production according to Renesas standard procedure				
	TEST GROUP G - CAVITY PACKAGE INTEGRITY TESTS (for Ceramic Package testing only)											
MS	G1	JESD22 B104	Mechanical Shock: (Test @ Rm)		-	-	-	N/A				
VFV	G2	JESD22 B103	Variable Frequency Vibration: (Test @ Rm)	-	-	-	-	N/A				
CA	G3	MIL-STD-883 Method 2001	Constant Acceleration: (Test @ Rm)	-	-	-	-	N/A				
GFL	G4	MIL-STD-883 Method 1014	Gross and Fine Leak:	-	-	-	-	N/A				
DROP	G5		Drop Test: (Test @ Rm) MEMS cavity parts only. Drop part on each of 6 axes once from a height of 1.2m onto a concrete surface.	-	-	-	-	N/A				
LT	G6	MIL-STD-883 Method 2004	Lid Torque:	-	-	-	-	N/A				
DS	G7	MIL-STD-883 Method 2019	Die Shear:	-	-	-	-	N/A				
IWV	G8	MIL-STD-883 Method 1018	Internal Water Vapor:	-	-	-	-	N/A				

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Calculation method of standard failure rate

Operating reliability is decided by inherent reliability of device and environment condition of use (See below).

·Calculation method of standard failure rate (λ)

$$\lambda = \underline{\lambda b} \times \underline{\pi T}$$
 (FIT)

(2)Temperature parameter

(1)Basic failure rate

(1) Basic failure rate (λ)

Ea :
$$0.7(eV)$$
 $\lambda b : 0.0011$ (FIT)

(2) Temperature parameter (πT)

$$\pi \text{ T=exp} \left\{ 11600 \times \text{Ea} \times \left(\frac{1}{273 + 55} - \frac{1}{273 + \text{Ta}} \right) \right\}$$

Ea : Activation energy(eV)
Ta : ambient temperature

πT simplified chart (Ea=0.7eV)												
Ta(°C)	40	50	55	60	65	70	75	80	85	90	100	110
πТ	0.31	0.68	1.00	1.45	2.08	2.95	4.15	5.77	7.96	10.88	19.82	34.99

•Confidence level 60% •Standard temperature Ta = 55°C

(3) MTTF (Mean Time To Failure)

MTTF =
$$\frac{1}{\lambda}$$