

# User Manual

## DA9061-63 Motherboard

### UM-PM-012

#### **Abstract**

*Explains the setup and operation of the DA9061, DA9062, and DA9063 motherboard.*

## DA9061-63 Motherboard

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## 1 Terms and Definitions

|      |                                   |
|------|-----------------------------------|
| DUT  | Device Under Test                 |
| GUI  | Graphical User Interface          |
| PMIC | Power Management IC               |
| ULI  | USB Lab IO Interface Chip (Atmel) |



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- All power outputs are available as pairs of pins to permit true Kelvin sensing of output voltage under load conditions.
- The board is intended to be supplied from a USB-host with approximate 5 V supply voltage. On-board boost and LDOs are used to regulate the supply.
- The DUT is supplied separately by a single 3.6 V supply (nominal) plugged into the 4 mm sockets VSYS and GND. A Lithium ion battery may be used for the same purpose, or a 'sourcemeter' such as Keithley 2400 or Hameg 8142.
- To avoid unexpected behaviour (back drive, unwanted GPIO triggering) of the DUT, never disconnect the USB connection from the PC while the DUT is powered.

### 2.1 Links

| Link | Position 1-2   | Position 2-3 Where Applicable | Function   |
|------|--|-------------------------------|--|
| J2   | VLDOCORE, or<br>VBUCK4, or<br>VDD_ULI_3v3, or<br>VDDIO_ULI_1V8 |                               | Selects VDDIO1 for the DUT   |
| J3   | VLDOCORE, or<br>VBUCK4, or<br>VDD_ULI_3v3, or<br>VDDIO_ULI_1V8 |                               | Selects VDDIO2 for the DUT   |
| J4   | VDDIO1   | VDDIO2                        | Selects VDDIO_GPIO for the DUT   |
| J5   | To 5V_USB  |                               | Connects 5V_USB supply to VSYS.<br>Note: Do not use with loaded regulators               |
| J12  | Position 3-5<br>To NIRQ (DUT)                                  | Position 1-3<br>Do not use    | Connects NIRQ to a 100 kΩ pull-up/down resistor  |
| J12  | Position 4-6<br>To NRESET (DUT)                                | Position 2-4<br>Do not use    | Connects NRESET to a 100 kΩ pull-up/down resistor  |
| J13  | Position 1-3<br>To VDDIO_ULI_1V8                               |                               | Connects supply for GPIO level shifter (ULI side)  |
| J13  | Position 2-4<br>To VDDIO_GPIO                                  |                               | Connects supply for GPIO level shifter (DUT side)  |
| J14  | To USB   |                               | Controls GPIOs and GPFB2, GPFB3 from USB device  |
| J15  | To ground  | To VDDIO_GPIO                 | Connects GPIOs and GPFB2, GPFB3 to pre-selected voltage via 100 kΩ pull-up/down resistor |
| J17  | Position 4-6<br>To GND   | Position 2-4<br>To VDDIO_GPIO | Selects NIRQ pull-up/down  |
| J17  | Position 3-5<br>To GND   | Position 1-3<br>To VDDIO_GPIO | Selects NRESET pull-up/down  |
| J20  | To USB   | To USB                        | Connects MISO and NCS_0 to level shifter   |
| J21  | To DUT   | To DUT                        | Connects SO and NCS to level shifter   |
| J233 | To USB   | To USB                        | Connects SCLK and MOSI to level shifter  |
| J234 | To DUT   | To DUT                        | Connects SK and SI to level shifter  |
| J26  | Position 1-3<br>To VDDIO_ULI_1V8                               |                               | Connects supply for I <sup>2</sup> C level shifter (ULI side)                            |

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| Link | Position 1-2                         | Position 2-3 Where Applicable | Function  |
|------|--------------------------------------|-------------------------------|---|
| J26  | Position 2-4<br>To VDDIO_GPIO        |                               | Connects supply for I <sup>2</sup> C level shifter (DUT side) |
| J27  | SPI                                  | I2C / SW controlled           | Select communication mode                                     |
| J28  | To USB                               | To USB                        | Connects SCL_ULI_0 and SDA_ULI_0 to level shifter             |
| J29  | Position 1-3<br>To VDDIO_ULI_1V8_I2C |                               | Connects supply for I2C level shifter (ULI side)              |
| J29  | Position 2-4<br>To VDDIO_ULI_3V3     |                               | Connects supply for I2C level shifter (Peripheral side)       |
| J30  | To USB                               | To USB                        | Connects SCL_ULI_1 and SDA_ULI_1 to level shifter             |
| J31  | To DUT                               | To DUT                        | Connects GPIO14 and GPIO15 to level shifter                   |
| J33  | Position 2-4<br>To VBOARD_5.5V       |                               | Connects supply for MUX addressing level shifter (MUX side)   |
| J33  | Position 1-3<br>To VBOARD_5.5V       |                               | Connects supply for MUX addressing level shifter (ULI side)   |
| J34  | To VBOARD                            | To 5V_USB                     | Select board supply (EXT/USB)                                 |
| J35  | To USB                               | To USB                        | Connects SCL_ULI_1 and SDA_ULI_1 to level shifter             |
| J36  | To peripheral                        | To DUT                        | Connects SCL_3V3 and SDA_3V3 to level shifter                 |
| J40  | To TP                                | To MUX                        | Connects TP to MUX and TP select switch                       |
| J41  | To MUX 1                             |                               | Connects signal rails to MUX 1                                |
| J44  | To TP select switch                  |                               | Connects different voltage levels to S2                       |
| J45  | Position 2-4<br>To VDD_ULI_3V3       |                               | Connects power supply for potentiometer                       |
| J45  | Position 1-3<br>To VDD_ULI_3V3       |                               | Connects signal supply for potentiometer                      |
| J46  | SW controlled                        | Manual control                | Selects OTP programming mode                                  |
| J47  | Position 1-2<br>To VDD_7V5           |                               | Connects supply for OPAMPs                                    |
| J47  | Position 3-4<br>To VBOARD_5.5V       |                               | Connects supply MUXs  |
| J48  | To DUT                               |                               | Connects analogue values from DAC to DUT                      |
| J50  | To ADC                               |                               | Connects mainly MUX outputs to ADC                            |
| J52  | To LDO                               |                               | Connects LDO to VBOARD_5.5V                                   |
| J53  | To VDD_7V5                           |                               | Connects VDD_7V5 to LDO                                       |
| J54  | To MUX 2                             |                               | Connects signal rails to MUX 2                                |
| J55  | Position 1-3<br>To NONKEY            |                               | Connect USB interface to NONKEY                               |
| J55  | Position 2-4                         |                               | Connect pull-up to NONKEY                                     |

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| Link | Position 1-2                   | Position 2-3 Where Applicable        | Function  |
|------|--------------------------------|--------------------------------------|---|
|      | To pull-up                     |                                      |   |
| J56  | Position 1-3<br>To OFFKEY      |                                      | Connect USB interface to OFFKEY   |
| J56  | Position 2-4<br>To pull-up     |                                      | Connect pull-up to OFFKEY   |
| J57  | Position 1-3<br>To SHUTDOWN    |                                      | Connect USB interface to SHUTDOWN   |
| J57  | Position 2-4<br>To pull-up     |                                      | Connect pull-up to SHUTDOWN   |
| S2   | Position left<br>SW controlled | Position right<br>Forced normal mode | TP select:<br>Right => the TP pin is grounded via 10 kΩ pull-down<br>Left => the TP pin is connected to the TP control matrix |

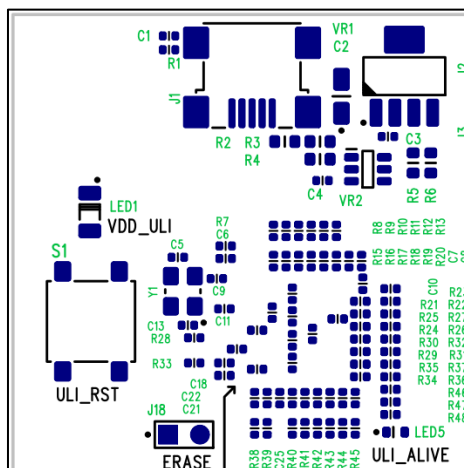
## 2.2 Motherboard Features

### 2.2.1 USB Interface

The USB Interface U12 (top-left corner of the PCB) is used here mainly for three purposes:

1. As a source of I<sup>2</sup>C and SPI (DA9063 only) control signals.
2. To provide and read discrete signals from/to the GPIOs
3. To communicate with on-board peripherals

The USB device is powered via the USB bus cable through fixed LDO regulators.



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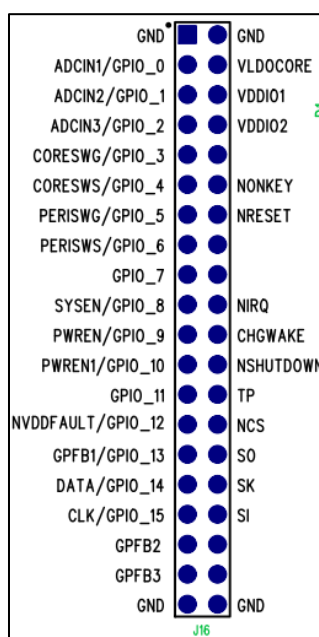


Figure 3: Control and IO Signals

## 2.2.3 PU/PD of IO Signals and Connection to USB

The arrangement of the jumper links to the GPIO pins allows maximum flexibility.

Insert the jumpers in J14 for USB control and monitoring.

Place the jumpers in J15 on the left side to connect VDDIO\_GPIO via 100 kΩ pull-up resistors, on the right side to connect ground via 100 kΩ pull-down resistors, or leave it open for external connections (see Figure 5).

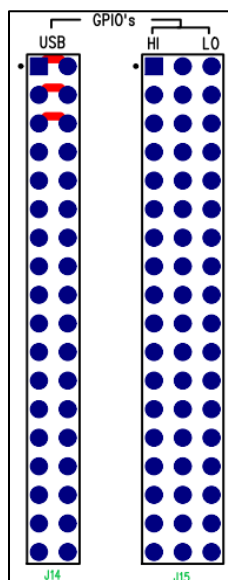


Figure 4: PU/PD and USB Connections



## DA9061-63 Motherboard

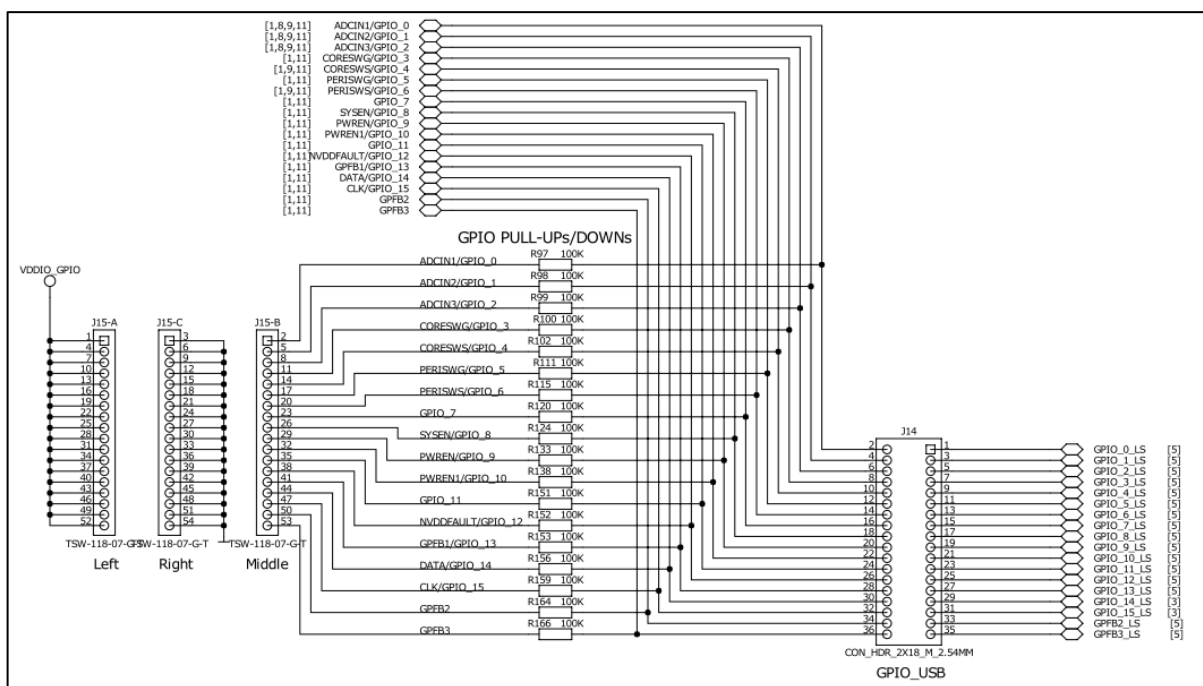


Figure 5: PU/PD/USB Schematic

## 2.2.4 Voltage Outputs from DUT

## 2.2.4.1 LDOs

The pin headers to access the LDO regulators from the DUT are located on the left side of the DUT connectors. Depending on the connected DUT type either J32 (DA9061/62) or J37 (DA9063) is valid.

They are arranged in pairs (left: thick power lines, right: thin sense line for Kelvin connection) for meaningful measurements under load conditions.

Each pin is connected separately to the regulator output, to a point closest to the device pin.

If required, a suitable connector can bring these signals to the system board for integrated development.

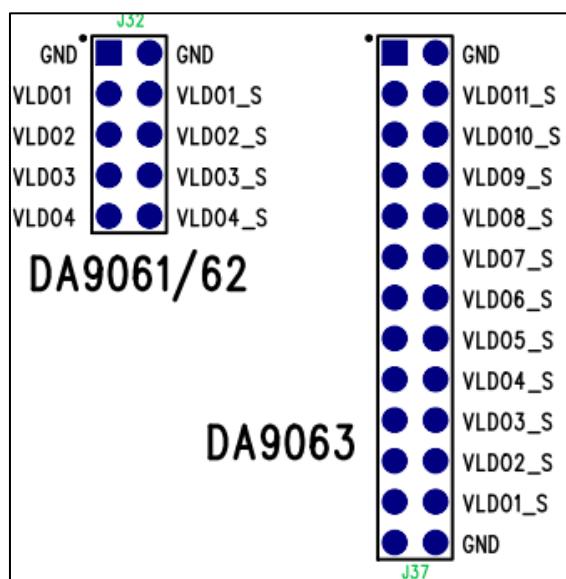


Figure 6: LDO Connectors

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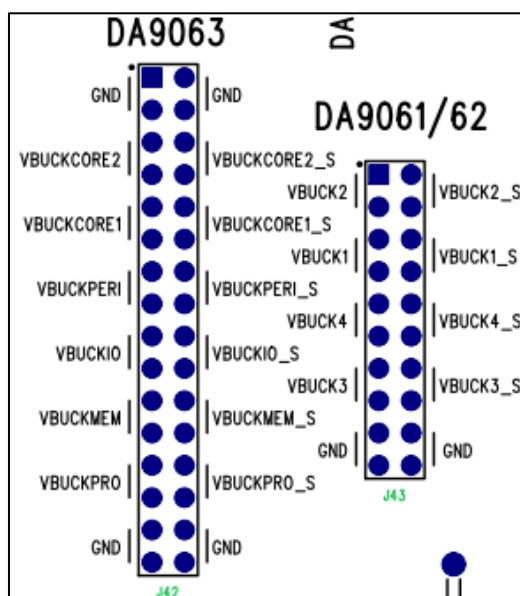
### 2.2.4.2 Bucks

The pin headers to access the Buck regulators from the DUT are located on the right side of the DUT connectors. Depending on the connected DUT type either J43 (DA9061/62) or J42 (DA9063) is valid.

They are arranged in pairs (left: thick power lines, right: thin sense line for Kelvin connection) for meaningful measurements under load conditions.

Each pin is connected separately to the regulator output, to a point as close as possible to the device pin.

If required, a suitable connector can bring these signals to the system board for integrated development.



**Figure 7: BUCK Connectors**

The left connections (for example VBUCK1) are routed with wide PCB traces, while the right connections (for example VBUCK1\_S) are routed with narrow PCB traces. The right connections are intended as Kelvin sense points, to allow regulator output measurement without effect from PCB resistance. This connection is not ideal since the plug that the daughterboard is mounted on adds some parasitic resistance at each pin which produces a small error when under load. For accurate performance measurements under load it is suggested to connect directly to the daughterboard pins.

### 2.2.5 VDDIO Select

This group of links allows selection of the VDDIO\_GPIO voltage rail, for example for GPIO pull-up.

VDDIO\_GPIO can be selected via VDDIO1 or VDDIO2 (VDDIO2 shown in example), each supplied either from VBUCKIO (VBUCK4), VLDOCORE, external 3.3 V or external 1.8 V. External voltages are supplied by the USB via external LDOs.

VDDIO1/2 can be selected by J2/J3 and VDDIO\_GPIO can be selected through VDDIO1/2 via J4.

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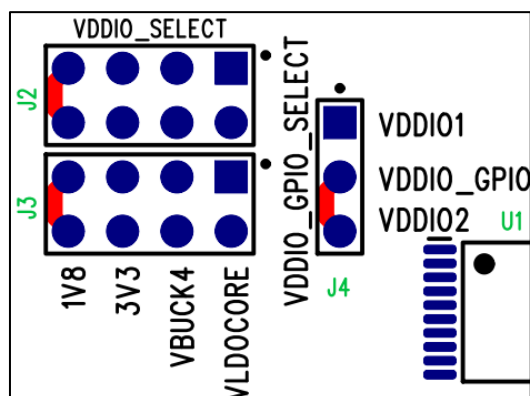


Figure 8: BUCK Connectors

A VDDIO1/2 voltage may cause back-powering of DUT from the VDDIO rail, particularly when external supplies are used (1.8 V, 3.3 V) without main VSYS supply. This may keep the digital core of the DUT powered, thereby preventing a POR of the logic and leading to undesired operating modes.

The VDDIO1/2 and VDDIO\_GPIO selection is shown in the diagram below.

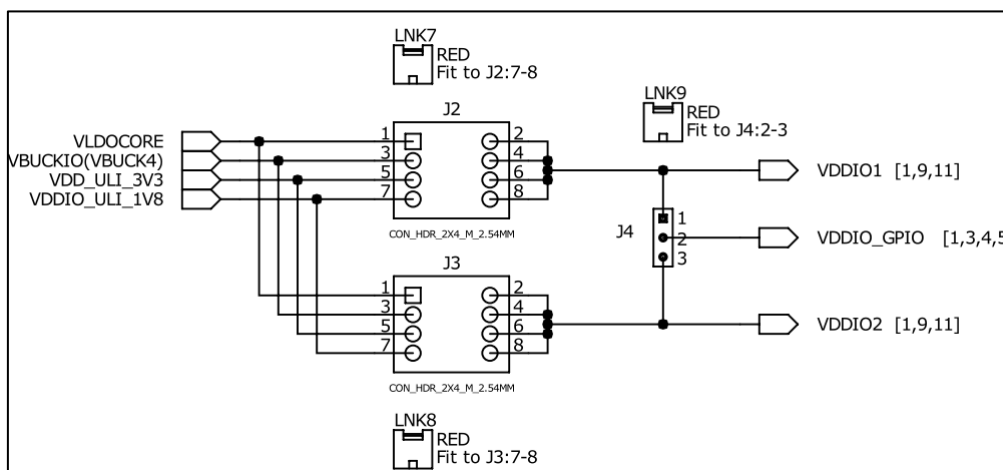


Figure 9: VDDIO1/2 and VDDIO\_GPIO

### 2.2.6 Test Pin (TP), PC Mode and OTP Programming Mode

The TP select switch selects between normal mode and Power Commander (PC) mode/OTP programming mode.

If configured in the right-hand position (TP\_OFF), the TP pin of the DUT is grounded via a 10 kΩ pull-down resistor, thereby selecting normal mode operation. In this case the register settings are loaded from a programmed OTP.

If configured on the left-hand position (TP\_ON), the TP can be connected to higher voltage levels.

The Smartcanvas GUI automatically selects the desired level, where 5 V activates the PC mode and 7.5 V activates the OTP programming mode or 0 V to select normal operation mode.

In PC mode, register settings are loaded from a file through the software interface.

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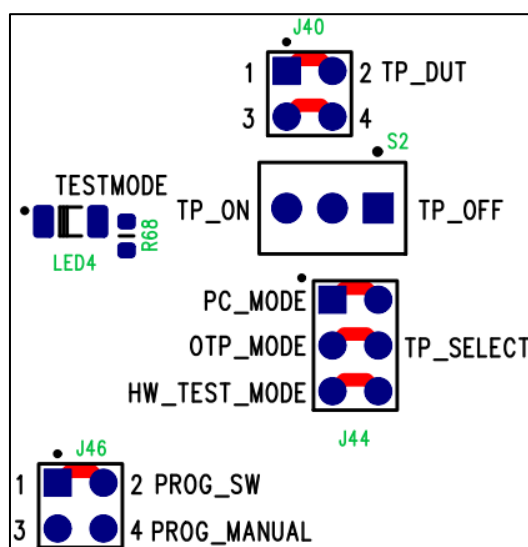


Figure 10: TP Select, PCB

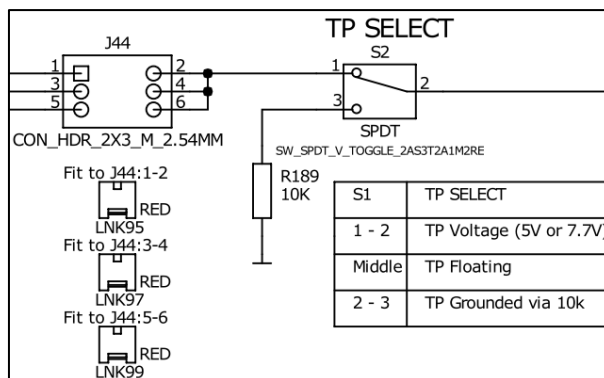


Figure 11: TP Select, Schematic

If a mode apart from normal mode is selected, a red LED (LED4) indicates that the TP test mode pin is supplied with a level other than 0 V.

### 2.2.7 On-Board Multiplexer and ADC

The motherboard has two multiplexers (MUX) where all power lines and some GPIOs from the DUT are connected. The output of the MUX is measured via an external ADC.

The front panel of the Smartcanvas GUI shows the most important measurements for a quick overview of the DUT.

#### NOTE

For precise measurements, use calibrated equipment only.

In some cases (such as quiescent current measurements) the input channels might need to be disconnected from the MUX. This can be done by removing the jumper links on J41 and J54.

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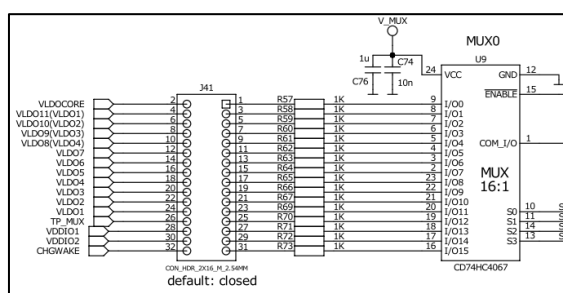


Figure 12: MUX1

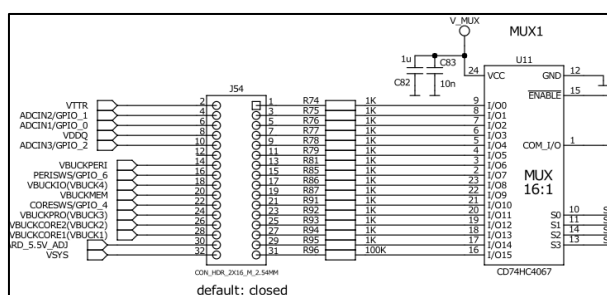


Figure 13: MUX2

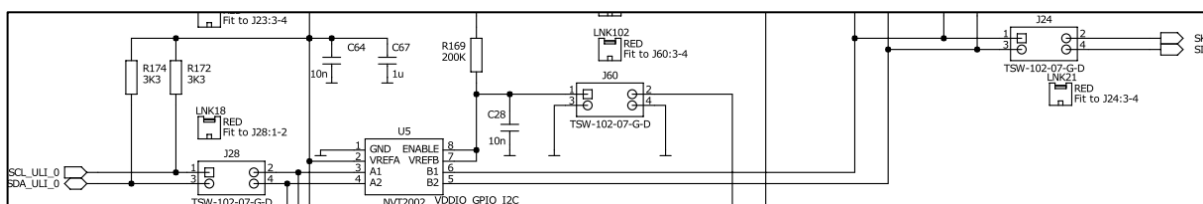
2.2.8 I<sup>2</sup>C Interface

The USB controller (ULI) provides two I<sup>2</sup>C master busses to communicate with connected I<sup>2</sup>C slaves.

The DUT communicates with the controller with bus0 (SDA/SCL\_ULI\_0), while bus1 (SDA/SCL\_ULI\_1) is used to communicate with all other peripherals on the motherboard.

Both busses have their own level shifter between master and slave. These level shifters can be disconnected from the slave by removing jumper links.

For bus0 only, J24 (DA906x) and J24/J31 (DA9063 only) can be opened to connect to a customer system board for integrated development.

Figure 14: I<sup>2</sup>C Level Shifter

## 3 Hardware Issues

Most hardware problems can be traced to incorrect jumper positions.

Check jumper positions carefully and compare them with the default positions: see Figure 1. Use the jumper table details and the board schematic as a guide to jumper functions and locations.

**NOTE**

When using the GUI to select a mode, the Power Commander switch must be in the left-hand position.

## Revision History

| Revision | Date        | Description  |
|----------|-------------|--|
| 1.0      | 12-Jan-2015 | Initial version  |
| 2.0      | 06-Jan-2016 | Changed references to Smartcanvas GUI.<br>Typographical edits. |
| 3.0      | 25-Feb-2022 | File was rebranded with new logo, copyright and disclaimer     |

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**DA9061-63 Motherboard****Status Definitions**

| Status                  | Definition   |
|-------------------------|--|
| DRAFT                   | The content of this document is under review and subject to formal approval, which may result in modifications or additions. |
| APPROVED<br>or unmarked | The content of this document has been approved for publication.  |

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