User's Manual

RAJ306000 Series

User's Manual: Hardware

General purpose Motor control IC

Renesas Electronics
www.renesas.com

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(Rev.3.0-1 November 2016)

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses Access to reserved addresses is prohibited.

   The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

How to Use This Manual

Readers This manual is intended for user engineers who wish to understand the functions of the RL78/G1F and design and develop application systems and programs for these devices. The target products are as follows.

- 64-pin: RAJ3060xx (xx = 01,10)

Purpose This manual is intended to give users an understanding of the functions described in the **Organization** below.

Organization The RAJ306000 series manual is separated into three parts: this manual, RL78/G1F hardware Manual and the software edition. This manual explains the function unique to RAJ306000 series. For detailed usage of the RL78/G1F microcomputer, refer to the RL78 / G1F User's Manual Hardware(R01UH0516E) and "Technical Update" on RL78/G1F. (common to the RL78 family).

RAJ306000 Series User's Manual Hardware (This Manual)	**RL78/G1F User's Manual Hardware**	**RL78 Family User's Manual Software**
About RAJ36000 • Pin functions • Internal block functions • Pre-Driver function • How to use RL78/G1F	About RL78/G1F • Pin functions • Internal block functions • Interrupts • Other on-chip peripheral functions • Electrical specifications	• CPU functions • Instruction set • Explanation of each instruction

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electrical engineering, logic circuits, and microcontrollers.

•To gain a general understanding of functions:

→ Read this manual in the order of the **CONTENTS**. The mark "<R>" shows major revised points. The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

•How to interpret the register format:

•To know details of the RL78/G1F Microcontroller instructions:

→ Refer to the separate document **RL78 Family User's Manual Software(R01US0015E).**

Conventions

Data significance: Higher digits on the left and lower digits on the right

Active low representations: $\overline{\times\times\times}$ (overscore over pin and signal name)

Note: Footnote for item marked with Note in the text

Caution: Information requiring particular attention

Remark: Supplementary information

Numerical representations: Binary ···×××× or ××××B

Decimal ···××××

Hexadecimal ..××××Hor 0x××××

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
RAJ306000 Series User's Manual Hardware	This manual
RL78/G1F User's Manual Hardware	R01UH0516E
RL78 Family User's Manual Software	R01US0015E
Data sheet RAJ306001, RAJ306010 (General-Purpose Motor Control IC)	R18DS0034E

Documents Related to Flash Memory Programming (User's Manual)

Document Name		Document No.
PG-FP5 Flash Memory Programmer		-
	RL78, 78K, V850, RX100, RX200, RX600 (Except RX64x), R8C, SH	R20UT2923E
	Common	R20UT2922E
	Setup Manual	R20UT0930E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing. Other Documents

Document Name	Document No.
Renesas Microcontrollers RL78 Family	R01CP0003E
Semiconductor Package Mount Manual	R50ZZ0003E
Semiconductor Reliability Handbook	R51ZZ0001E

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Caution: This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.

CONTENTS

CHAPTER 1 Outline

1.1 Features

<R> RAJ306000 series is a general-purpose Motor control IC consists of RL78/G1F and Pre-Driver.

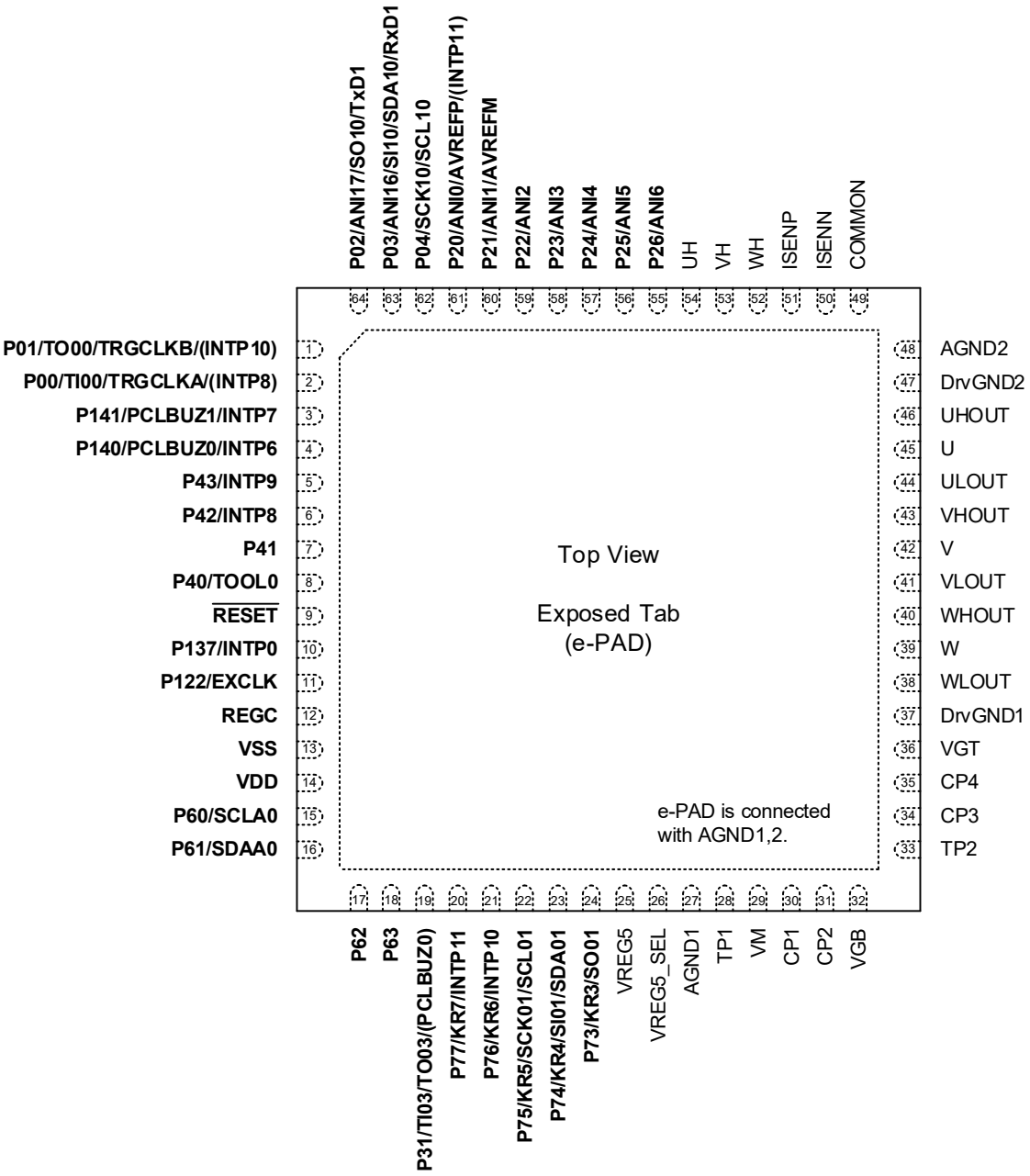
- RL78/G1F (R5F11BLEGFB)-powered
  - Code-Flash 64KB
  - Data-Flash 4KB
  - RAM 5.5KB
- Possible to drive three phase Brushless DC motors
  - Supports sensor [Hall based] and sensor-less control
  - Dead time adjustment function.
  - Adjustable gate drive current.
- Operating voltage: (Using double boost function of charge-pump
  - 6V to 30V for RAJ306001
  - 6V to 42V for RAJ306010
- Built in 5V regulator.
- Drive possible Nch MOSFET
- Peak gate drive current is 500mA.
- Driving mode is selectable. (PWM control or commutation control)
- Support safety function
  - The installed MCU (RL78/G1F) corresponds to IEC60730 safety standards.
  - Over temperature protection (Thermal Shutdown)
  - Over current protection (CS AMP, Built in 5V regulator)
  - Under-voltage detection (VM, charge-pump)
  - Over-voltage detection (Built in 5V regulator, charge-pump)
  - Motor lock detection
- Hall IC comparator
  - Adjustable input threshold voltage.
  - Adjustable input hysteresis voltage.
- Various measurement circuit.
  - VM voltage
  - Chip temperature (Pre-Driver)
  - Motor current
  - Back-EMF voltage

1.2 Pin Configuration (Top View)

Figure 1-1 shows the pin configuration diagram.
Table 1-1,Table 1-2, and Table 1-3 show the pin configuration table of RAJ306000 series.

<R>

Figure 1-1 Pin configuration diagram



Note:
Bold text : RL78 pins
Normal-face font : Pre-driver pins

Table 1-1 Terminal table (1/3)

RL78 or Pre-Driver	PIN		I/O level	IN/OUT or Power/GND	Initial Condition	Function
	Number	Name				
RL78	1	P01	VDD	I/O	Input Port	Main Function : GPIO Alternate Function : TO00/TRGCLKB/(INTP10)
	2	P00	VDD	I/O	Input port	Main Function : GPIO Alternate Function : TI00/TRGCLKA/(INTP8)
	3	P141	VDD	I/O	Input port	Main Function : GPIO Alternate Function : PCLBUZ1/INTP7
	4	P140	VDD	I/O	Input port	Main Function:GPIO Alternate Function:PCLBUZ0/INTP6
	5	P43	VDD	I/O	Input port	Main Function:GPIO Alternate Function:INTP9
	6	P42	VDD	I/O	Input port	Main Function:GPIO Alternate Function:INTP8
	7	P41	VDD	I/O	Input port	GPIO
	8	P40	VDD	I/O	Input port	Main Function:GPIO Alternate Function:TOOL0
	9	$\overline{\text{RESET}}$	VDD	-	Input port	Reset pin
	10	P137	VDD	INPUT	Input port	Main Function:GPI Alternate Function:INTP0
	11	P122	VDD	INPUT	Input port	Main Function : GPI Alternate Function : EXCLK
	12	REGC	VDD	-	-	Regulator output
	13	VSS	VDD	GND		Ground potential for RL78/G1F pin.
	14	VDD	VDD	Power		Positive power supply for RL78/G1F pin.
	15	P60	VDD	I/O	Input port	Main Function : GPIO Alternate Function : SCLA0
	16	P61	VDD	I/O	Input port	Main Function : GPIO Alternate Function : SDAA0
	17	P62	VDD	I/O	Input port	GPIO
	18	P63	VDD	I/O	Input port	GPIO
	19	P31	VDD	I/O	Input port	Main Function : GPIO Alternate Function :TI03/TO03/(PCLBUZ0)
	20	P77	VDD	I/O	Input port	Main Function : GPIO Alternate Function : KR7/INTP11
	21	P76	VDD	I/O	Input port	Main Function : GPIO Alternate Function : KR6/INTP10
	22	P75	VDD	I/O	Input port	Main Function : GPIO Alternate Function : KR5/SCK01/SCL01
	23	P74	VDD	I/O	Input port	Main Function : GPIO Alternate Function : KR4/SI01/SDA01
	24	P73	VDD	I/O	Input port	Main Function:GPIO Alternate Function:KR3/SO01

Table 1-2 Terminal table (2/3)

<R>

RL78 or Pre-Driver	PIN		I/O level	IN/OUT or Power/GND	Initial Condition	Function
	Number	Name				
Pre-Driver	25	VREG5	5V	IN/OUT	IN/OUT	Function of VREG5 pin is depends on VREG5_SEL pin level VREG5_SEL=GND:Built-in 5V regulator is selected. (Output 5V) VREG5_SEL=5V:External 5V regulator is selected (Input 5V)
	26	VREG5_SEL	VDD	IN	IN	
	27	AGND1	GND	GND	GND	Ground potential for analog and logic circuits of Pre-Driver.
	28	TP1	VDD	IN	IN	Terminal for Test. (Usually conect to GND via resistance.)
	29	VM	VM	Power	Power	Power Supply
	30	CP1	VGB	-	-	Charge pump flying capacitor for VGB (CP1)
	31	CP2	VGB	-	-	Charge pump flying capacitor for VGB (CP2)
	32	VGB	VGB	OUT	OUT	Gate drive voltage for Low-side
	33	TP2	5V	IN	IN	Terminal for Test. (Usually conect to GND)
	34	CP3	VM	-	-	Charge pump flying capacitor for VGT (CP3)
	35	CP4	VGT	-	-	Charge pump flying capacitor for VGT (CP4)
	36	VGT	VGT	OUT	OUT	Gate drive voltage for High-side
	37	DrvGND1	GND	GND	GND	Ground potential for driving circuits of Pre-Driver.
	38	WLOUT	VGB	OUT	OUT	Output of Pre-driver for W phase Low-side (Nch MOSFET).
	39	W	VM	IN	IN	W phase voltage.
	40	WHOUT	VGT	OUT	OUT	Output of Pre-driver for W phase High-side (Nch MOSFET).
	41	VLOUT	VGB	OUT	OUT	Output of Pre-driver for V phase Low-side (Nch MOSFET).
	42	V	VM	IN	IN	V phase voltage.
	43	VHOUT	VGT	OUT	OUT	Output of Pre-driver for V phase High-side (Nch MOSFET).
	44	ULOUT	VGB	OUT	OUT	Output of Pre-driver for U phase Low-side (Nch MOSFET).
	45	U	VM	IN	IN	U phase voltage.
	46	UHOUT	VGT	OUT	OUT	Output of Pre-driver for U phase High-side (Nch MOSFET).
	47	DrvGND2	GND	GND	GND	Ground potential for driving circuits of Pre-Driver.
	48	AGND2	GND	GND	GND	Ground potential for analog and logic circuits of Pre-Driver.
	49	COMMON	VM	IN	IN	Input for Common signal of Motor.
	50	ISENN	5V	IN	IN	Connect Negative side of Shunt resistor.
	51	ISENP	5V	IN	IN	Connect Positive side of Shunt resistor.
	52	WH	5V	IN	IN	RAJ306001:Input of Hall IC signal for W phase
				IN/OUT	IN	RAJ306010:Input of Hall IC signal for W phase. Output of BEFM amplifier signal.
	53	VH	5V	IN	IN	Input of Hall IC signal for V phase
	54	UH	5V	IN	IN	Input of Hall IC signal for U phase

Table 1-3 Terminal table (3/3)

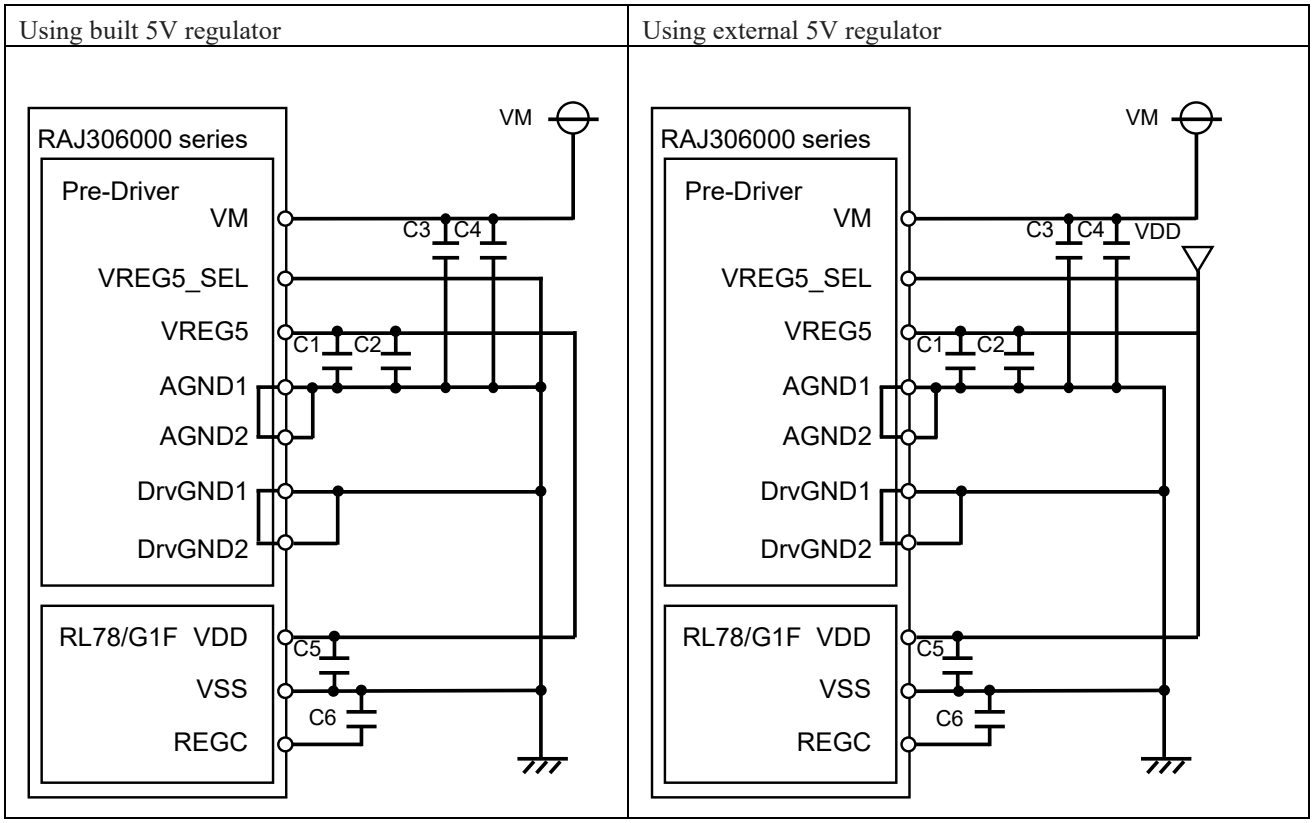
RL78 or Pre-Driver	PIN		I/O level	IN/OUT or Power/GND	Initial Condition	Terminal function
	Number	Name				
RL78	55	P26	VDD	I/O	Analog function	Main Function:GPIO Sub Function:ANI6
	56	P25	VDD	I/O	Analog function	Main Function:GPIO Sub Function:ANI5
	57	P24	VDD	I/O	Analog function	Main Function:GPIO Sub Function:ANI4
	58	P23	VDD	I/O	Analog function	Main Function:GPIO Sub Function:ANI3
	59	P22	VDD	I/O	Analog function	Main Function:GPIO Sub Function:ANI2
	60	P21	VDD	I/O	Analog function	Main Function:GPIO Sub Function:ANI1/AVREFM
	61	P20	VDD	I/O	Analog function	Main Function:GPIO Sub Function:ANI0/AVREFP/(INTP11)
	62	P04	VDD	I/O	Input port	Main Function:GPIO Sub Function:SCK10/SCL10
	63	P03	VDD	I/O	Analog function	Main Function:GPIO Sub Function:ANI16/SI10/SDA10/RxD1
	64	P02	VDD	I/O	Analog function	Main Function:GPIO Sub Function:ANI17/SO10/TxD1

1.3 Recommended circuit

1.3.1 Power supply

This IC has built in 5V regulator. When using built in 5V regulator, connect VREG5_SEL Pin to GND, Then Pre-Diver regulates 5V from VM and supply to Pre-Driver and RL78/G1F. And when using external 5V regulator, connect 5V to VREG5, VREG5_SEL and VDD.

Figure 1-2 Power Supply configuration and connection



Note 1: When not using internal 5V regulator, please supply same voltage of 5V to VREG5_SEL, VREG5 and VDD.
And the sequence is as follows.
●Start-up :VM → VREG5
●Finish :VREG5 → VM

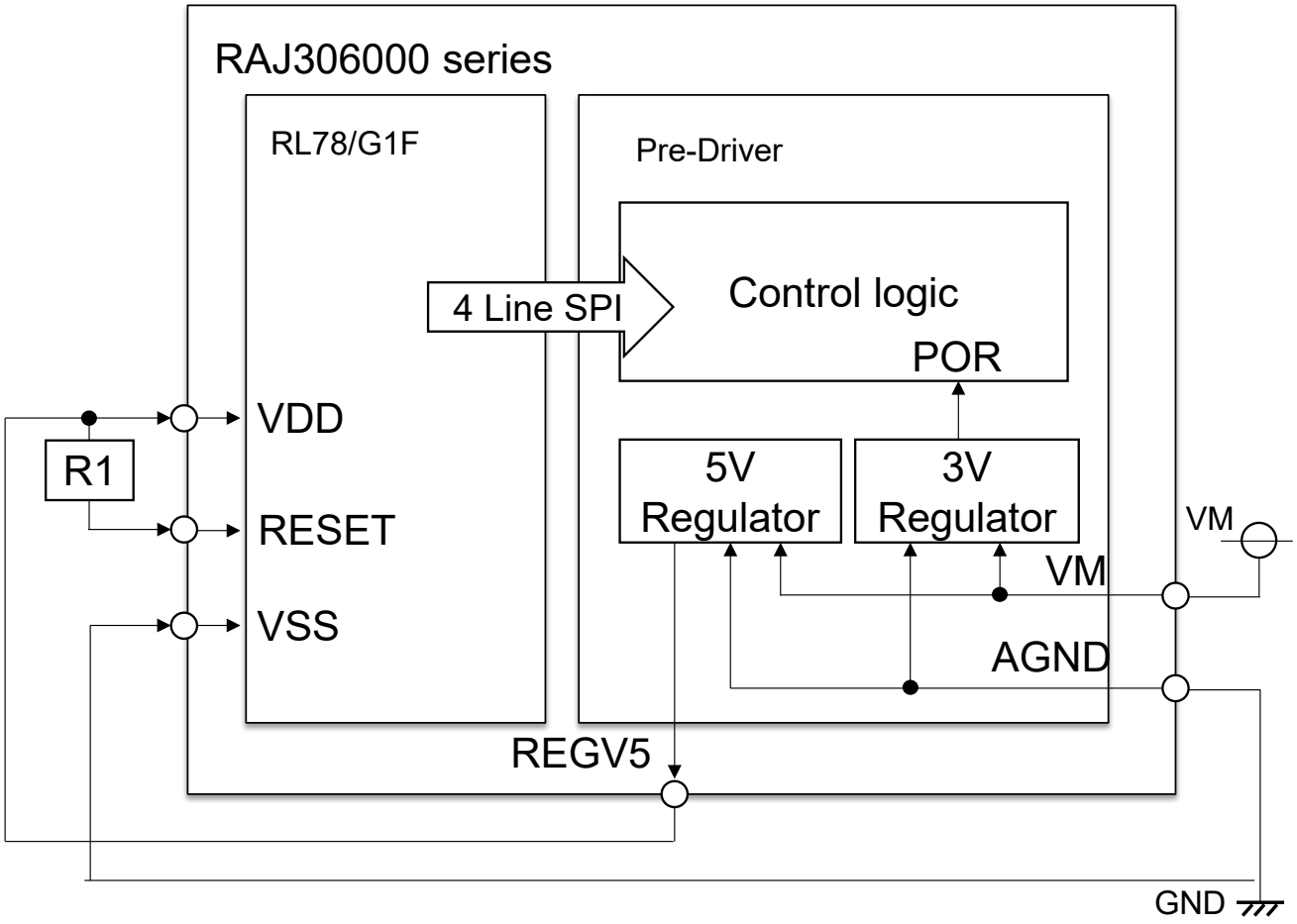
1.3.2 Reset function

This IC has the following two reset way.

- ●Power on reset by VM power supply
- ●Software reset by SPI communication.

RESET pin is reset for only RL78/G1F. So, when using reset pin, use with software reset.

Figure 1-3 Reset Construction.



1.3.3 Charge-pump

The Charge-pump external circuits are shown in Figure 1-4. The recommended circuit depends on whether double boost function of charge-pump use or not. CPSE2 register initial value is 02H, this means double boost function. If you don't use double Boost, set CPSET2=0CH before you start the charge pump.

<R> In RAJ306001, connect the smoothing capacitance C2 of VGT to either VM or DrvGND. It is recommended to connect to the VM for applications where the VM voltage changes significantly.

In RAJ306010, set the connection destination of VGT smoothing capacity C2 to VM. It is prohibited to connect to DrvGND.

Figure 1-4 Boost function of charge-pump and recommended circuit.

<R>

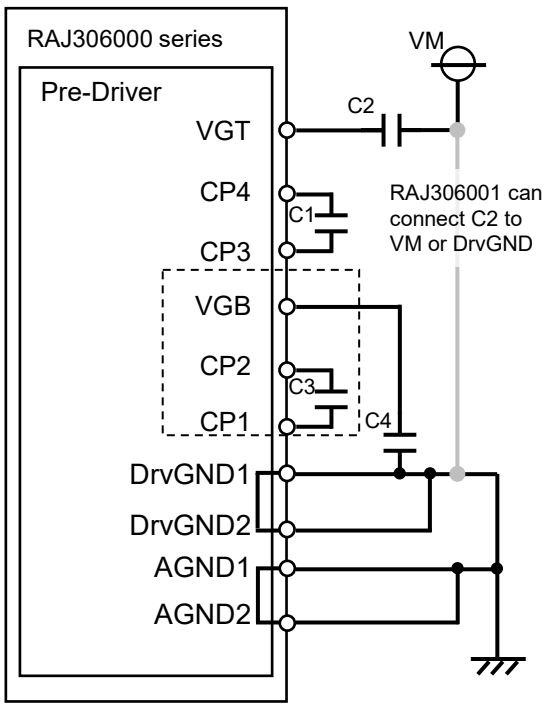
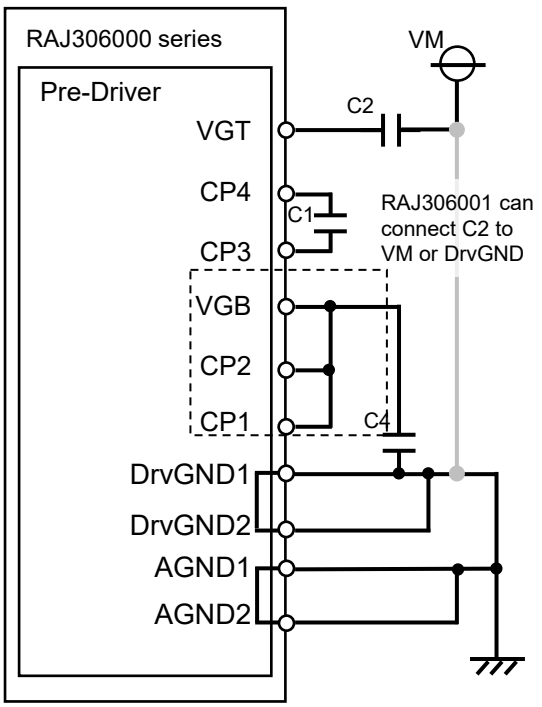
Use the double boost function of charge-pump. (CPSET2=02H : initial value)	Don't use the double boost function of charge-pump. (CPSET2=0CH)
	

Table 1-4 Boost Voltage

Setting	VGB(V)	VGT(V)
Double Boost	13	VM+13
Not double Boost	10	VM+10

1.4 Recommended drive waveform

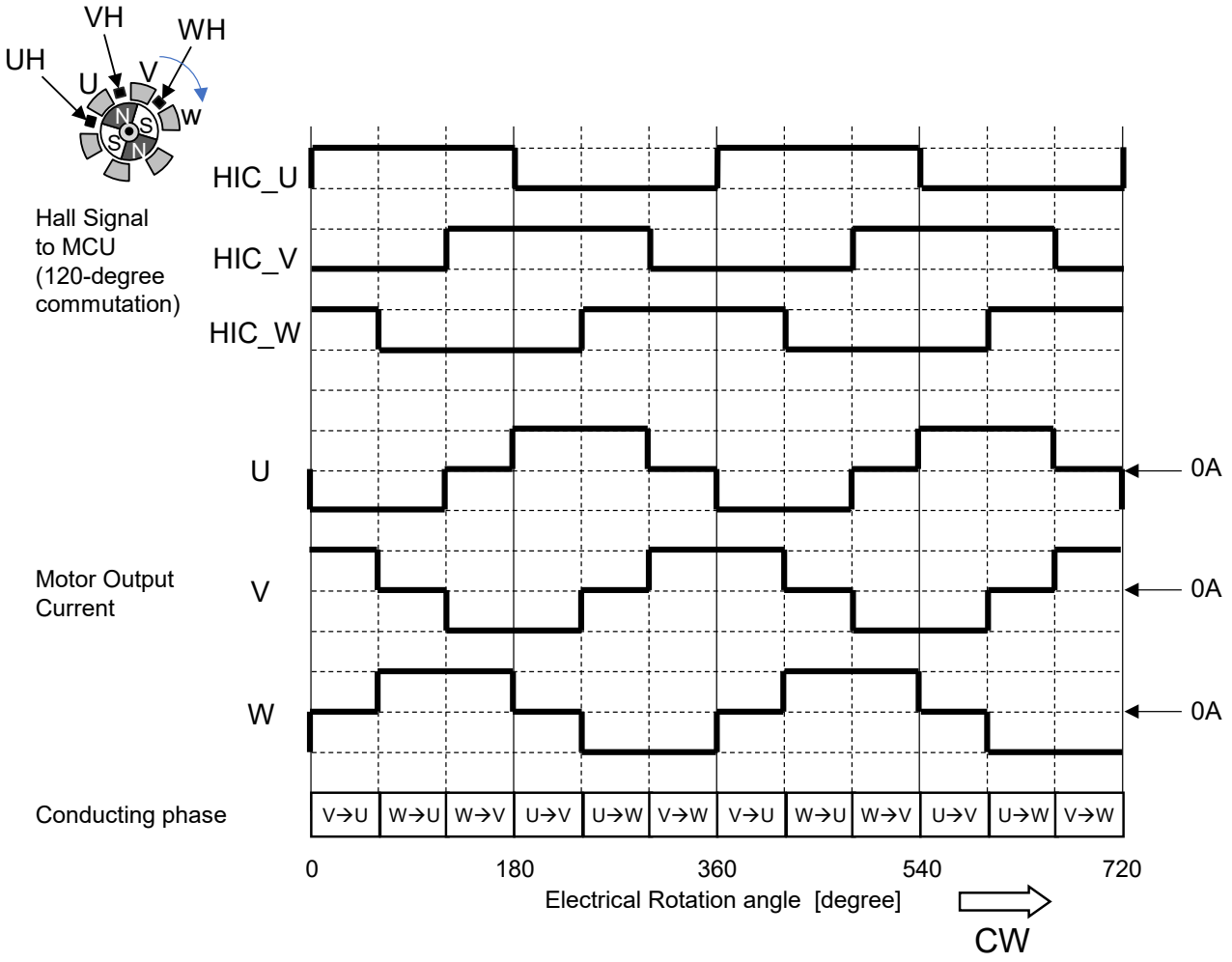
Figure 1-5 shows recommended waveform of Hall-IC signal at HIC* and driving current when using Hall-IC.

Pre-Driver in this IC control the function of commutation drive mode.

Then using these functions, set this relationship of recommended drive waveform by using registers of SELSIG_U, SELSIG_V, SELSIG_W and HALL_SIG.

When not using the abovementioned function, there is no need to follow this recommended waveform.

Figure 1-5 recommended drive waveform



1.5 How to select the external MOSFET

The selection method of the external MOSFET is described.

When using the dead time adjustment function, it is necessary to use an external MOSFET that satisfies the following condition. If an external MOSFET that does not satisfy the following conditions is used, the external MOSFET may be destroyed by the through current. And when using auto deadtime adjust function, Renesas recommends not to insert the resistance on gate line of External Drive MOS. The reason is followings.

<R>
- By inserting the resistance, the signal delay is occurred on the node at before and after the resistance. By this delay, dead time auto adjust function cannot operate to External Drive MOS.

And by inserting the resistance, the impedance to fix Lo on gate node is also decreased. By decreasing impedance, “Self Turn On” phenomenon would be easily occurred and become potential high to generate through current.

Detail description of the dead time adjustment function is described in “2.5.1.1 Dead time auto adjust function”.

For the external MOSFET with the condition of “Vt_monitor> Vt_power”, fall time is calculated using the following equation and it needs the calculation result satisfies “t = <30 nsec”.

When external MOSFETs satisfy the condition “Vt_monitor =< Vt_power”, there are no restrictions.

$$t = -C \times R \times \ln\left(\frac{Vt\_power}{Vt\_monitor}\right)$$

Vt_monitor :Threshold voltage of MOSFET Vgs monitor circuit
Vt_power :External MOSFET threshold voltage
C :External MOSFET gate capacitance (Refer to the MOSFET data sheet)
R:Low side output impedance
(Refer to the gate drive output impedance in the device characteristics reference data of the RAJ306000 series data sheet.)

Even if condition is satisfied, Renesas recommends evaluating sufficiently to select the external MOSFET, especially through current.

Showing a setting example below
Vt_monitor :Threshold voltage of MOSFET Vgs monitor circuit = 1.0 V
Vt_power :External MOSFET threshold voltage = 0.8 V
C:External MOSFET gate capacitance= 4000 pF
R:Low side output impedance = 20 Ω
(From the device characteristic reference data of the data sheet of RAJ306000 series)

In case of calculation with the above reference value

$$t = -4000\text{pF} \times 20 \times \ln\left(\frac{0.8}{1.0}\right) = 17.85nsec$$

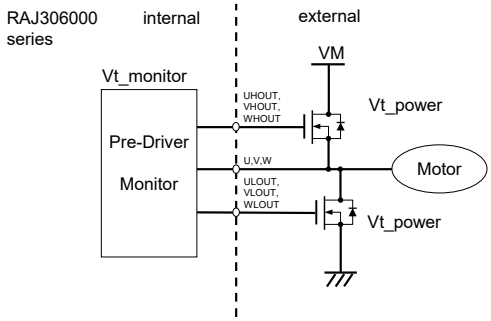
This satisfies t = <30 nsec.

In the case of Vt_power = 0.6 V,

$$t = -4000\text{pF} \times 20 \times \ln\left(\frac{0.6}{1.0}\right) = 40.87nsec$$

This does not satisfy t = <30 nsec.

Figure 1-6 Connection diagram of external MOSFET



CHAPTER 2 Pre-Driver

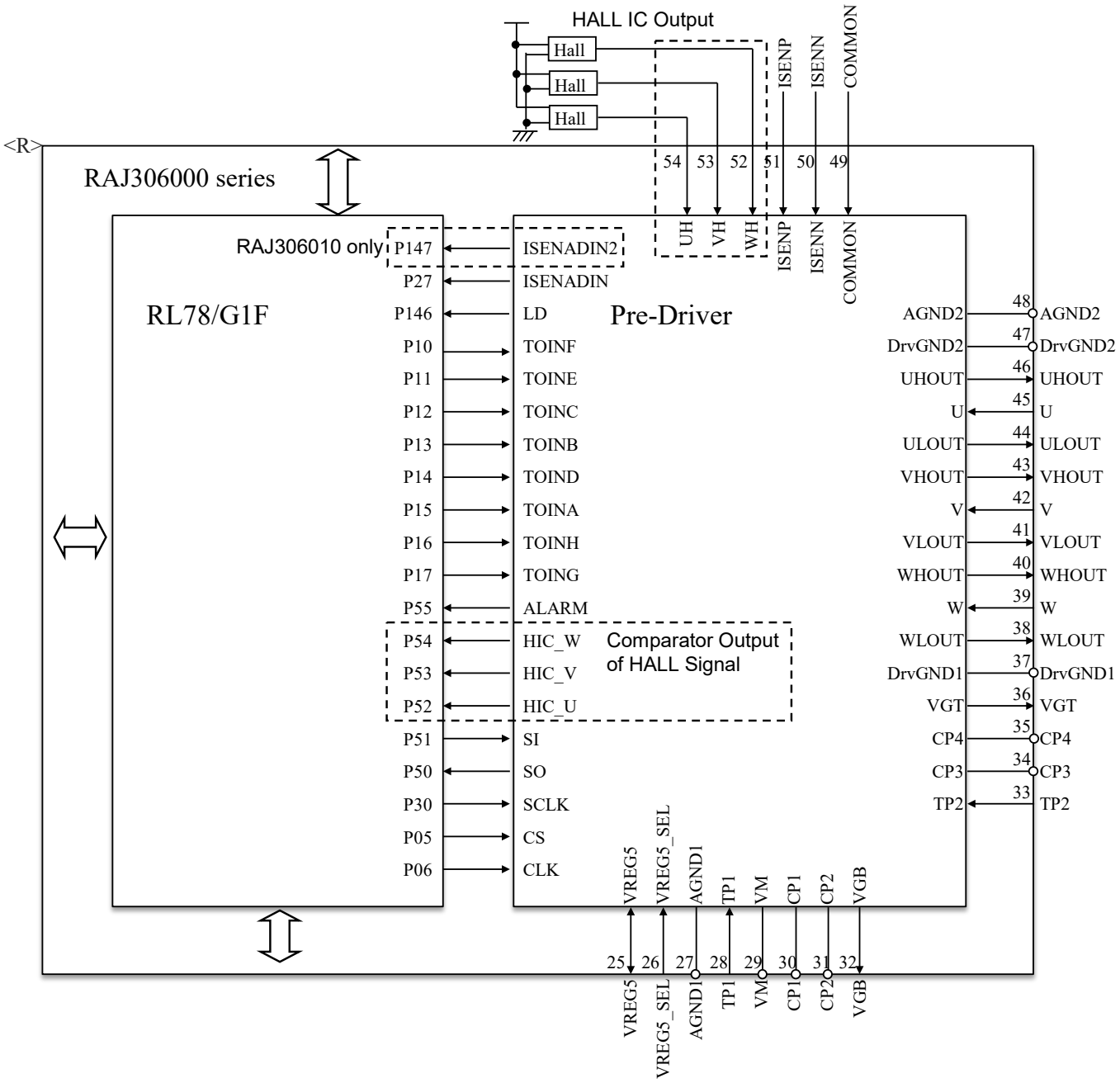
2.1 Terminal configuration of Pre-Driver.

2.1.1 The terminal connection of Pre-Driver

2.1.1.1 The connection when using HALL_IC

When HALL_IC is connected, please set to 0 (HALL_IC control: initial value) at the HALL_MODE_SEL bit of the HALL_SIG register. Signals of UH, VH, WH are outputted from HIC_U, HIC_V, HIC_W via Hall IC comparator.

Figure 2-1 Pre-Driver terminal configuration for Hall-IC based control



2.1.1.2 The connection of sensor-less mode

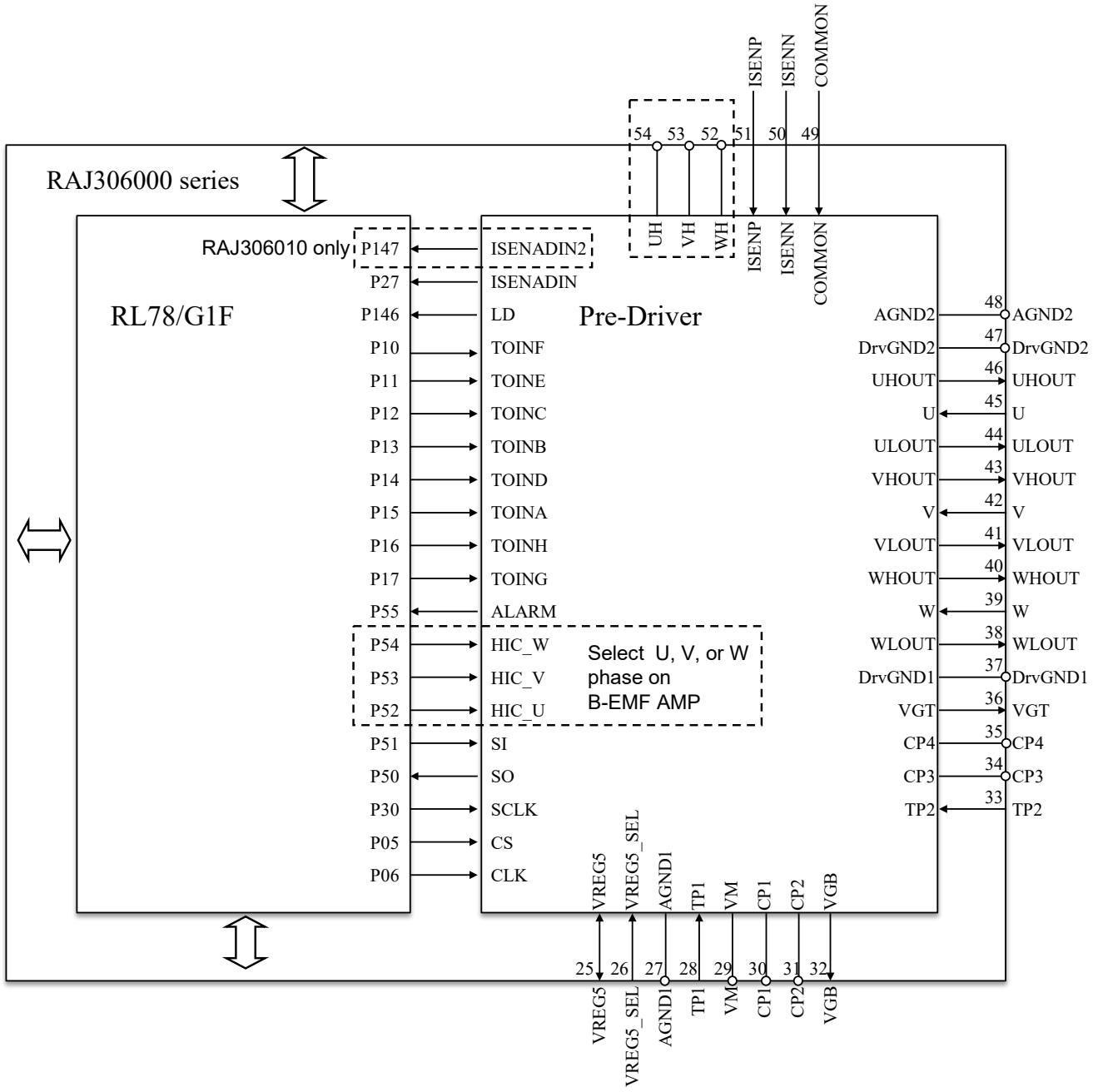
When controlling using the sensor-less mode, please set to1 (sensor-less control) at the HALL_MODE_SEL bit of the HALL_SIG register.

The phase that measures the back-EMF voltage can be selected by controlling P52, P53 and P54. which is the output terminal of GPIO,

When controlling in sensorless mode using RAJ306001, UH, VH, and WH terminals are pulled down by built-in resistors. If not used, open or connect to GND.

When controlling in sensorless mode using RAJ306010, there is a function to output BEMF amplifier output from WH terminal. When using this function, do not connect WH pin to GND.

Figure 2-2 Pre-Driver terminal configuration for sensor-less



2.1.2 Pre-Driver terminal table

Table 2-1 shows the Pre-Driver external pins.

Table 2-2 shows the internal pins of the pre-driver internally connected to the RL78/G1F.

Table 2-1 Pre-Driver external pins.

PIN		I/O level	IN/OUT or Power/GND	Initial Condition	Function
Number	Name				
25	VREG5	5V	IN/OUT	IN/OUT	Function of VREG5 pin is depends on VREG5_SEL pin level VREG5_SEL=GND:Built-in 5V regulator is selected. (Output 5V) VREG5_SEL=5V:External 5V regulator is selected (Input 5V)
26	VREG5_SEL	VDD	IN	IN	
27	AGND1	GND	GND	GND	Ground potential for analog and logic circuits of Pre-Driver.
28	TP1	VDD	IN	IN	Terminal for Test. (Usually conect to GND via resistance.)
29	VM	VM	Power	Power	Power Supply
30	CP1	VGB	-	-	Charge pump flying capacitor for VGB (CP1)
31	CP2	VGB	-	-	Charge pump flying capacitor for VGB (CP2)
32	VGB	VGB	OUT	OUT	Gate drive voltage for Low-side
33	TP2	5V	IN	IN	Terminal for Test. (Usually conect to GND)
34	CP3	VM	-	-	Charge pump flying capacitor for VGT (CP3)
35	CP4	VGT	-	-	Charge pump flying capacitor for VGT (CP4)
36	VGT	VGT	OUT	OUT	Gate drive voltage for High-side
37	DrvGND1	GND	GND	GND	Ground potential for driving circuits of Pre-Driver.
38	WLOUT	VGB	OUT	OUT	Output of Pre-driver for W phase Low-side (Nch MOSFET).
39	W	VM	IN	IN	W phase voltage.
40	WHOUT	VGT	OUT	OUT	Output of Pre-driver for W phase High-side (Nch MOSFET).
41	VLOUT	VGB	OUT	OUT	Output of Pre-driver for V phase Low-side (Nch MOSFET).
42	V	VM	IN	IN	V phase voltage.
43	VHOUT	VGT	OUT	OUT	Output of Pre-driver for V phase High-side (Nch MOSFET).
44	ULOUT	VGB	OUT	OUT	Output of Pre-driver for U phase Low-side (Nch MOSFET).
45	U	VM	IN	IN	U phase voltage.
46	UHOUT	VGT	OUT	OUT	Output of Pre-driver for U phase High-side (Nch MOSFET).
47	DrvGND2	GND	GND	GND	Ground potential for driving circuits of Pre-Driver.
48	AGND2	GND	GND	GND	Ground potential for analog and logic circuits of Pre-Driver.
49	COMMON	VM	IN	IN	Input for Common signal of Motor.
50	ISENN	5V	IN	IN	Connect Negative side of Shunt resistor.
51	ISENP	5V	IN	IN	Connect Positive side of Shunt resistor.
52	WH	5V	IN	IN	RAJ306001:Input of Hall IC signal for W phase
			IN/OUT	IN	RAJ306010:Input of Hall IC signal for W phase. Output of BEFM amplifier signal.
53	VH	5V	IN	IN	Input of Hall IC signal for V phase
54	UH	5V	IN	IN	Input of Hall IC signal for U phase

Table 2-2 Pre-Driver internal pins.

PIN Name	I/O level	IN/OUT or Power/GND	Function
ISENADIN2	Analog	OUT	RAJ306010 only:Output analog signal of current sense amplifier(P147).
ISENADIN	Analog	OUT	Output analog signal of selected by ADC_SEL register to ANI17(P27).
LD	Digital	OUT	Output moter lock status to P147 pin.
TOINF	Digital	IN	Input of PWM pulse from TRDIOD1(P10) pin.
TOINE	Digital	IN	Input of PWM pulse from TRDIOC1(P11) pin.
TOINC	Digital	IN	Input of PWM pulse from TRDIOB1(P12) pin.
TOINB	Digital	IN	Input of PWM pulse from TRDIOA1(P13) pin.
TOIND	Digital	IN	Input of PWM pulse from TRDIOD0(P14) pin.
TOINA	Digital	IN	Input of PWM pulse from TRDIOB0(P15) pin.
TOINH	Digital	IN	Input of PWM pulse from TRDIOC0(P16) pin.
TOING	Digital	IN	Input of PWM pulse from TRDIOA0(P17) pin.
ALARM	Digital	OUT	Output ALARM pulse to INTP4(P55) pin.
HIC_W	Digital	IN/OUT	Function of HIC_W depends on HALL_MODE_SEL bit. 0:Select hall-comparator W phase output tp INTP3(P54). 1:Select W phase BEMF measurement instruction signal input for sensor-less from P54.
HIC_V	Digital	IN/OUT	Function of HIC_V depends on HALL_MODE_SEL bit. 0:Select hall-comparator V phase output tp INTP2(P53). 1:Select V phase BEMF measurement instruction signal input for sensor-less from P53
HIC_U	Digital	IN/OUT	Function of HIC_U depends on HALL_MODE_SEL bit. 0:Select hall-comparator V phase output tp INTP1(P52). 1:Select V phase BEMF measurement instruction signal input for sensor-less from P52
SI	Digital	IN	4Line-SPI:Input data from SO00(P51) pin as CSI00.
SO	Digital	OUT	4Line-SPI:Output data to SI00(P50) pin as CSI00. Set on-chip pull-up enable in RL78/G1F.
SCLK	Digital	IN	4Line-SPI::Output communication clk[1MHz] to SCK00(P30) pin as CSI00.
CS	Digital	IN	4Line-SPI:Input chip select signal from P05 pin.H;Not selected,L:Selected.
CLK	Digital	IN	Input system clock[4MHz] from TRJIO0(P06).

2.2 System clock of Pre-Driver

In order to use the Pre-Driver of this IC, it is necessary to supply the system clock by using the pulse output function of the I/O setting and timer RJ of RL78/G1F.

1. I/O setting
   Peripheral I/O redirection register 1 (PIOR1): Set to 0BH [PIOR13,12,11,10]= [1, 0, 1, 1]
   Target pin: RL78/G1F P06 is selected as TRJIO0
   P06 is internally connected to the CLK pin of the pre-driver.
2. Timer RJ
   Operation mode: Pulse output mode.
   Cycle setting: Set the timer RJ counter register 0 (TRJ0) to 125ns. The output is inverted every 125ns.
   As a result, a signal with a cycle of 250 ns (4 MHz) is output to the Pre-Driver as a clock.

The Pre-Driver has a clock stop detection function and switches to the power save mode when it is determined that the clock has not been input.

The internal interface terminals are changed as shown in Table 2-3 shows the Pre-Driver pin states and recommended settings for the MCU pins when the clock is stopped. When stopping the Pre-Driver to save power, change the MCU pin processing while the clock is stopped.

Also, if the following register settings of the pre-driver are set to 1 at the start of clock re-supply, a charge pump related status error may be detected. Set these bits to 0 before stopping the clock.

1. MOT_EN bit of motor drive control setting register,
2. PS_CPREG_N, PS_CP_N bits in the power save control setting register for each function

Table 2-3 Internal terminal state when clock supply is stopped

<R>

PreDriver		RL78/G1F	
PIN	Level	PIN	Recommended pin processing
ISENADIN	Hi-Z	P27/ANI7	Set output pin and output low level.
ISENADIN2 Note 1	Hi-Z	P147/ANI18	Please select either setting ●Set Output low level ●Set input pin and internal pull-up.
LD	Pull-down	P146	Set input pin.
TOINF	Pull-down	P10	Set output pin and output low level.
TOINE	Pull-down	P11	
TOINC	Pull-down	P12	
TOINB	Pull-down	P13	
TOIND	Pull-down	P14	
TOINA	Pull-down	P15	
TOINH	Pull-down	P16	
TOING	Pull-down	P17	
ALARM	Pull-down	P55	Set input pin.
HIC_W	Pull-down	P54	Set output pin and output low level.
HIC_V	Pull-down	P53	
HIC_U	Pull-down	P52	
SI	Pull-down	P51	
SO	Hi-Z	P50	
SCLK	Pull-down	P30	
CS	Pull-down	P05	
CLK	Pull-down	P06	

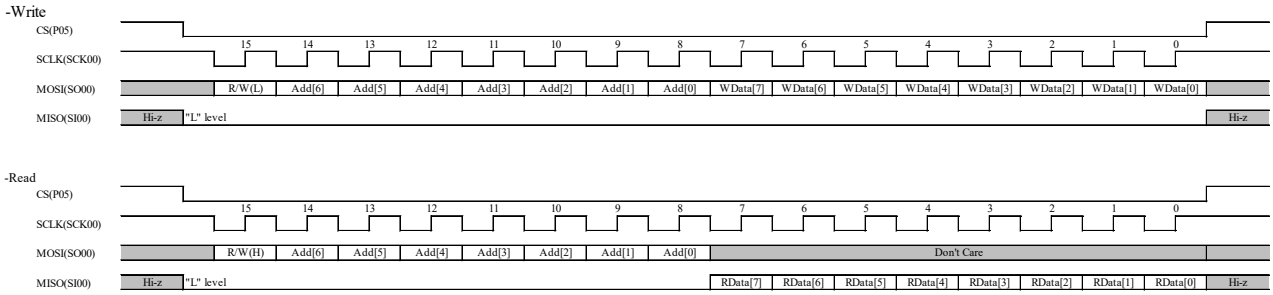
Note 1 ISENADIN2 is RAJ306010 only. In case of RAJ306001, regardless of the power save status, please process the terminals when stopped.
*Perform port switching processing while the clock is stopped.

2.3 Communication format

When setting Pre-Driver register, use 1MHz 4-Line SPI communication by using CSI00 (SCK00, SO00, SI00) and P05 (CS) pin. Output the CS signal is by using GPIO of P05.

Figure 2-3 Shows Communication format. SPI communication is denied when not satisfy the format.

Figure 2-3 Communication format



2.4 Pre-Driver register

The register map is shown in Table 2-4.

- The column “b14-8” means the address of each registers. Set value to 14-8 bit in SPI communication.
- “0” and “1” mean initial value for each bit after reset. For these registers, Set to these values at writing.

<R>

Table 2-4 register map

Register Name	Symbol	After Reset	R/W	b14-8	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
-	-	-	-	00h	0	0	0	0	0	0	0	0
Power Save Control	PS_ALL	00h	R/W	02h	0	0	0	0	0	0	0	PS_ALL_N
By Function Power Control Setting	PS	00h	R/W	04h	PS_PRE_N	0	PS_BEMF_N	PS_CSAMP_N	PS_VMC_N	PS_HALL_N	PS_CPREG_N	PS_CP_N
Software Reset	SW_RESET	00h	R/W	06h	0	0	0	0	0	0	0	SW_RESET
ADC Selector	ADC_SEL	00h	R/W	08h	0	0	0	0	ADC_CH_SEL3 - ADC_CH_SEL0			
U Phase Motor Control Signal Select	SELSIG_U	03h	R/W	0Ah	0	SELSIG_U_H2 - SELSIG_U_H0			0	SELSIG_U_L2 -SELSIG_U_L0		
V Phase Motor Control Signal Select	SELSIG_V	14h	R/W	0Ch	0	SELSIG_V_H2 - SELSIG_V_H0			0	SELSIG_V_L2 - SELSIG_V_L0		
W Phase Motor Control Signal Select	SELSIG_W	25h	R/W	0Eh	0	SELSIG_W_H2 - SELSIG_W_H0			0	SELSIG_W_L2 - SELSIG_W_L0		
Hall Signla Processign Setting	HALL_SIG	00h	R/W	10h	BEMF_MODE_SEL	CENTERTAP_SEL	HALL_MODE_SEL	PWM_SEL	HALL_POLA	HALL_SEL2 - HALL_SEL0		
ALARM Status 1	ALMSTS1	FFh	R	12h	VREG5_OVP_N	VGT_OVP1_N	VGT_OVP2_N	VGT_UVP_N	VGB_OVP_N	VGB_UVP_N	OCP_N	TSD_N
ALARM Operation Setting 1	ALMOPE1	00h	R/W	14h	0	0	0	VGT_UVP_OPE_N	0	VGB_UVP_OPE_N	OCP_OPE_N	TSD_OPE_N
ALARM Pin Output Setting 1	ALMOUT1	00h	R/W	16h	VREG5_OVP_ALE_N	VGT_OVP1_ALE_N	VGT_OVP2_ALE_N	VGT_UVP_ALE_N	VGB_OVP_ALE_N	VGB_UVP_ALE_N	OCP_ALE_N	TSD_ALE_N
ALARM Status 2	ALMSTS2	FFh	R	18h	1	1	1	1	1	1	1	VM_UVP_N
Current Sense setting 2	CS_SET2	00h	R/W	1Ah	CSAMP_IREF1, 0		CSAMP_ATT	0	0	0	0	0
ALARM Pin Output Setting 2	ALMOUT2	00h	R/W	1Ch	0	0	0	0	0	0	0	VM_UVP_ALE_N
Error Detection Wait Time Setting	ERROR_WAIT	00h	R/W	1Eh	0	0	0	VREG5_OVP_WAIT	UVCP_WAIT1, 0		OCP_WAIT1, 0	
Current Sense setting 1	CS_SET1	00h	R/W	20h	0	SHUNT_SEL2 - SHUNT_SEL0			OCP_SEL_H3 - OCP_SEL_H0			
Hall IC Threshold Adjustment	HAIC_TH	00h	R/W	22h	0	0	HAIC_HYS1 - HAIC_HYS0		0	HAIC_TH2 - HAIC_TH0		
Pre-Driver Drive Status	PDDSTS	F0h	R	24h	1	1	1	LDS_N	FG	HALLMON_U	HALLMON_V	HALLMON_W
LD Judgment Wait Time	LD_WAIT	00h	R/W	26h	LD_ALE_N	0	0	0	0	LD_WAIT2 - LD_WAIT0		
Motor Drive Control Setting	DRIVE_SET	00h	R/W	28h	OCP_HYS_N	ALM_LATCH_CLR	0	DECAY_MODE_SEL	DT_REG_N	OCP_ERR_SEL	DIR_SEL	MOT_EN
-	-	-	-	2Ah	0	0	0	0	0	0	0	0
High Side Output Current Capability Setting	IDRCNT_H	00h	R/W	2Ch	0	IDR_H_P2 - IDR_H_P0			0	IDR_H_N2 - IDR_H_N0		
Low Side Output Current Capability Setting	IDRCNT_L	00h	R/W	2Eh	0	IDR_L_P2 - IDR_L_P0			0	IDR_L_N2 - IDR_L_N0		
Pch Slew Rate Setting	TRCNT_P	00h	R/W	30h	0	TR_H_P2 - TR_H_P0			0	TR_L_P2 - TR_L_P0		
Charge Pump Setting 1	CPSET1	01h	R/W	32h	0	0	0	0	0	0	CP_CLK_DIV1, 0	
Charge Pump Setting 2	CPSET2	02h	R/W	34h	0	0	0	0	CP_BOOST_N	VREG10_OUT	VREG6P5_OUT	0
Charge Pump Trimming	CP_TRIM	00h	R/W	36h	CP_TRIM_7 - CP_TRIM_0							
-	-	-	-	38h-3Eh	0	0	0	0	0	0	0	0
5V Regulator Voltage Setting	VREG5_TRIM	00h	R/W	40h	VREG5_TRIM_7 - VREG5_TRIM_0							
Ext. FET Current Detect AMP Setting	CSAMP_TRIM	00h	R/W	42h	CSAMP_TRIM_7 - CSAMP_TRIM_0							
-	-	-	-	44h-56h	0	0	0	0	0	0	0	0
ALAM Raw Status Monitor	ALMRAW1	FFh	R	58h	1	VGT_OVP1_RAW_N	VGT_OVP2_RAW_N	VGT_UVP_RAW_N	VGB_OVP_RAW_N	VGB_UVP_RAW_N	1	1
-	-	-	-	5Ah	0	0	0	0	0	0	0	0
TOIN Pin Monitor	TOIN_MONI	-	R	5Ch	TOINA	TOINB	TOINC	TOIND	TOINE	TOINF	TOING	TOINH
WHO AM I	WHO_AM_I	*1	R	5Eh	WHO_AM_I_7 - WHO_AM_I_0							
Trimming Protect	TRIM_PT	00h	R/W	60h	TRIM_PT_7 - TRIM_PT_0							
-	-	-	-	62h-72h	0	0	0	0	0	0	0	0
Triming Data Valid	TRIM_EN	00h	R/W	74h	0	0	0	0	0	0	0	TRIM_EN
-	-	-	-	76h	0	0	0	0	0	0	0	0
High Precise BGR Temp. Correction	BGR_TRIM	xxh	R/W	78h	BGR_TRIM_7 - BGR_TRIM_0							
BUFF AMP Absolute Value Correction	BFAMP_TRIM	xxh	R/W	7Ah	BFAMP_TRIM_7 - BFAMP_TRIM_0							
-	-	-	-	7Ch-7Eh	0	0	0	0	0	0	0	0

*.1 The value of the WHO_AM_I register depends on the product.
RAJ306001: 6Ah, RAJ06010: 6Bh

2.4.1 Power Save Control Register (PS_ALL)

<R> PS_ALL is a register that controls the power saving of the pre-driver.

The setting of "0" to PS_ALL_N bit, the power saving mode for the entire pre-driver is entered.

The setting of "1" to PS_ALL_N bit, power save settings for each function block enables the setting of the power save control setting register (PS) will be possible.

However, the following functions are not saved regardless of the setting of this register.

- Thermal shutdown (TSD) detection function
- 5V regulator

Changing the setting of this register is prohibited during motor rotation control. (MOT_EN bit = 1).

Table 2-5 Format of power save control register (PS_ALL)

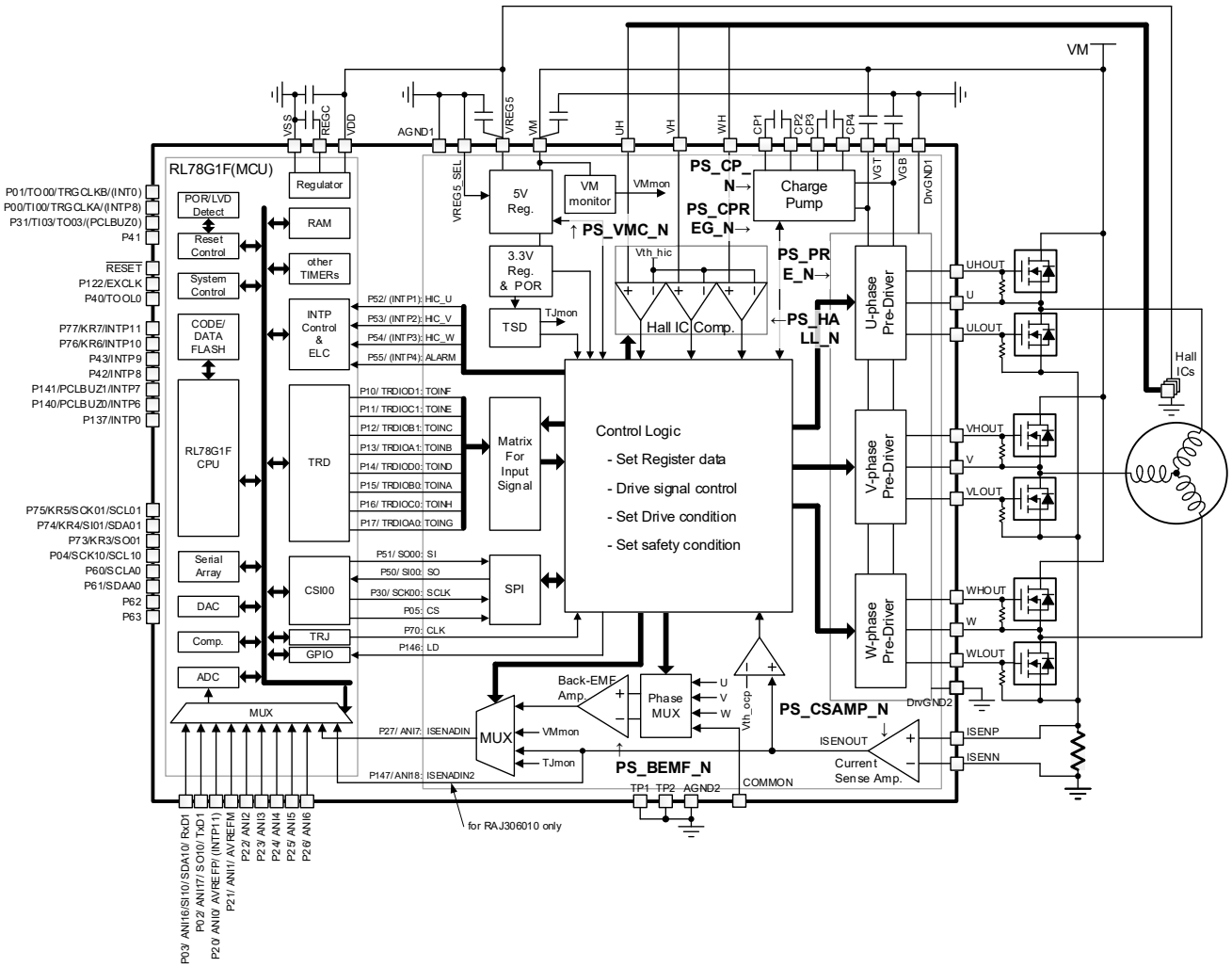
Address: 02h After reset: 00h R/W

Symbol	7	6	5	4	3	2	1	0
PS_ALL	0	0	0	0	0	0	0	PS_ALL_N

PS_ALL_N	Power save for common circuit and by function power save.
0	Power save for chip is effective.
1	Power save for chip is invalid.(By function power save control are available by PS register)
When this bit is 0, Regardless of the PS register setting, power save of all circuit excluding TSD are valid.	

Figure 2-4 Block controlled by PS register

<R>



2.4.2 Power Save Control Setting Register by function (PS)

PS is a register to set the effective or invalid for the power save on each block function of Pre-driver.

Power saving for each function with this bit can reduce power consumption.

The setting change of this register is prohibited when driving the motor (MOT_EN bit = 1).

Table 2-6 Format of power saving control setting register (PS) by function

Address: 04h Reset: 00h R/W

Symbol	7	6	5	4	3	2	1	0
PS	PS_PRE_N	0	PS_BEMF_N	PS_CSAMP_N	PS_VMC_N	PS_HALL_N	PS_CPREG_N	PS_CP_N

PS_PRE_N	Power-save control for the Pre-driver block.
0	Power-save is effective.
1	Power save is invalid.
When PS_ALL_N bit is 0, Power save invalidity function is invalid.	

PS_BEMF_N	Power-save control for the BEMF detection block.
0	Power-save is effective.
1	Power save is invalid.
When PS_ALL_N bit is 0, Power save invalidity function is invalid.	

PS_CSAMP_N	Power-save control for the Current sense Amp block.
0	Power-save is effective.
1	Power save is invalid.
When PS_ALL_N bit is 0, Power save invalidity function is invalid.	

PS_VMC_N	Power-save control of Comparator for the detection of VM pin voltage.
0	Power-save is effective.
1	Power save is invalid.
When PS_ALL_N bit is 0, Power save invalidity function is invalid.	

PS_HALL_N	Power-save control of Comparator for the connection of Hall IC (U,V,W).
0	Power-save is effective.
1	Power save is invalid.
When PS_ALL_N bit is 0, Power save invalidity function is invalid.	

PS_CPREG_N	Power-save control of Regulator block for Charge pump.
0	Power-save is effective.
1	Power save is invalid.
When PS_ALL_N bit is 0, Power save invalidity function is invalid.	

PS_CP_N	Power-save control for Charge-pump block.
0	Power-save is effective.
1	Power save is invalid.
When PS_ALL_N bit is 0, Power save invalidity function is invalid.	

2.4.3 Software Reset Register (SW_RESET)

SW_RESET is a register to set the initialization operation of the register data in the pre-driver.

By setting "1" to this register, the register of the pre-driver is reset.

Since this register is not software reset. Set the "0" to release the reset state.

Table 2-7 Format of software reset register (SW_RESET)

Address: 06h Reset: 00h R/W

Symbol	7	6	5	4	3	2	1	0
SW_RES	0	0	0	0	0	0	0	SW_RESET0

SW_RESET0	Software reset for Pre-Driver register.
0	Normal operation.
1	Register data are initialized.

2.4.4 ADC Selector Register (ADC_SEL)

This register switches the analog output to be output from the ISENADIN pin of the pre-driver to the ANI7 pin of RL78/G1F. After the channel change to start the AD conversion, in order for the necessary wait time more than 1us for the AMP response. The output of the AD value to ANI7 is valid only when PS_ALL = 1.

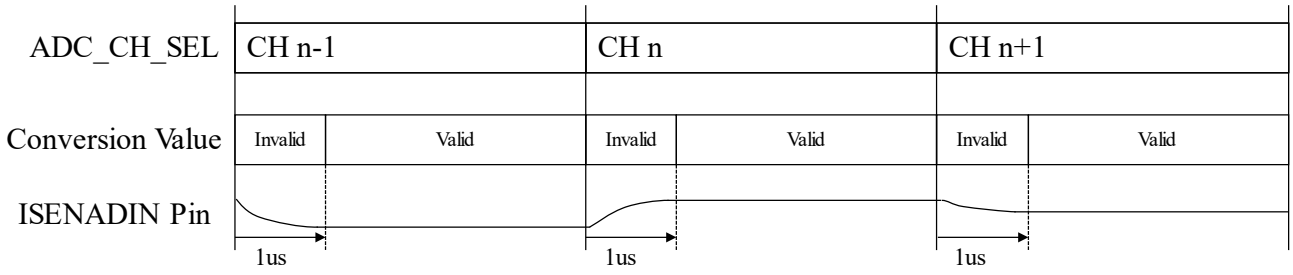
Table 2-8 Format of ADC selector register (ADC_SEL)

Address: 08h Reset: 00h R/W

Symbol	7	6	5	4	3	2	1	0
ADC_SEL	0	0	0	0	ADC_CH_SEL3	ADC_CH_SEL2	ADC_CH_SEL1	ADC_CH_SEL0

ADC_CH_SEL3	ADC_CH_SEL2	ADC_CH_SEL1	ADC_CH_SEL0	Select function for AD conversion.
0	0	0	0	Detection of VM voltage level(VMC).
0	0	0	1	Detection of the current level(ISENSE).
0	0	1	0	Detection of chip temperature level.(TSD)
0	0	1	1	Detection of BEMF AMP output level.
Other than above.				Setting prohibited.

Figure 2-5 ADC sampling timing



2.4.5 U/V/W Phase Motor Control Signal Select Register (SELSIG_U/V/W)

This register selects the PWM signal input from RL78/G1F for driving U phase.

This register is valid by setting 1 to the PWM_SEL bit in the HALL_SIG register when the MOT_EN bit of the DRIVE_SET register is "0".

The setting change of this register is invalid when driving the motor (MOT_EN bit = 1).

Table 2-9 Format of U Phase Motor Control Signal Select Register (SELSIG_U)

Addres: 0Ah Reset: 03h R/W

Symbol	7	6	5	4	3	2	1	0
SELSIG_U	0	SELSIG_U_H2	SELSIG_U_H1	SELSIG_U_H0	0	SELSIG_U_L2	SELSIG_U_L1	SELSIG_U_L0

SELSIG_U_H2	SELSIG_U_H1	SELSIG_U_H0	Select U phase high side PWM signal for input pin from RL78/G1F.
0	0	0	TOINA(TRDIOB0)(initial)
0	0	1	TOINB(TRDIOA1)
0	1	0	TOINC(TRDIOB1)
0	1	1	TOIND(TRDIOD0)
1	0	0	TOINE(TRDIOC1)
1	0	1	TOINF(TRDIOD1)
1	1	0	TOING(TRDIOA0)
1	1	1	TOINH(TRDIOC0)

SELSIG_U_L2	SELSIG_U_L1	SELSIG_U_L0	Select U phase low side PWM signal for input pin from RL78/G1F.
0	0	0	TOINA(TRDIOB0)
0	0	1	TOINB(TRDIOA1)
0	1	0	TOINC(TRDIOB1)
0	1	1	TOIND(TRDIOD0)(initial)
1	0	0	TOINE(TRDIOC1)
1	0	1	TOINF(TRDIOD1)
1	1	0	TOING(TRDIOA0)
1	1	1	TOINH(TRDIOC0)

Table 2-10 Format of V Phase Motor Control Signal Select Register (SELSIG_V)

Addres: 0Ch Reset: 14h R/W

Symbol	7	6	5	4	3	2	1	0
SELSIG_V	0	SELSIG_V_H2	SELSIG_V_H1	SELSIG_V_H0	0	SELSIG_V_L2	SELSIG_V_L1	SELSIG_V_L0

SELSIG_V_H2	SELSIG_V_H1	SELSIG_V_H0	Select V phase high side PWM signal for input pin from RL78/G1F.
0	0	0	TOINA(TRDIOB0)
0	0	1	TOINB(TRDIOA1)(initial)
0	1	0	TOINC(TRDIOB1)
0	1	1	TOIND(TRDIOD0)
1	0	0	TOINE(TRDIOC1)
1	0	1	TOINF(TRDIOD1)
1	1	0	TOING(TRDIOA0)
1	1	1	TOINH(TRDIOC0)

SELSIG_V_L2	SELSIG_V_L1	SELSIG_V_L0	Select V phase low side PWM signal for input pin from RL78/G1F.
0	0	0	TOINA(TRDIOB0)
0	0	1	TOINB(TRDIOA1)
0	1	0	TOINC(TRDIOB1)
0	1	1	TOIND(TRDIOD0)
1	0	0	TOINE(TRDIOC1)(initial)
1	0	1	TOINF(TRDIOD1)
1	1	0	TOING(TRDIOA0)
1	1	1	TOINH(TRDIOC0)

Table 2-11 Format of W Phase Motor Control Signal Select Register (SELSIG_W)

Addres: 0Eh Reset: 25h R/W

Symbol	7	6	5	4	3	2	1	0
SELSIG_	0	SELSIG_W_H2	SELSIG_W_H1	SELSIG_W_H0	0	SELSIG_W_L2	SELSIG_W_L1	SELSIG_W_L0

SELSIG_W_H2	SELSIG_W_H1	SELSIG_W_H0	Select W phase high side PWM signal for input pin from RL78/G1F.
0	0	0	TOINA(TRDIOB0)
0	0	1	TOINB(TRDIOA1)
0	1	0	TOINC(TRDIOB1)(initial)
0	1	1	TOIND(TRDIOD0)
1	0	0	TOINE(TRDIOC1)
1	0	1	TOINF(TRDIOD1)
1	1	0	TOING(TRDIOA0)
1	1	1	TOINH(TRDIOC0)

SELSIG_W_L2	SELSIG_W_L1	SELSIG_W_L0	Select W phase low side PWM signal for input pin from RL78/G1F.
0	0	0	TOINA(TRDIOB0)
0	0	1	TOINB(TRDIOA1)
0	1	0	TOINC(TRDIOB1)
0	1	1	TOIND(TRDIOD0)
1	0	0	TOINE(TRDIOC1)
1	0	1	TOINF(TRDIOD1)(initial)
1	1	0	TOING(TRDIOA0)
1	1	1	TOINH(TRDIOC0)

2.4.6 Hall Signal Processing Setting Register (HALL_SIG)

Register to setting for processing of Hall signal of the pre-driver.

The setting modification of this register is prohibited when driving the motor (MOT_EN bit = 1).

The change of the HALL_MODE_SEL bit is prohibited during the Hall power save release (PS_HALL_N bit = 1).

<R>
- BEMF_MODE_SEL bit
  Back electromotive force can be measured using BEMF amplifier.
  Note:RAJ306001 and RAJ306010 have different bit specifications.

- CENTERTAP_SEL bit
  Select whether the midpoint used for back electromotive force measurement is the virtual midpoint (Vn) or the COMMON terminal.

<R>
- HALL_MODE_SEL bit
  Select whether to perform Hall IC control or sensor-less control.
  When sensor-less control is selected, by outputting Hi from P52, P53, and P54 of RL78/G1F, the Pre-Driver internal terminals HIC_U, HIC_V, and HIC_W are controlled, and the non-conducting phase to be measured by BEMF AMP is selected.

- HALL_POLA bit & HALL_SEL bit
  The HALL_IC input signal can be switched by setting the HALL_POLA and HALL_SEL bits.

Table 2-12 Format for Hall Signal Processing Setting Register (HALL_SIG)

Address: 10h After reset: 00h R/W

Symbol	7	6	5	4	3	2	1	0
HALL_SIG	BEMF_MODE_SEL	CENTERTAP_SEL	HALL_MODE_SEL	PWM_SEL	HALL_POLA	HALL_SEL2	HALL_SEL1	HALL_SEL0

BEMF_MODE_SEL	RAJ306001 : Selection of measurement object by BEMF amplifier circuit.
0	Stop BEMF amplifier signal to RL78/G1F P27 (ANI7)
1	Output BEMF amplifier signal to P27 (ANI7) of RL78/G1F(At the same time, ADC_CH_SEL=3 must be set.)
BEMF_MODE_SEL	RAJ306010:Selection of measurement object by BEMF amplifier circuit.
0	Stop BEMF amplifier signal to the WH terminal. Output BEMF amplifier signal to P27 (ANI7) of RL78/G1F(At the same time, ADC_CH_SEL=3 must be set.)
1	Output BEMF amplifier signal to WH terminal. Output BEMF amplifier signal to P27 (ANI7) of RL78/G1F(At the same time, ADC_CH_SEL=3 must be set.)
When use this function, Power save invalidity is need by set 1 to PS_BEMF_N bit. RAJ306001 and RAJ306010 have different functions. Notes on using RAJ306010. (1)When using the Hall-IC comparator, set the BEMF_MODE_SEL bit to “0”. (2)Output to P27 (ANI7) of RL78/G1F of BEMF amplifier is possible by setting only ADC_CH_SEL bit to 3 regardless of BEMF_MODE_SEL bit.	

CENTERTAP_SEL	Select COMMON signal, when measurement of BEMF voltage for sensor-less motor control.
0	Select virtual center tap as moter center tap.
1	Select common signal as moter center tap.

HALL_MODE_SEL	Celect moter driving method.
0	Hall-IC driving method(Pre-Driver side: output, RL78/G1F side : input)
1	Sensor-less driving method(RL78/G1F side:output ,Pre-Driver side: input)
Switch pre-driver side pin function input or output, according to the control method. When switch driving method from Hall-Ic to sensor-less,Set 0 to PS_HALL_N and output low from RL78/G1F pin before chage this bit value. When select sensor-less driving method,the phase to be measured by the BEMF amplifier is specified by outputting the high level from RL78/G1F port function.Simultaneous selection of multiple phases is prohibited. By the H output from the RL78 / G1F of the side port, you can select the phase to be measured by the BEMF. Termina object: Pre-Driver RL78/G1F HIC_U: P.52 / INTP1 HIC_V: P.53 / INTP2 HIC_W: P.54 / INTP3 When a sensor-less function is select, the following function is not available. -Output function of FG signal -Commutation mode of motor control -Detection function of motor lock	

PWM_SEL	Trigger signal for port setting of signal for motor control.
0	Keep the port setting.
1	Switch port connection by each moter control signal select register(SELSIG_U, SELSIG_V, SELSIG_W).
This bit automatically returns to 0. The change is applied only when MOT_EN bit is "0".If MOT_EN bit is "1" the setting is Ignored.	

HALL_POLA	Inversion of Hall IC input signal.					
0	Not inversion					
1	Inversion					
HALL_SEL2	HALL_SEL1	HALL_SEL0	Switch Hall IC signal connection internally			Note
			UtoV	VtoH	WToU	
0	0	0	UH pin	VH pin	WH pin	
0	0	1	UH pin	WH pin	VH pin	
0	1	0	VH pin	UH pin	WH pin	
0	1	1	VH pin	WH pin	UH pin	
1	0	0	UH pin	UH pin	VH pin	
1	0	1	UH pin	VH pin	UH pin	
Other than above.			Setting prohibited.			
With these bits, it is possible to switch the polarity and input order of the signals input from the UH, VH, and WH terminals and output them to the RL78/G1B3:AJ41F and internal logic (commutation function). When using the internal logic, input according to the recommended drive waveforms in section 1.4 is required. If the input Hall signal matches the recommended drive waveform, switch the Hall IC waveform.						

2.4.7 ALARM Status Register1 (ALMSTS1)

This register stores the abnormal state detected by the pre-driver. The abnormal state detection function is enabled after release the power save of the analog block corresponding to the abnormal state."1" is the abnormal undetected state, "0" is the anomaly detection state. The bits for corresponding to each factor changes from "1" to "0" after detection abnormal. The status is retained until reading the register, and these are updated to the latest information at the time.

However, the protection functions against overcurrent detection (OCP), and charge pump undervoltage (VGB_UVP, VGT_UVP) are retained until the ALM_LATCH_CLR bit in the DRIVE_SET register is set to "1", even if the register value changes from "0" to "1" by reading the register.

<R>

Table 2-13 Format of ALARM Status Register1 (ALMSTS1)

Address 12h After reset: FFh R/W

Symbol	7	6	5	4	3	2	1	0
ALMSTS1	VREG5_OVP_N	VGT_OVP1_N	VGT_OVP2_N	VGT_UVP_N	VGB_OVP_N	VGB_UVP_N	OCP_N	TSD_N

VREG5_OVP_N	Detection of abnormal over voltage at 5V Regulator.
0	Detect abnormal voltage.
1	Not detect abnormal voltage.
The threshold of the detection by ALARM VREG5 => 5.7V (typical) Error detection wait time can be set in VREG5_OVP_WAIT bit of ERROR_WAIT register..	

VGT_OVP1_N	Detection of abnormal over voltage at the charge pump (VGT terminal) 1.
0	Detect abnormal voltage.
1	Not detect abnormal voltage.
The threshold of the detection by ALARM VGT => VM voltage + 18V (typical) The threshold for the cancellation of ALARM. VGT < VM voltage + 17V (typical) This protection is effective in all of PS_ALL_N bit,PS_CP_REG_N bit,PS_CP_N bit and MOT_EN bit are 1. Watch ALMRAW1register, When MOT_EN bit is 0.	

VGT_OVP2_N	Detection of abnormal over voltage at the charge pump (VGT terminal) 2.
0	Detect abnormal voltage.
1	Not detect abnormal voltage.
The threshold of the detection by ALARM RAJ306001 : VGT => 48V , RAJ306010 : VGT => 60V (typical) The threshold for the cancellation of ALARM. RAJ306001 : VGT < 47V , RAJ306010 : VGT < 59V (typical) This protection is effective in all of PS_ALL_N bit,PS_CP_REG_N bit,PS_CP_N bit and MOT_EN bit are 1. Watch ALMRAW1register, When MOT_EN bit is 0.	

VGT_UVP_N	Detection of abnormal under voltage at the charge pump (VGT terminal).
0	Detect abnormal voltage.
1	Not detect abnormal voltage.
The threshold of the detection by ALARM VGT =< VM voltage + 7V (typical) The threshold for the cancellation of ALARM. VGT >VM voltage + 7.5V (typical) Error detection wait time can be set in UVCP_WAIT bit of ERROR_WAIT register.. This protection is effective in all of PS_ALL_N bit,PS_CP_REG_N bit,PS_CP_N bit and MOT_EN bit are 1. Watch ALMRAW1register, When MOT_EN bit is 0.	

VGB_OVP_N	Detection of abnormal over voltage at the charge pump (VGB terminal).
0	Detect abnormal voltage.
1	Not detect abnormal voltage.
The threshold of the detection by ALARM VGB => 18V (typical) The threshold for the cancellation of ALARM. VGB < 17V (typical) This protection is effective in all of PS_ALL_N bit,PS_CP_REG bit,PS_CP bit and MOT_EN bit are 1. Watch ALMRAW1register, When MOT_EN bit is 0.	

VGB_UVP_N	Detection of abnormal under voltage at the charge pump (VGB terminal).
0	Detect abnormal voltage.
1	Not detect abnormal voltage.
The threshold of the detection by ALARM VGB =< 7.6V (typical) The threshold for the cancellation of ALARM. VGB > 7.8V (typical) Error detection wait time can be set in UVCP_WAIT bit of ERROR_WAIT register. This protection is effective in all of PS_ALL_N bit,PS_CP_REG_N bit,PS_CP_N bit and MOT_EN bit are 1. Watch ALMRAW1register, When MOT_EN bit is 0.	

OCP_N	Register for setting a state of the overcurrent detection of the output phase.
0	Detect OCP.
1	Not detect OCP: .
The ALARM detection threshold can be set with the CS_SET1 register and the CS_SET2 register. When using this function, it is necessary to invalid power saving by PS_CSAMP_N bit in PS register. Error detection wait time can be set in OCPWAIT bit of ERROR_WAIT register.	

TSD_N	Register for setting the state of the thermal-shutdown(TSD) function.
0	Detect TSD.
1	Not detect TSD.
This protection is effective after supply the VM voltage. However, if this error occurs before supplying the system clock, it will not be recorded as a cause.	

2.4.8 ALARM Operation Setting Register1 (ALMOPE1)

This register selects protection processing by the pre-driver when errors are detected.

By setting this register, it is possible to stop the motor drive by operating the protection function when detecting errors of heat generation detection (TSD), overcurrent detection (OCP), and charge pump under-voltage (VGB_UVP, VGT_UVP). If the protection function is not used, set the corresponding function bit to 1 before release the power save mode. However, 0 must be set for the TSD_OPE_N bit.The protection function that operates when an OCP, VGB_UVP, or VGT_UVP occurs is not automatically released even if the cause of the error is released and the corresponding bit in the ALARM status register 1 (ALMSTS1) returns from “0” to “1”.

To clear the protection function must be set by the ALM_LATCH_CLR bit of the motor drive control setting register (DRIVE_SET). Error detection for VGB_UVP and VGT_UVP is possible only while motor drive permission is enabled. When a TSD error is detected, the 5V regulator is stopped by the protection function. However, when the TSD error is resolved (temperature drop), the 5V regulator automatically returns. Figure 2-15 shows changes in the motor drive status due to the protection function, using OCP as an example.

Figure 2-6 The Change in Motor Drive Status with the OCP Protection Function

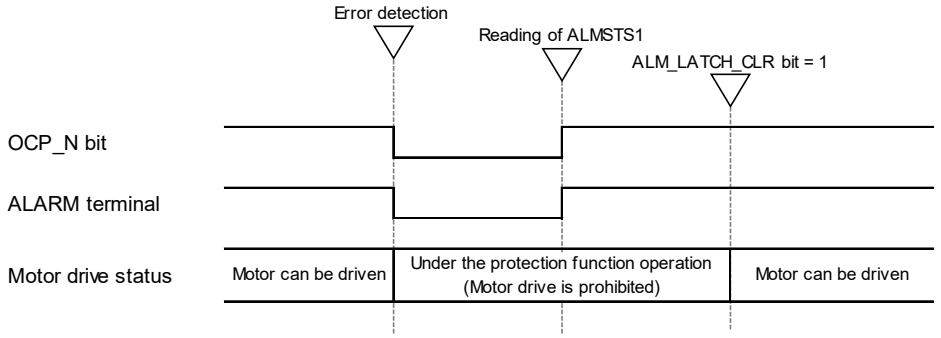


Table 2-14 Format of ALARM Operation Setting Register1 (ALMOPE1)

Address 14h After reset: 00h R/W

Symbol	7	6	5	4	3	2	1	0
ALMOPE1	0	0	0	VGT_UVP_OPE_N	0	VGB_UVP_OPE_N	OCP_OPE_N	TSD_OPE_N

VGT_UVP_OPE_N	Permission of abnormal under voltage detect protection at the charge pump (VGT terminal).
0	Permit
1	Prohibition
Detect abnormal:Output level for motor drive: Low (External MOFET: Hi-Z) To release the protection, please set the ALM_LATCH_CLR bit of the DRIVE_SET register to 1. NOTE: The abnormality detection is effective during the motor drive (PS_ALL_N bit = 1, PS_CP_REG bit = 1, PS_CP bit = 1, MOT_EN bit = 1).	

VGB_UVP_OPE_N	Permission of abnormal under voltage detect protection at the charge pump (VGB terminal).
0	Permit
1	Prohibition
Detect abnormal:Output level for motor drive: Low (External MOFET: Hi-Z) To release the protection, please set the ALM_LATCH_CLR bit of the DRIVE_SET register to 1. NOTE: The abnormality detection is effective during the motor drive (PS_ALL_N bit = 1, PS_CP_REG bit = 1, PS_CP bit = 1,MOT_EN bit = 1).	

OCP_OPE_N	Permission of abnormal overcurrent detection of the output phase.
0	Permit
1	Prohibition
Detect abnormal:Perform protection according to the OCP_ERR_SEL bit in DRIVE_SET register. During the protection, the operation can be selected by the OCP_ERR_SEL bit of the DRIVE_SET register. To release the protection, please set the ALM_LATCH_CLR bit of the DRIVE_SET register to 1. NOTE: When using the abnormality detection function, it is necessary to release the power save mode by the PS_CSAMP_N bit of the PS register. When prohibiting the execution of OCP protection processing (when setting the OCP_OPE_N bit to "1"), set the OCP_WAIT bit of the ERROR_WAIT register to a value other than "00".	

TSD_OPE_N	Permission of TSD detect protection.
0	Permit[Fixed]
1	Prohibition[No change]
Detect abnormal:Output level for motor drive: Low (External MOFET: Hi-Z) When utilizing the built-in 5V regulator, the TSD protection invalidates the operation of the built-in 5V regulator, so the power supply of RL78/G1F may be turned off.While the 5 V regulator is OFF, circuits other than the 3 V regulator (logic circuit power supply) and the TSD circuit are turned OFF.The built-in 5V regulator will recover as the temperature decreases.	

2.4.9 ALARM Pin Output Setting Register1 (ALMOUT1)

In order to perform the interrupt processing in the RL78/G1F, at the time of abnormality detection, and set the factor to carry out the error output from the ALARM terminal. “0” is enabled, “1” is disabled, and immediately after reset, all are enabled.

The ALARM pin returns from Low to High by the reading of the ALMSTS1 register when abnormal state is removed.

Table 2-15 Format of ALARM Pin Output Setting Register1 (ALMOUT1)

Address 16h After reset: 00h R/W

Symbol	7	6	5	4	3	2	1	0
ALMOUT1	VREG5_OVP_ALE_N	VGT_OVP1_ALE_N	VGT_OVP2_ALE_N	VGT_UVP_ALE_N	VGB_OVP_ALE_N	VGB_UVP_ALE_N	OCP_ALE_N	TSD_ALE_N

VREG5_OVP_ALE_N	Permission for output the detection state of abnormal over voltage at 5V Regulator to ALARM pin . .
0	Permit
1	Prohibition
The threshold of the detection by ALARM VREG5 => 5.7V (typical) Error detection wait time can be set in VREG5_OVP_WAIT bit of ERROR_WAIT register..	

VGT_OVP1_ALE_N	Permission for output the detection state of abnormal over voltage at the charge pump (VGT pin) 1 to ALARM pin .
0	Permit
1	Prohibition
The threshold of the detection by ALARM VGT => VM voltage + 18V (typical) The threshold for the cancellation of ALARM. VGT < VM voltage + 17V (typical) This protection is effective in all of PS_ALL_N bit,PS_CP_REG_N bit,PS_CP_N bit and MOT_EN bit are 1. Watch ALMRAW1register, When MOT_EN bit is 0.	

VGT_OVP2_ALE_N	Permission for output the detection state of abnormal over voltage at the charge pump (VGT pin) 2 to ALARM pin .
0	Permit
1	Prohibition
The threshold of the detection by ALARM VGT => 48V for RAJ306001, 60V for RAJ306010 (typical) The threshold for the cancellation of ALARM. VGT < 47V for RAJ306001, 59V for RAJ306010 (typical) This protection is effective in all of PS_ALL_N bit,PS_CP_REG_N bit,PS_CP_N bit and MOT_EN bit are 1. Watch ALMRAW1 register, When MOT_EN bit is 0.	

VGT_UVP_ALE_N	Permission for output the detection state of abnormal under voltage at the charge pump (VGT pin) to ALARM pin .
0	Permit
1	Prohibition
The threshold of the detection by ALARM VGT =< VM voltage + 7V (typical) The threshold for the cancellation of ALARM. VGT >VM voltage + 7.5V (typical) Error detection wait time can be set in UVCP_WAIT bit of ERROR_WAIT register.. This protection is effective in all of PS_ALL_N bit,PS_CP_REG_N bit,PS_CP_N bit and MOT_EN bit are 1. Watch ALMRAW1register, When MOT_EN bit is 0.	

VGB_OVP_ALE_N	Permission for output the detection state of abnormal over voltage at the charge pump (VGB pin) 1 to ALARM pin .
0	Permit
1	Prohibition
The threshold of the detection by ALARM VGB => 18V (typical) The threshold for the cancellation of ALARM. VGB < 17V (typical) This protection is effective in all of PS_ALL_N bit,PS_CP_REG_N bit,PS_CP_N bit and MOT_EN bit are 1. Watch ALMRAW1register, When MOT_EN bit is 0.	

VGB_UVP_ALE_N	Permission for output the detection state of abnormal under voltage at the charge pump (VGB pin) to ALARM pin .
0	Permit
1	Prohibition
The threshold of the detection by ALARM VGB =< 7.6V (typical) The threshold for the cancellation of ALARM. VGB > 7.8V (typical) Error detection wait time can be set in UVCP_WAIT bit of ERROR_WAIT register. This protection is effective in all of PS_ALL_N bit,PS_CP_REG_N bit,PS_CP_N bit and MOT_EN bit are 1. Watch ALMRAW1 register, When MOT_EN bit is 0.	

OCP_ALE_N	Permission for output the detection state of oabnormal overcurrent detection to ALARM pin .
0	Permit
1	Prohibition
The ALARM detection threshold can be set with the CS_SET1 register and the CS_SET2 register. When using this function, it is necessary to invalid power saving by PS_CSAMP_N bit in PS register. Error detection wait time can be set in OCPWAIT bit of ERROR_WAIT register.	

TSD_ALE_N	Permission for output the detection state of the thermal-shutdown(TSD) detection to ALARM pin .
0	Permit
1	Prohibition
This protection is effective after supply the VM voltage. However, if this error occurs before supplying the system clock, it will not be recorded as a cause.	

2.4.10 ALARM Status Register2 (ALMSTS2)

This register stores the abnormal state detected by the pre-driver. The abnormal state detection function is enabled after release the power save of the analog block corresponding to the abnormal state."1" is the abnormal undetected state, "0" is the anomaly detection state.

When an abnormal condition is detected, the bits corresponding to each factor changes from "1" to "0". The status is retained until reading the register after an error is detected, and these are updated to the latest information at the time.

<R>

Table 2-16 Format of ALARM Status Register2 (ALMSTS2)

Address: 18h Reset: FFh R

Symbol	7	6	5	4	3	2	1	0
ALMSTS2	1	1	1	1	1	1	1	VM_UVP_N

VM_UVP_N	Detection of abnormal under voltage at VM by VMC function.
0	Detect abnormal voltage.
1	Not detect abnormal voltage.
The threshold of the detection by ALARM VM =< 5.5V The threshold for the cancellation of ALARM. VM >5.9V This protection is effective in all of PS_ALL_N bit and PS_VMC_N bit are 1.	

2.4.11 Current Sense Setting Register2 (CS_SET2)

<R>

It is a register that adjusts the setting of the CS amplifier that detects the voltage level difference between the ISENP and ISENN terminals due to the current flowing through the shunt resistor. Please use in combination with the Current Sense Setting Register1 (CS_SET1).

Table 2-17 Format of Current Sense setting Register2 (CS_SET2)

Address: 1Ah Reset: 00h R/W

Symbol	7	6	5	4	3	2	1	0
CS_SET2	CSAMP_IREF1	CSAMP_IREF0	CSAMP_ATT	0	0	0	0	0

CSAMP_IREF1	CSAMP_IREF0	Adjustment of possible the current detection width
0	0	Variable width x1
0	1	Variable width x3
1	0	Variable width x5
1	1	Setting prohibited.

CSAMP_ATT	Adjustment of the input level for the current detection
0	Setting prohibited.
1	x1.0
Initinal value is "0".Be sure to set 1 when using CS amp.	

2.4.12 ALARM Pin Output Setting Register2 (ALMOUT2)

In order to perform the interrupt processing in the RL78 / G1F, at the time of abnormality detection, and set the factor to carry out the error output from the ALARM terminal. “0” is enabled, “1” is disabled, and immediately after reset, all are enabled.

The ALARM pin returns from Low to High by the reading of the ALMSTS2 register when abnormal state is removed.

Table 2-18 Format of ALARM Pin Output Setting Register2 (ALMOUT2)

Address: 1Ch Reset: 00h R/W

Symbol	7	6	5	4	3	2	1	0
ALMOUT2	0	0	0	0	0	0	0	VM_UVP_ALE_N

VM_UVP_ALE_N	Permission for output the detection state of abnormal under voltage at VM to ALARM pin .
0	Permit
1	Prohibition

2.4.13 Error Detection Wait Time Setting Register (ERROR_WAIT)

This register is used to set the filter time for detecting abnormal conditions.

If an error condition is detected for more than the time set in this register, it is judged as an error.

The setting change of this register is prohibited when driving a motor (MOT_EN bit = 1).

Setting OCP_WAIT to “0us” is prohibited when the protection processing execution prohibition for OCP by the ALMOPE1 register

Table 2-19 Format of Error Detection Wait Time Setting Register (ERROR_WAIT)

Address: 1Eh Reset: 00h R/W

Symbol	7	6	5	4	3	2	1	0
ERROR_WAIT	0	0	0	VREG5_OVP_WAIT	UVCP_WAIT1	UVCP_WAIT0	OCP_WAIT1	OCP_WAIT0

VREG5_OVP_WAIT	Setting of Waiting time for the judgment of the overvoltage detection by the 5V regulator.
0	Waiting time: 1us
1	Waiting time: 2us

UVCP_WAIT1	UVCP_WAIT0	Setting of Waiting time for the judgment of detection of under voltage at the charge pump. (VGB and VGT pin).
0	0	From Detection of drop voltage: 0ms (None Waiting time.)
0	1	From Detection of drop voltage: 0.5ms
1	0	From Detection of drop voltage: 1ms
1	1	From Detection of drop voltage: 5ms

OCP_WAIT1	OCP_WAIT0	Setting of Waiting time for the judgment of detection of over current at output phase.
0	0	From detection of over current at output phase: 0us (None Waiting time.) [Setting prohibited when OCP_OPE_N bit is 1]
0	1	From detection of over current at output phase: 1us
1	0	From detection of over current at output phase: 2.5us
1	1	From detection of over current at output phase: 5us

2.4.14 Current Sense Setting Register1 (CS_SET1)

It is a register that adjusts the setting of the CS amplifier that detects the voltage level difference between the ISENP and ISENN terminals. Please use in combination with the Current Sense Setting Register2 (CS_SET2).

Table 2-20 Format of Current Sense Setting Register1 (CS_SET1)

Address: 20h After reset: 00h R/W

Symbol	7	6	5	4	3	2	1	0
CS_SET1	0	SHUNT_SEL2	SHUNT_SEL1	SHUNT_SEL0	OCP_SEL_H3	OCP_SEL_H2	OCP_SEL_H1	OCP_SEL_H0

<R>

SHUNT_SEL2	SHUNT_SEL1	SHUNT_SEL0	Setting of samplifier gain level for detection voltage.
0	0	0	Amp gain level for detection of Overcurrent: x10 Amp gain level for detection of the current level: x50
1	0	0	Amp gain level for detection of Overcurrent: x5 Amp gain level for detection of the current level: x25
1	0	1	Amp gain level for detection of Overcurrent: x1.65 Amp gain level for detection of the current level: x8.25
Other than above.			Setting prohibited.

<R>

OCP_SEL_H3	OCP_SEL_H2	OCP_SEL_H1	OCP_SEL_H0	Setting threshold voltage level for overcurrent detection comparator. [Condition] SHUNT_SEL : "000" (Voltage level that was detected x 50) CSAMP_IREF : "10" (The threshold of the voltage x 5) CSAMP_ATT : "1" (The threshold of the voltage x 1)
0	0	0	0	0.07[V]-----The current level for detection = 0.07 / SHUNT resistance level
0	0	0	1	0.08[V]-----The current level for detection = 0.08 / SHUNT resistance level
0	0	1	0	0.09[V]-----The current level for detection = 0.09 / SHUNT resistance level
0	0	1	1	0.10[V]-----The current level for detection = 0.10 / SHUNT resistance level
0	1	0	0	0.11[V]-----The current level for detection = 0.11 / SHUNT resistance level
0	1	0	1	0.12[V]-----The current level for detection = 0.12 / SHUNT resistance level
0	1	1	0	0.13[V]-----The current level for detection = 0.13 / SHUNT resistance level
0	1	1	1	0.14[V]-----The current level for detection = 0.14 / SHUNT resistance level
1	0	0	0	0.15[V]-----The current level for detection = 0.15 / SHUNT resistance level
Other than above.				Setting prohibited.
The threshold of the voltage for overcurrent detection comparators can set. Voltage level for detection of external SHUNT resistance can set by SHUNT_SEL and OCP_SL_H being set. A potential difference of SHUNT resistance connected to ISENP terminal and ISENN terminal becomes the voltage level for detection of the SHUNT resistance.				

2.4.15 Hall IC Threshold Adjustment Register (HAIC_TH)

Detection setting for the Hall-IC comparator.

Table 2-21 Format of Hall IC Threshold Adjustment Register (HAIC_TH)

Address: 22h Reset: 00h R/W

Symbol	7	6	5	4	3	2	1	0
HAIC_TH	0	0	HAIC_HYS1	HAIC_HYS0	0	HAIC_TH2	HAIC_TH1	HAIC_TH0

HAIC_HYS1	HAIC_HYS0	Hysteresis setting for Hall IC comparator.
0	0	0mV
0	1	50mV
1	0	100mV
1	1	Setting prohibited.

HAIC_TH2	HAIC_TH1	HAIC_TH0	Threshold setting for Hall IC comparator.
0	0	0	0.4V (typical)
0	0	1	0.7V (typical)
0	1	0	1.0V (typical)
0	1	1	1.3V (typical)
1	0	0	1.6V (typical)
1	0	1	1.9V (typical)
1	1	0	2.2V (typical)
1	1	1	2.5V (typical)

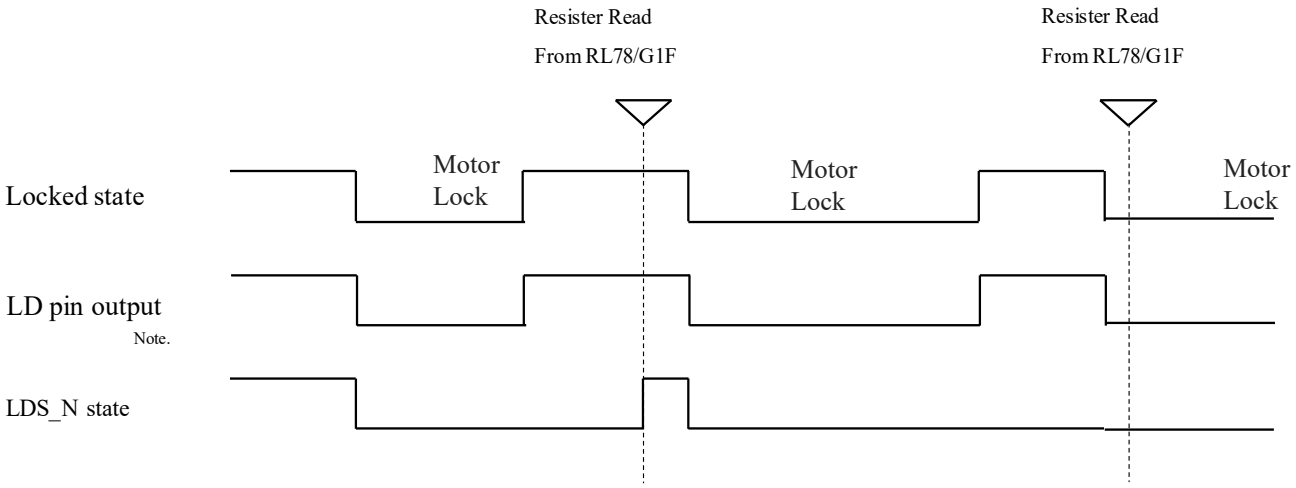
2.4.16 Pre-Driver Drive Status Register (PDDSTS)

This register stores the Hall IC input status (HALLMON_U, HALLMON_V, HALLMON_W) , the FG (rotation electrical angle 60 degree) status(FG) determined. and the motor lock status (LDS_N). This function cannot be used when sensor-less control is adopted.

Motor lock status can be confirmed from LD pin and LDS_N bit. The output of the LD pin shows the current motor status (High: Not lock, Low: Lock), whereas the LDS_N bit, when motor lock state is detected, this change from “1” to “0” and keeps this signal till readout is done. As a result, it is possible to check whether motor lock occurred between the last access and the current access.

Figure 2-7 Motor locking detection

<R>



Note. When LDWAIT = “000” is set , LD_ALE_E enables output to the LDS pin (LD_ALE_E=0)

Table 2-22 Format of Pre-Driver Drive Status Register (PDDSTS)

<R>

Addres: 24h Reset: F0h R

Symbol	7	6	5	4	3	2	1	0
PDDSTS	1	1	1	LDS_N	FG	HALLMON_U	HALLMON_V	HALLMON_W

LDS_N	Confirmation of the motor lock detection state.
0	Detect the motor lock state.
1	Non detect the motor lock state.
When IC detect a motor lock state, the LDS_N bit becomes 0 data. It is updated in a latest lock state by the read operation of the data of this bit.	

FG	The output changes by each rotation of electric angle of 60 degrees.
0	Low
1	High
This bits is always updated when PS_ALL_N bit = 1 and PS_HALL_N bit = 1.	

HALLMON_U	Result of U-phase Hall-IC comparator.
0	Inpout level is low.
1	Inpout level is high.
HALLMON_V	Result of V-phase Hall-IC comparator.
0	Inpout level is low.
1	Inpout level is high.
HALLMON_W	Result of W-phase Hall-IC comparator.
0	Inpout level is low.
1	Inpout level is high.
These bits are always updated when PS_ALL_N bit = 1 and PS_HALL_N bit = 1.	

2.4.17 LD Judgment Wait Time Register (LD_WAIT)

This register is used to set the status output from the LD terminal and the judgment time for detecting the motor lock when the motor lock is detected. The setting change of the LD_WAIT bit is prohibited when driving a motor (MOT_EN bit = 1)

The definition of “Motor lock” is that input of any two of three Hall IC output are not changed.

Table 2-23 Format of LD Judgment Wait Time Register (LD_WAIT)

Address: 26h Reset: 00h R/W

Symbol	7	6	5	4	3	2	1	0
LD_WAIT	LD_ALE_N	0	0	0	0	LD_WAIT2	LD_WAIT1	LD_WAIT0

LD_ALE_N	Output permission setting to LD pin in motor locked state,
0	Permit
1	Prohibition

LD_WAIT2	LD_WAIT1	LD_WAIT0	Setting of waiting time for the motor lock detection judgement .
0	0	0	0.01s
0	0	1	0.02s
0	1	0	0.05s
0	1	1	0.10s
1	0	0	0.20s
1	0	1	0.30s
1	1	0	0.40s
1	1	1	0.50s

2.4.18 Motor Drive Control Setting Register (DRIVE_SET)

This register is used to be set the motor drive permission, the motor rotation direction, the protection operation when OCP occurs, the dead time adjustment function, the motor drive permission, the release protection operation when abnormality is detected, and the CS amplifier hysteresis.

<R> When protection processing is activated by detecting OCP, VGB_UVP, or VGT_UVP and the motor drive is stopped, writing “1” to the ALM_LATCH_CLR bit in this register releases the protection processing and restarts the motor drive. I can do it. For details, see the example in “Figure 2 15 Changes in motor drive status due to OCP protection function”.

The protection method for OCP errors can be selected using the OCP_ERR_SEL bit.

Table 2-24 Format of Motor Drive Control Setting Register (DRIVE_SET)

Addres:28h Reset: 00h R/W

<R>

Symbol	7	6	5	4	3	2	1	0
DRIVE_SET	OCP_HYS_N	ALM_LATCH_CLR	0	DECAY_MODE_SEL	DT_REG_N	OCP_ERR_SEL	DIR_SEL	MOT_EN

OCP_HYS_N	Enable / Disable of the hysteresis for OCP can be changed.
0	The hysteresis is Enable.
1	The hysteresis is Disable.

ALM_LATCH_CLR	Stop protection operation when detecting ALARM.
0	Keep protective action.
1	Stop protective action.
When an ALARM event subject to protection operation occurs, the protection operation is executed until this protection bit is released by this bit. While the protection operation is in operation, the motor is in Hi-Z state or Low brake state. [Target function]: OCP (Over current protection) VGT_UVP(Under voltege protection for VGT side charge-pump) ,VGB_UVP(Under voltege protection for VGB side charge-pump)	

DECAY_MODE_SEL	Setting of motor driving method (regenerative method)
0	Normal PWM control method.
1	Commutation control method.
Commutation control is prohibited when setting sensorless control. When commutation control is performed using this function, follow the recommended waveform	

DT_REG_N	Adjustment of dead-off time
0	Permit---For the input PWM signal, adjust the dead time on the Pre-Driver side.
1	Prohibition---It drives with the input PWM signal.make dead time with F/W.

OCP_ERR_SEL	Setting of the control of when an alarm phenomenon of OCP was generated.
0	Output of Hi-Z
1	Low-side output: Brake control.
When other alarm occurs, the Hi-Z output takes most priority.	

DIR_SEL	Setting of the rotation direction of the motor.
0	CW
1	CCW
Please set which direction of MCU control is CW / CCW. It performs control based on the above setting by internal circuit operation. This register is used for commutation mode and BEMF amplifier control during Hall IC control.	

MOT_EN	Setting of permission for the motor rotation operation.
0	Motor is stopped state.
1	Motor is rotation state.
When this bit is 0, the motor drive stage output (UH, UL, VH, VL, WH, WL terminals) become L output. If change the connection of the motor, when this bit is 0, set SELSIG_U, SELSIG_V and SEL_SIG_W register, and be set to 1 PWM_SEL bit of HALL_SIG register.	

2.4.19 High Side Output Current Capability Setting Register (IDRCNT_H)

This register adjusts the peak level of the drive current when turning on the drive MOSFET.

By changing the peak level, it is possible to change the rising slew rate.

By setting the IDR_H_P*, IDR_H_N*, IDR_L_P* and IDR_L_N* bits in High/Low Side Output Current Capability Setting Register (IDRCNT_H / IDRCNT_L), it is possible to adjust the sink/source current flow level by 8 step.

It is more effective with using Pch Slew Rate Setting Register (TRCNT_P). The simple block diagram is shown below.

Figure 2-8 Output current adjustment function

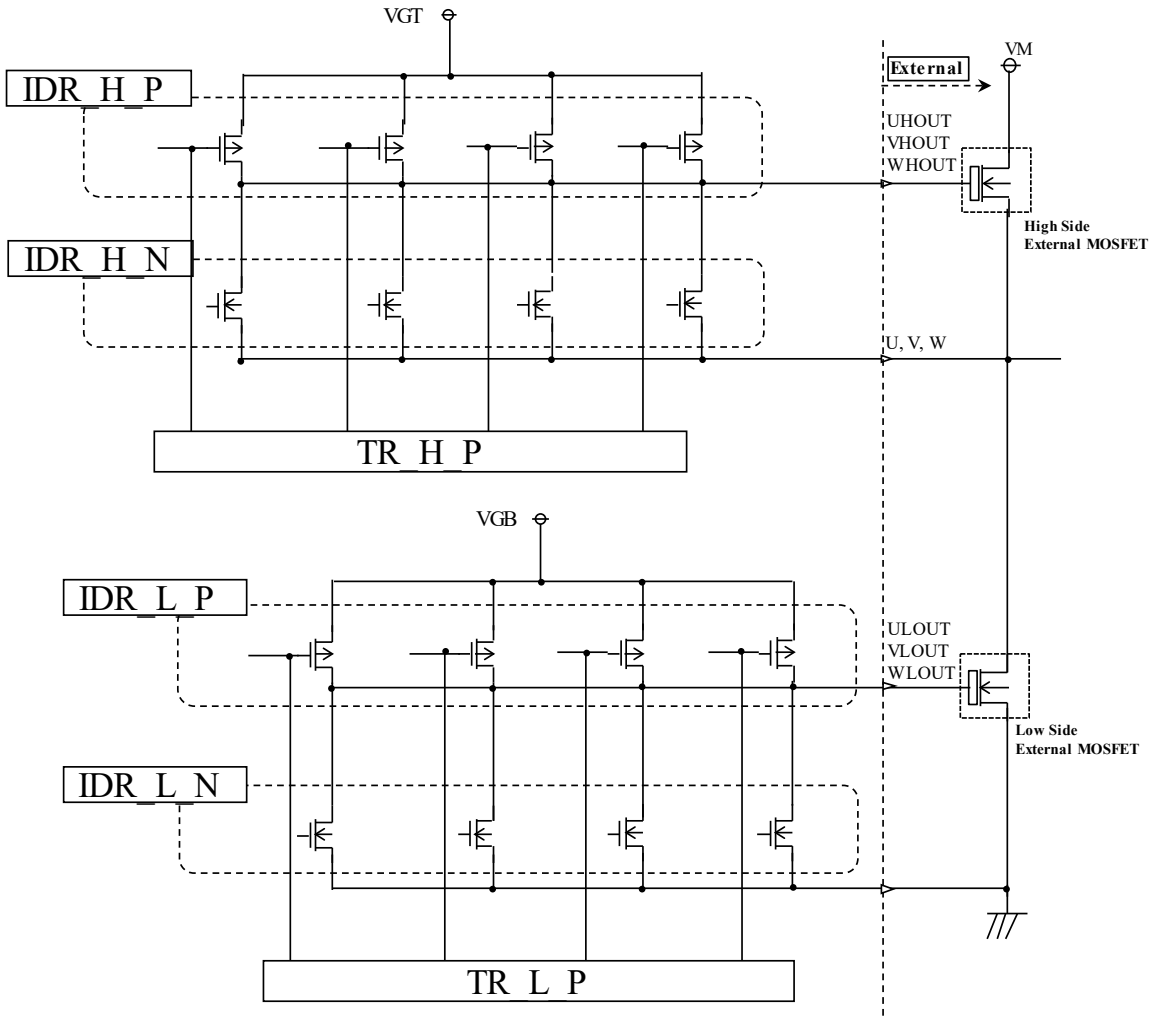


Table 2-25 Format of High Side Output Current Capability Setting Register (IDRCNT_H)

Address: 2Ch Reset: 00h R/W

Symbol	7	6	5	4	3	2	1	0
IDRCNT_H	0	IDR_H_P2	IDR_H_P1	IDR_H_P0	0	IDR_H_N2	IDR_H_N1	IDR_H_N0

IDR_H_P2	IDR_H_P1	IDR_H_P0	High side Pch current output capability setting
0	0	0	65.0 ohm (typical)
0	0	1	32.0 ohm (typical)
0	1	0	22.5 ohm (typical)
0	1	1	17.5 ohm (typical)
1	0	0	14.0 ohm (typical)
1	0	1	12.0 ohm (typical)
1	1	0	10.5 ohm (typical)
1	1	1	9.5 ohm (typical)

IDR_H_N2	IDR_H_N1	IDR_H_N0	High side Nch current output capability setting
0	0	0	5.0 ohm (typical)
0	0	1	6.0 ohm (typical)
0	1	0	7.0 ohm (typical)
0	1	1	8.5 ohm (typical)
1	0	0	10.0 ohm (typical)
1	0	1	13.5 ohm (typical)
1	1	0	19.0 ohm (typical)
1	1	1	38.5 ohm (typical)

Table 2-26 Format of Low Side Output Current Capability Setting Register (IDRCNT_L)

Address: 2Eh Reset: 00h R/W

Symbol	7	6	5	4	3	2	1	0
IDRCNT_L	0	IDR_L_P2	IDR_L_P1	IDR_L_P0	0	IDR_L_N2	IDR_L_N1	IDR_L_N0

IDR_L_P2	IDR_L_P1	IDR_L_P0	Low side Pch current output capability setting
0	0	0	27.0 ohm (typical)
0	0	1	14.0 ohm (typical)
0	1	0	10.0 ohm (typical)
0	1	1	8.0 ohm (typical)
1	0	0	7.0 ohm (typical)
1	0	1	6.0 ohm (typical)
1	1	0	5.5 ohm (typical)
1	1	1	5.0 ohm (typical)

IDR_L_N2	IDR_L_N1	IDR_L_N0	Low side Nch current output capability setting
0	0	0	2.5 ohm (typical)
0	0	1	3.0 ohm (typical)
0	1	0	3.5 ohm (typical)
0	1	1	4.0 ohm (typical)
1	0	0	5.0 ohm (typical)
1	0	1	6.0 ohm (typical)
1	1	0	9.0 ohm (typical)
1	1	1	17.5 ohm (typical)

2.4.20 Pch Slew Rate Setting Register (TRCNT_P)

This register adjusts the peak level of the driving current when the external MOSFET is ON.

Changing the peak level of the drive current changes the rising slew rate.

The slew rate is adjusted by changing the gate drive waveforms of MPU1 to 4 and MPL1 to 4 that drive the drive MOSFET. TR_H_P bit corresponds to the High side current and the TR_L_P bit corresponds to the Low side current. To accurately adjusted more current, please use in combination with IDRCNT_H and IDRCNT_L.

The adjustment part of the pre-driver is shown below.

Figure 2-9 External MOSFET current Control.

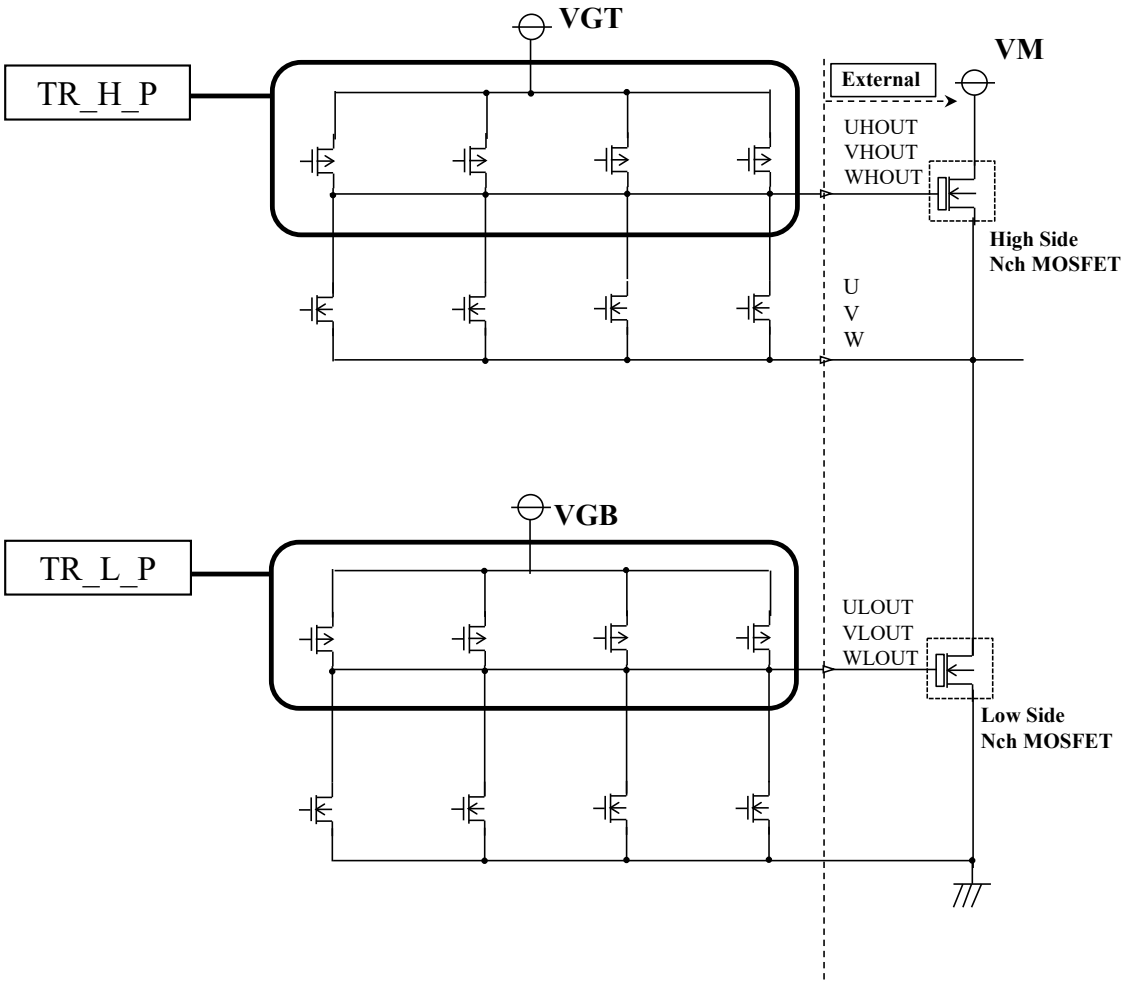


Table 2-27 Format of Pch Slew Rate Setting Register (TRCNT_P)

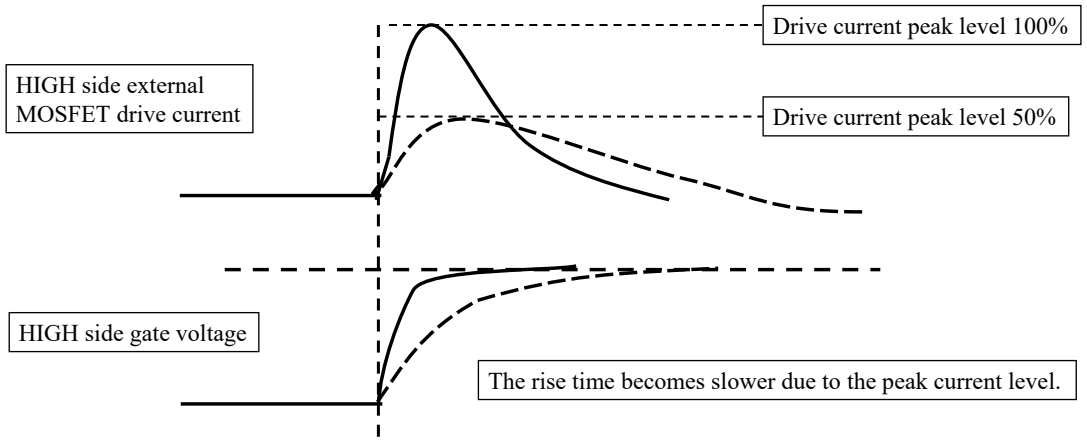
Addres: 30h Reset: 00h R/W

Symbol	7	6	5	4	3	2	1	0
TRCNT_P	0	TR_H_P2	TR_H_P1	TR_H_P0	0	TR_L_P2	TR_L_P1	TR_L_P0

TR_H_P2	TR_H_P1	TR_H_P0	High side external MOSFET driving current peak level adjustment.
0	0	0	100%
0	0	1	95%
0	1	0	90%
0	1	1	80%
1	0	0	65%
1	0	1	55%
1	1	0	40%
1	1	1	30%
NOTE: When the gate capacitance of the external MOSFET is 25000pF, the peak level of the driving current is being made as the reference.			

TR_L_P2	TR_L_P1	TR_L_P0	Low side external MOSFET driving current peak level adjustment.
0	0	0	100%
0	0	1	95%
0	1	0	90%
0	1	1	80%
1	0	0	65%
1	0	1	55%
1	1	0	40%
1	1	1	30%
NOTE: When the gate capacitance of the external MOSFET is 25000pF, the peak level of the driving current is being made as the reference.			

Figure 2-10 Slew Rate Change with Peak Current Adjustment



2.4.21 Charge Pump Setting Register 1 (CPSET1)

This register is used to set the division ratio of the operation clock of the charge pump.

The initial value is divided by 24 (167KHz).

The setting change is prohibited when the charge pump circuit power save is released (PS_CP_N = 1).

Table 2-28 Format of Charge Pump Setting Register 1 (CPSET1)

Addres: 32h Reset: 01h R/W

Symbol	7	6	5	4	3	2	1	0
CPSET1	0	0	0	0	0	0	CP_CLK_DIV1	CP_CLK_DIV0

CP_CLK_DIV1	CP_CLK_DIV0	Change the charge pump operation clock frequency.
0	0	Frequency division ratio: 1/18---222kHz
0	1	Frequency division ratio: 1/24---167kHz(initial)
1	0	Frequency division ratio: 1/36---111kHz
1	1	Frequency division ratio: 1/40---100kHz

2.4.22 Charge Pump Setting Register2 (CPSET2)

Set the charge boost setting by using the charge pump. In the initial state, the double boost function is effective.

When the double boost function is valid, the VGB voltage becomes to about 13V, and VGT becomes to “VM + VGB” voltage. By using this function, it is capable of VGB voltage over 10V even if low VM voltage (VM=6~10V).

When the double boost function is invalid, VGB is 10V and VGT is “VM+10V”. And when VM voltage becomes under about 10V, VGB voltage decrease and is almost equal to VM voltage.

<R> It is prohibited to change the value of this register while the charge pump circuit is operating (PS_CPREG_N = 1).

Table 2-29 Format of Charge Pump Setting Register2(CPSET2)

Address: 34h After reset: 02h R/W

Symbol	7	6	5	4	3	2	1	0
CPSET2	0	0	0	0	CP_BOOST_N	VREG10_OUT	VREG6P5_OUT	0

CP_BOOST_N	Setting of the Enable / Disable of the Double Boost function for Charge pump.
0	Enable double boost function(initial)
1	Disable double boost function

VREG10_OUT	Setting of operation for 10V Charge pump.
0	Prohibition(initial)
1	Permit

VREG6P5_OUT	Setting of operation for 6.5V Charge pump.
0	Prohibition
1	Permit(initial)

<R> To change the setting, change the PS_CPREG_N bit and PS_CP_N bit in the PS register to 0 before changing the setting.
Use this register in the following combination.

	CP_BOOST_N	VREG10_OUT	VREG6P5_OUT
Enable double boost function.	0(initial)	0(initial)	1(initial)
Disable double boost function.	1	1	0

The recommended circuit differs depending on the double boosting.

2.4.23 Charge Pump Trimming Register (CP_TRIM)

Set the trimming value of the charge pump.

This register does not need to be set or changed, but is written to prevent incorrect writing.

Table 2-30 Format of Charge Pump Trimming Register (CP_TRIM)

Address: 36h Reset: 00h R/W

Symbol	7	6	5	4	3	2	1	0
CP_TRIM	CP_TRIM7 - CP_TRIM0							

CP_TRIM7 - CP_TRIM0	
If not specified, please set 00h (initial value).	

2.4.24 5V Regulator Voltage Setting Register (VREG5_TRIM)

<R> Set the trimming value of the 5V regulator. Output voltage at shipped is 4.8V typ. (Bit5 & 4 = 0)

Trimming data is written at upper 4 bit of TRIM_DATA0(EFFECh) when this IC is shipped from Renesas. Please write bit5=1 and bit4=0, and also write bit 3-0 upper 4 bit of TRIM_DATA0.

Concrete procedure is described in “2.5.11 Trimming Register Block”

Table 2-31 Format of 5V Regulator Voltage Trimming Register (VREG5_TRIM)

Address: 40h After reset: 00h R/W

Symbol	7	6	5	4	3	2	1	0
VREG5_TRIM	VREG5_TRIM_7 - VREG5_TRIM_0							

VREG5_TRIM_5 - VREG5_TRIM_4	Center of the output voltage	Note.
00	4.8V	Reference : Trimmed value to center voltage This value is reference value when trimming data is changed. Renesas recommend to use trimming data stored in TRIM_DATA0 on RL78.
01	4.9V	
10	5.0V	
11	5.1V	

VREG5_TRIM_3 - VREG5_TRIM_0	Displacement amount relative to the center of the output voltage	Note.
0000	About 0.00%	Reference : Trimmed value to center voltage This value is reference value when trimming data is changed. Renesas recommend to use trimming data stored in TRIM_DATA0 on RL78.
0001	About 0.14%	
0010	About 0.29%	
0011	About 0.43%	
0100	About 0.57%	
0101	About 0.72%	
0110	About 0.86%	
0111	About 1.01%	
1000	About -1.12%	
1001	About -0.98%	
1010	About -0.84%	
1011	About -0.70%	
1100	About -0.56%	
1101	About -0.42%	
1110	About -0.28%	
1111	About -0.14%	

2.4.25 Current Sense AMP Trimming Register (CSAMP_TRIM)

Table 2-32 Format of Current Sense AMP Trimming Register (CSAMP_TRIM)

Address: 42h Reset: 00h R/W

Symbol	7	6	5	4	3	2	1	0
CSAMP_TRIM	CSAMP_TRIM7 - CSAMP_TRIM0							

CSAMP_TRIM7 - CSAMP_TRIM0	
It is a trimming register for the current detection AMP. By setting this register, the current detection amplifier is adjusted 0. When using over current detection function, please set "CSAMP_TRIM5" bit = "1". "CSAMP_TRIM4" bit = "0".	

2.4.26 ALARM Raw Status Monitor Register1 (ALMRAW1)

With this register, it is possible to check whether the voltage of the charge pump (VGT pin, VGB pin) is normal. If the monitor voltage is within the threshold (normal), it will be “1”, and if it exceeds the threshold, it will be “0”, and the charge pump status (voltage abnormality) can be confirmed.

After starting up, the charge pump may become undervoltage or overvoltage until it stabilizes. Use this register to confirm that the charge pump voltage has stabilized and then start driving the motor.

This register is valid when PS_ALL_N bit = “1”, PS_CPREG_N bit = “1”, PS_CP_N bit = “1”. The ALMSTS1 register is latched, while this register is not latched.

<R>

Table 2-33 Format of ALARM Raw Status Monitor Register1 (ALMRAW1)

Address: 58h After reset: FFh R/W

Symbol	7	6	5	4	3	2	1	0
ALMRAW1	1	VGT_OVP1_RAW_N	VGT_OVP2_RAW_N	VGT_UVP_RAW_N	VGB_OVP_RAW_N	VGB_UVP_RAW_N	1	1

VGT_OVP1_RAW_N	Detection of abnormal over voltage at the charge pump (VGT terminal) 1.
0	Detecting
1	Not detected
The threshold of the detection by ALARM VGT => VM voltage + 18V (typical) The threshold for the cancellation of ALARM. VGT < VM voltage + 17V (typical) This protection is effective in all of PS_ALL_N bit,PS_CP_REG_N bit and PS_CP_N bit are 1.	

VGT_OVP2_RAW_N	Detection of abnormal over voltage at the charge pump (VGT terminal) 2.
0	Detecting
1	Not detected
The threshold of the detection by ALARM VGT => 48V for RAJ306001, 60V for RAJ306010 (typical) The threshold for the cancellation of ALARM. VGT < 47V for RAJ306001, 59V for RAJ306010 (typical) This protection is effective in all of PS_ALL_N bit,PS_CP_REG_N bit and PS_CP_N bit are 1.	

VGT_UVP_RAW_N	Detection of abnormal under voltage at the charge pump (VGT terminal).
0	Detecting
1	Not detected
The threshold of the detection by ALARM VGT =< VM voltage + 7V (typical) The threshold for the cancellation of ALARM. VGT >VM voltage + 7.5V (typical) This protection is effective in all of PS_ALL_N bit,PS_CP_REG_N bit and PS_CP_N bit are 1.	

VGB_OVP_RAW_N	Detection of abnormal over voltage at the charge pump (VGB terminal).
0	Detecting
1	Not detected
The threshold of the detection by ALARM VGB => + 18V (typical) The threshold for the cancellation of ALARM. VGB < + 17V (typical) This protection is effective in all of PS_ALL_N bit,PS_CP_REG_N bit and PS_CP_N bit are 1.	

VGB_UVP_RAW_N	Detection of abnormal under voltage at the charge pump (VGB terminal).
0	Detecting
1	Not detected
The threshold of the detection by ALARM VGB =< + 7.6V (typical) The threshold for the cancellation of ALARM. VGB > + 7.8V (typical) This protection is effective in all of PS_ALL_N bit,PS_CP_REG_N bit and PS_CP_N bit are 1.	

2.4.27 TOIN Pin Monitor Register (TOIN_MONI)

This register is used to confirm that the expected signal is input from the MCU by monitoring the pin level of the PWM pin.

Table 2-34 Format of TOIN Pin Monitor Register (TOIN_MONI)

<R> Address: 5Ch Reset: - R

Symbol	7	6	5	4	3	2	1	0
TOIN_MONI	TOINA	TOINB	TOINC	TOIND	TOINE	TOINF	TOING	TOINH

TOINA	Monitor input level of TOINA pin.
0	Low level
1	High level
TOINB	Monitor input level of TOINB pin.
0	Low level
1	High level
TOINC	Monitor input level of TOINC pin.
0	Low level
1	High level
TOIND	Monitor input level of TOIND pin.
0	Low level
1	High level
TOINE	Monitor input level of TOINE pin.
0	Low level
1	High level
TOINF	Monitor input level of TOINF pin.
0	Low level
1	High level
TOING	Monitor input level of TOING pin.
0	Low level
1	High level
TOINH	Monitor input level of TOINH pin.
0	Low level
1	High level
Change of input is prohibited while reading this register.	

2.4.28 WHO_AM_I register (WHO_AM_I)

This register is used to check the communication status between the Pre-Driver and MCU.

After supplying the clock, read the value of this register and make sure that the correct value can be read before making various settings.

Table 2-35 Format of WHO_AM_I register (WHO_AM_I)

Address: 5Eh After reset: A6/6B R

Symbol	7	6	5	4	3	2	1	0
WHO_AM_I	WHO_AM_I7 - WHO_AM_I0							

WHO_AM_I7 - WHO_AM_I0	Communication confirmation
RAJ306001:01101010b(6Ah) RAJ306010:01101011b(6Bh)	Communication OK
Other than above.	Communication NG

2.4.29 Trimming Protect Register (TRIM_PT)

This is protection bit related to the TRIM_EN register, BGR_TRIM register and BFAMP_TRIM register. Before writing to the above register, release the this protect mode.

Moreover, after the completion of the above setting, set the protect mode again.

Table 2-36 Format of Trimming Protect Register (TRIM_PT)

Address: 60h Reset: 00h R/W

Symbol	7	6	5	4	3	2	1	0
TRIM_PT	TEST_PT_7 - TEST_PT_0							

TEST_PT_7 - TEST_PT_0	The write protect of the TRIM_EN register, BGR_TRIM register and BFAMP_TRIM register.
10010101	Protect release (Write enable)
Other than the above	During protection (Write disable)
Set it up before accessing the TRIM_EN register, BGR_TRIM register and BFAMP_TRIM register.	

2.4.30 Trimming Data Enable Register (TRIM_EN)

After setting the trimming value in the BGR_TRIM register and BFAMP_TRIM register, the values will be active by writing 1.

Table 2-37 Format of Trimming Data Enable Register (TRIM_EN)

Address: 74h Reset: 00h R/W

Symbol	7	6	5	4	3	2	1	0
TRIM_EN	0	0	0	0	0	0	0	TRIM_EN

TRIM_EN	The switching between the setting enable/disable of the trimming data that write to the BGR_TRIM register and BFAMP_TRIM register.
0	Invalid trim data
1	Valid trim data
Before setting this register, please release write protect function by setting "TRIM_PT" register. Please set "1" after storing trimming data in "BGR_TRIM" and "BFAMP_TRIM" register.	

2.4.31 High Accuracy BGR Temperature Correction Register (BGR_TRIM)

Table 2-38 Format of High Accuracy BGR Temperature Correction Register (BGR_TRIM)

Address: 78h Reset: 00h R/W

Symbol	7	6	5	4	3	2	1	0
BGR_TRIM	BGR_TRIM_7 - BGR_TRIM_0							

BGR_TRIM_7 - BGR_TRIM_0	The trimming register for the temperature correction of BGR for the 5V regulator
By storing the trimming data into this register, the temperature accuracy of the 5V regulator can be preserved. The setting of this register is enabled by setting 1 into the TRIM_EN register. Before setting this register, please release the write protect by setting the TRIM_PT register.	

2.4.32 BUFFAMP Absolute Value Correction Register (BFAMP_TRIM)

Table 2-39 Format of BUFFAMP Absolute Value Correction Register (BFAMP_TRIM)

Address: 7Ah Reset: 00h R/W

Symbol	7	6	5	4	3	2	1	0
BFAMP_TRIM	BFAMP_TRIM_7 - BFAMP_TRIM_0							

BFAMP_TRIM_7 - BFAMP_TRIM_0	The trimming register of BUFFAMP for the 5V regulator
By storing the trimming data into this register, BUFFAMP of 5V regulator is trimmed, and 5V is outputted from VREG5 pin. The setiing of this register is enabled by setting 1 into the TRIM_EN register. Before setting this register, please release the write protect by setting the TRIM_PT register.	

2.5 Pre-Driver Function (Setting / Usage)

2.5.1 Pre-Drive Block

Pre-Driver has a dead time adjustment function and a slew rate adjustment function which can be controlled by MCU. When using this function, it is necessary to release power save by PS_ALL_N, PS_CPREG_N, PS_CP_N, and PS_PRE_N bits.

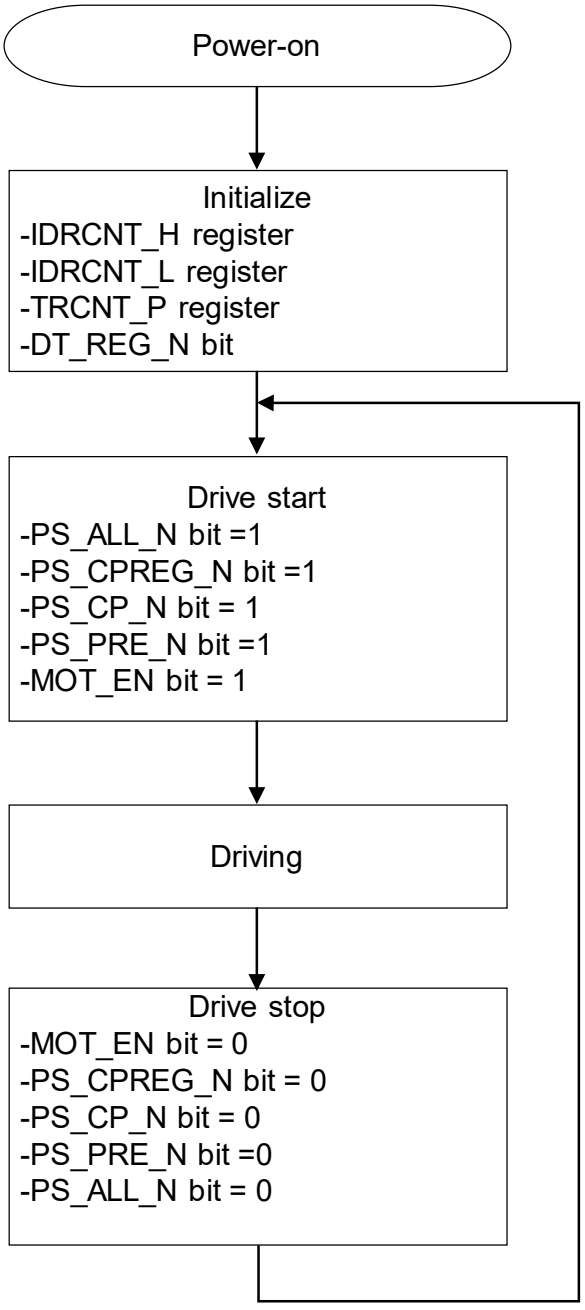
Related registers are as follows.

- ●High Side Output Current Capability Setting Register (IDRCNT_H)
- ●Low Side Output Current Capability Setting Register (IDRCNT_L)
- ●Pch Slew Rate Setting Register (TRCNT_P)
- ●Motor Drive Control Register (DRIVE_SET)
- ●Power Save Control Setting Register (PS_ALL)
- ●By Function Power Save Control Setting Register (PS)

<R> When using the dead time adjustment and slew rate adjustment function, do the setting as follows.

And be care of changing input signal for driving the Pre-Driver to be set after releasing power save of Pre-Driver.

Figure 2-11 Flowchart: Pre-Driver setting



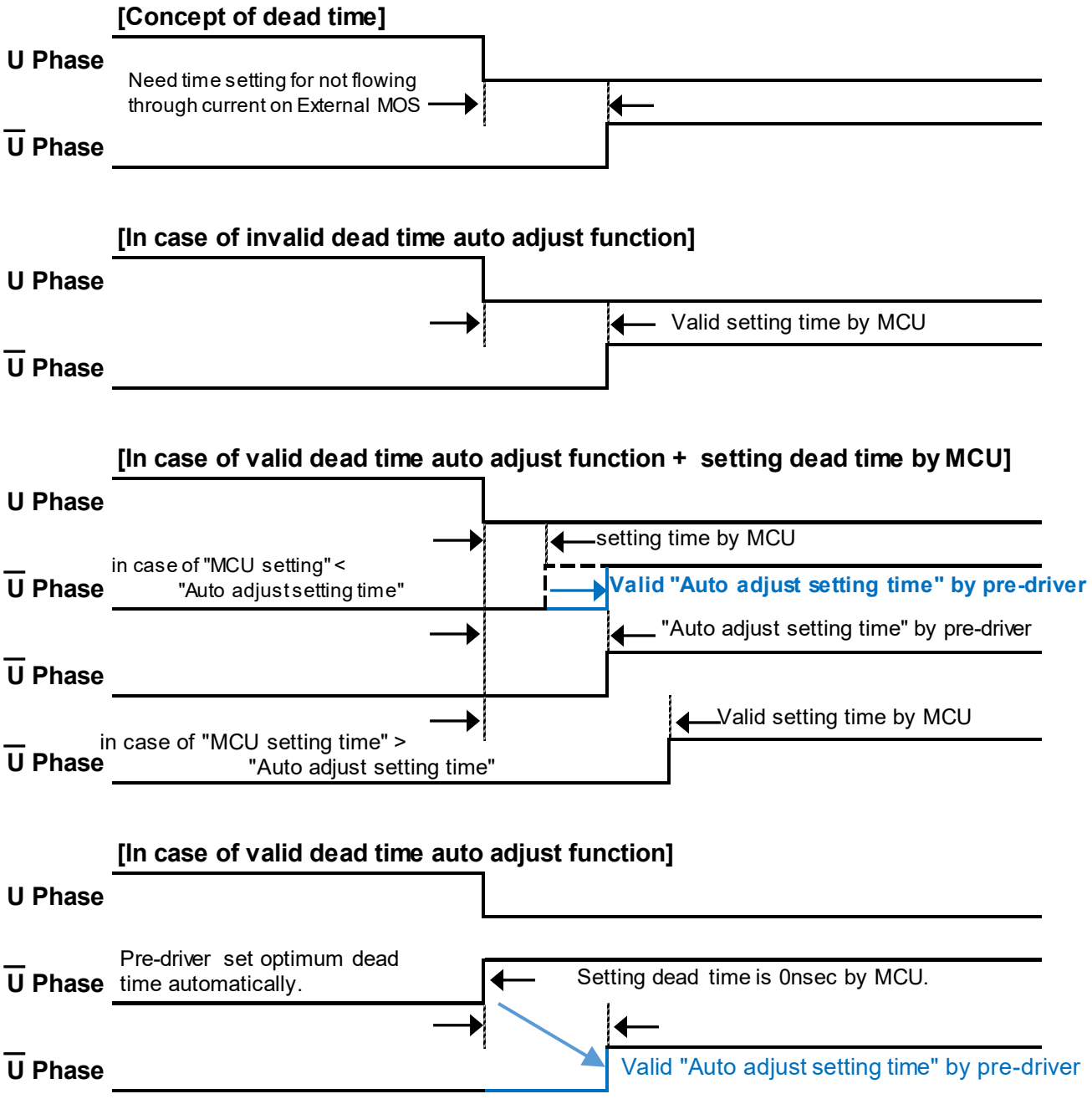
2.5.1.1 Dead time auto adjust function

Dead time Adjustment Enable bit (DT_REG_N) in the Motor Drive Control Setting Register (DRIVE_SET) can enable or disable the dead time adjustment function.

When this bit is enabled and the external MOS FET satisfy the condition on “1.5 How to select the external MOSFET”, it does not need to set dead time by MCU. and If there is enough dead time with the signal from the MCU, IC’s dead time adjustment function will be ineffective.

Renesas recommend keeping this function enable even if MCU has enough dead time for safety. Below are examples of waveforms when dead time adjustment function is Enable / Disable.

Figure 2-12 Dead time adjustment function Enable / Disable



2.5.2 5V Regulator Block

<R> When using the built-in 5V regulator, 5V is outputted from the VREG5 pin by fixing the VREG5_SEL pin to low. Note 1

This 5V regulator circuit detects about 5.7V (typ. design value) as an overvoltage detection function.

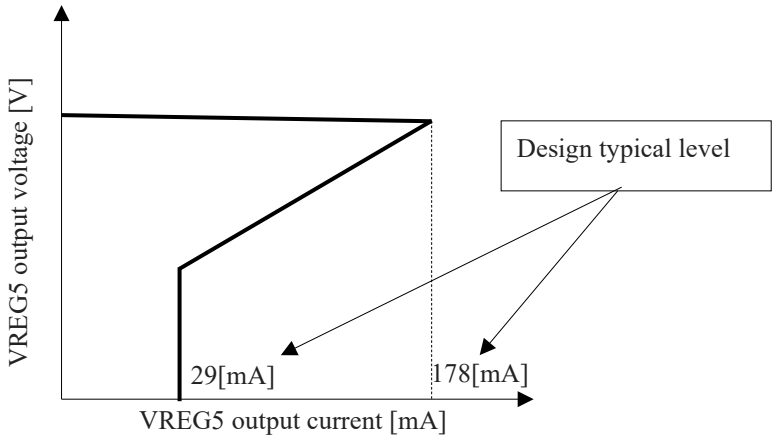
When TSD is detected, the 5V regulator stops and restarts when temperature falls below the TSD threshold. Please refer to TSD item for detailed functions.

When overcurrent is detected, current limit is applied according to the fold back current limit. (It is not recorded in the ALARM register.)

When using external 5V, please fix VREG5_SEL pin to high and supply 5V to VREG5 pin.

Note1: The output level of the 5V regulator after VM is supplied is about 4.8V.
By setting the trimming register, it can set to 5V. Please refer to “2.5.11.1 Built-in 5V regulator trimming"

Figure 2-13 Current characteristic of 5V regulator



2.5.3 Hall IC Comparator Block

The Pre-Driver has 3 channels of comparator corresponding to 3 Hall IC inputs. The outputs of the comparator are inputted to RL78/G1F and can be used for position sensing.

In addition, this Pre-Driver has functions to detect motor locked condition, commutation control, and FG (Frequency generator) judgment. When using commutation control must be satisfied "Figure 1-5 recommended drive waveform".

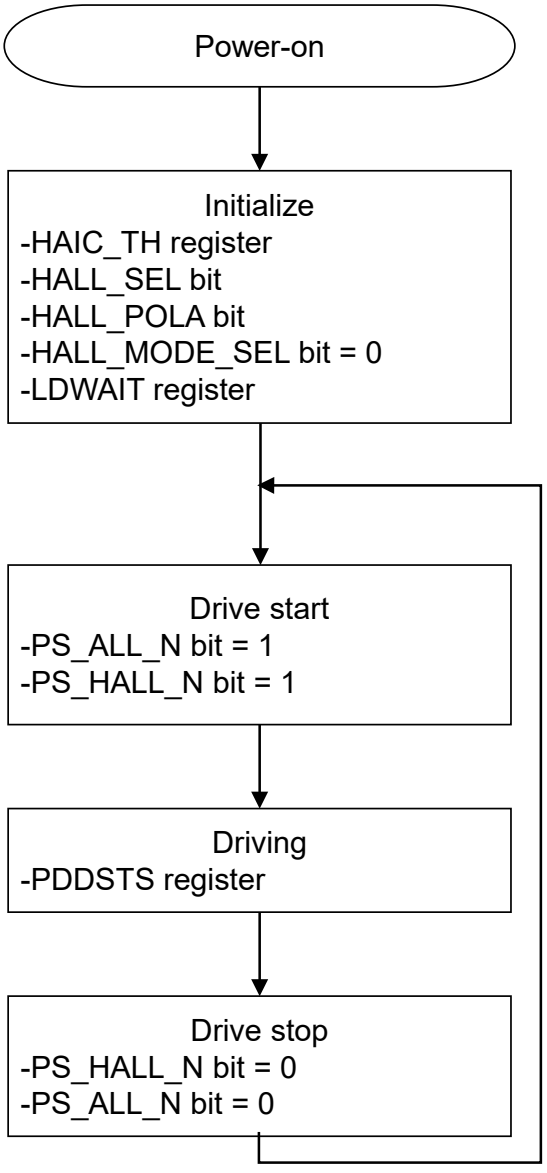
<R> When using this comparator, it is necessary to release power save mode by PS_ALL_N bit and PS_HALL_N bit.

Registers involved are as follows.

- Hall IC Threshold Adjustment Register (HAIC_TH)
- Hall Signal Processing Setting Register (HALL_SIG)
- LD Judgment Wait Time Register (LDWAIT)
- Power Save Control Register (PS_ALL)
- By Function Power Save Control Setting Register (PS)
- Motor Drive Control Setting Register (DRIVE_SET)
- Pre-Driver Drive Status Register (PDDSTS)

When using the Hall comparator function, do the setting in the following sequence.

Figure 2-14 Flowchart: Hall-IC comparator setting

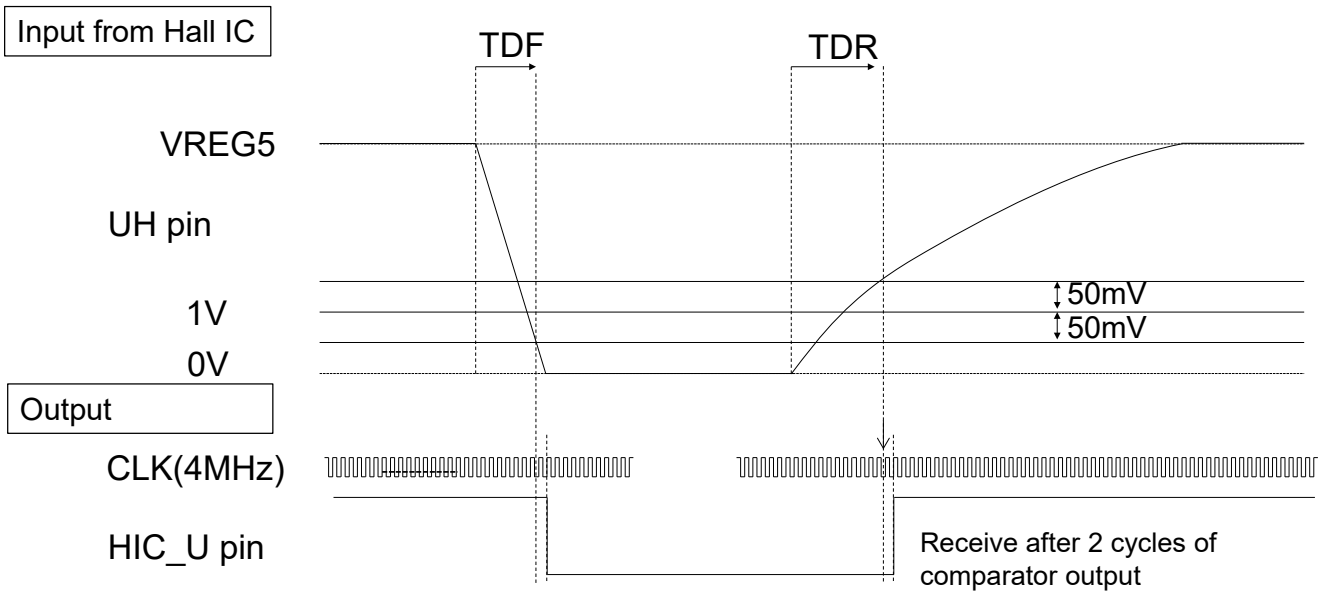


2.5.3.1 Hall IC Threshold Adjustment Register (HAIC_TH)

By setting the Hall IC Threshold Adjustment Register (HAIC_TH), it is possible to adjust the response performance by setting the threshold voltage and hysteresis voltage for the Hall IC input signal.

Below is an example of waveform when HA_TH = 010b (1V) and HAIC_HYS = 10b (100 mV).

Figure 2-15 Waveform of Hall-IC comparator.



2.5.4 Error Detection Block

This block monitors the driving state and detecting error condition, when detecting error state, following function is done and execute protect and report error.

- Store error signal into ALMSTS1 and ALMSTS2 register.
- Inform MCU error state by changing from Hi to Lo at ALARM terminal
- Stop drive external MOS FET

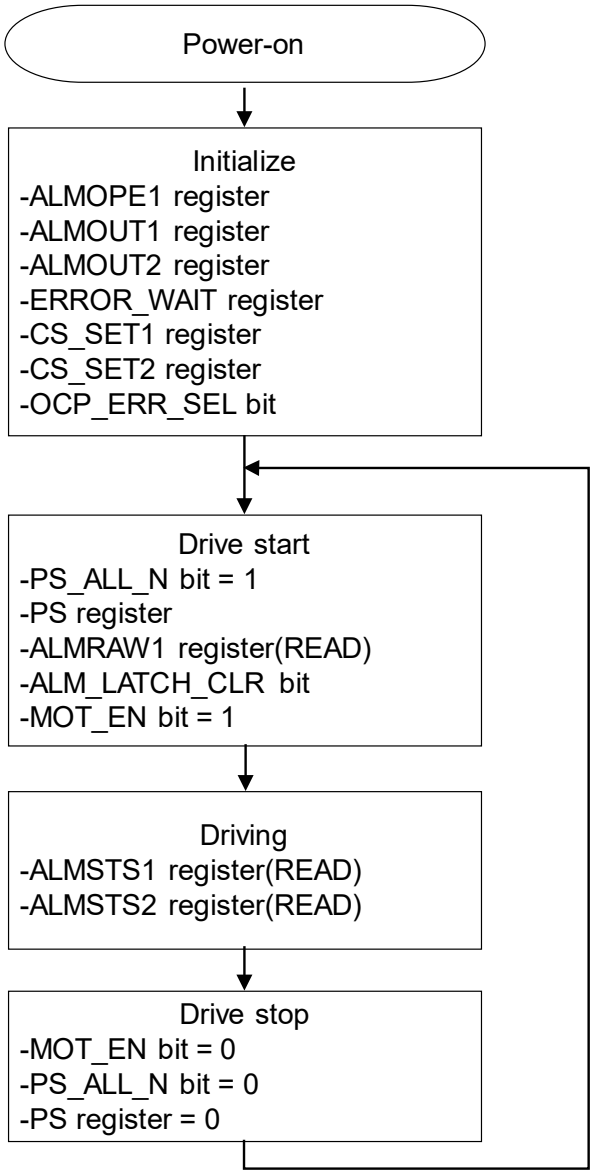
To detect error state, release of power save mode is needed on related function.

Related registers are as follows.

- ALARM Status Register1 (ALMSTS1)
- ALARM Operation Setting Register1 (ALMOPE1)
- ALARM Pin Output Setting Register1 (ALMOUT1)
- ALARM Status Monitor Register1 (ALMRAW1)
- ALARM Status Register2 (ALMSTS2)
- ALARM Pin Output Setting Register2 (ALMOUT2)
- Error Detection Waiting Time Setting Register (ERROR_WAIT)
- Motor Drive Control Setting Register (DRIVE_SET)
- Current Sense setting Register1 (CS_SET1)
- Current Sense setting Register2 (CS_SET2)
- Power Save Control Setting Register (PS_ALL)
- By Function Power Save Control Setting Register (PS)

When using the error detection function, do the setting in the following sequence.

Figure 2-16 Flowchart: Error detect setting



2.5.5 CS AMP Block

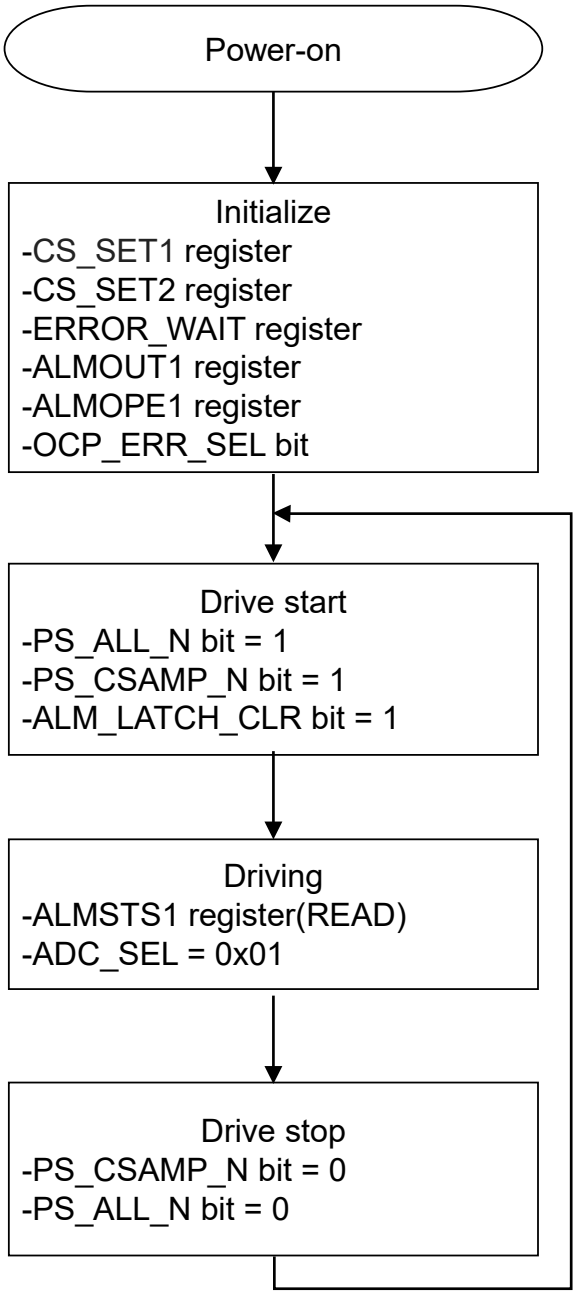
The CS Amp circuit detects the overcurrent condition by the potential difference generated across the shunt resistor.
Registers involved are as follows.

- ●Error Detection Wait Time Setting Register (ERROR_WAIT)
- ●ALARM Status Register1 (ALMSTS1)
- ●ALARM Pin Output Setting Register1 (ALMOUT1)
- ●ALARM Operation Setting Register1 (ALMOPE1)
- ●Current Sense setting Register1 (CS_SET1)
- ●Current Sense setting Register2 (CS_SET2)
- ●ADC Selector Register (ADC_SEL)

When using CS Amp function, do the setting in the following sequence.

<R>

Figure 2-17 Flowchart: CS AMP setting



2.5.5.1 Error Detection Wait Time Setting Register (ERROR_WAIT)

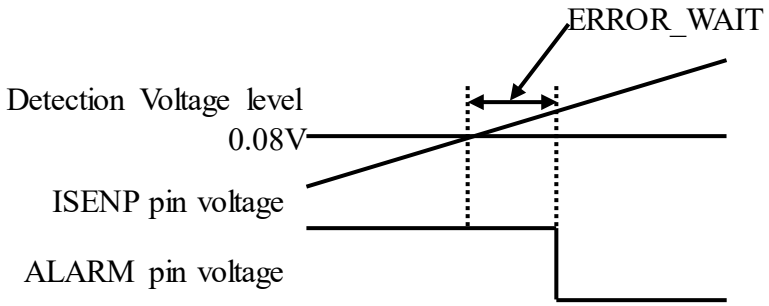
It sets the judgment time condition for overcurrent detection.

After the time set by the Output Phase Overcurrent Detection Judgment bit (OCP_WAIT) of the Error Detection Wait Time Setting Register (ERROR_WAIT), and when the overcurrent continued, the OCP_N bit of ALARM Status Register1 (ALMSTS1) is set to "0". The initial value will be without the wait time.

When OCP_ALE_N of ALARM Pin Output Setting Register1 (ALMOUT1) is enabled, the ALARM pin goes from high to low.

When OCP_OPE_N of ALARM Operation Setting Register1 (ALMOPE1) is enabled, the output of the Pre-Driver becomes low (external MOSFET: Hi-Z).

Figure 2-18 Example of Error detection of OCP (Detection voltage: 0.08V)



2.5.5.2 Current Sense setting Register 1,2 (CS_SET1, CS_SET2)

The overcurrent detection level is set by the combination of the “Current Sense setting Register1” (CS_SET1) and the “Current Sense setting Register2” (CS_SET2). At the “External MOSFET Over-Current Sense Setting Register1”, there are detection voltage gain adjustment (SHUNT_SEL) and threshold voltage setting (OCP_SEL_H) that determines the threshold.

In addition, setting the ADC Selector Register (ADC_SEL) to 0x01, the CS Amp output voltage can be monitored from the ANI7 pin.

The typical combinations of settings and the detection voltage values are shown in Table 2-40. The detection voltage value is the difference between the ISENP and the ISENN pin.

Table 2-40 Detection voltage threshold setting of CS amplifier

Detected voltage gain control	SHUNT_SEL	Setting Value	000(x50)			100(x25)	101(x8.25)
		1st AMP	x10			x5	x1.65
		2nd AMP	x5				
Detection voltage threshold control	CSAMP_IREF	Setting Value	00(x1)	01(x3)	10(x5)		
	CSAMP_ATT	Setting Value	1(x1)				
	OCP_SL_H	Setting Value	Detection potential difference[V] (ISENP-ISENN)				
		0000	0.016	0.044	0.07	0.14	0.44
		0001	0.018	0.050	0.08	0.17	0.50
		0010	0.020	0.057	0.09	0.19	0.56
		0011	0.023	0.063	0.10	0.21	0.62
		0100	0.025	0.069	0.11	0.23	0.69
		0101	0.027	0.076	0.12	0.25	0.75
		0110	0.029	0.082	0.13	0.27	0.81
		0111	0.032	0.088	0.14	0.29	0.87
		1000	0.034	0.094	0.15	0.31	0.93

An example of calculating the overcurrent detection level using a 0.5m ohm shunt resistor is shown below when setting the following registers.

The calculation formula of the overcurrent detection level is as follows.

●Detected current [A] = Detected voltage [V] / Shunt resistance value [ohm]

The registers settings.

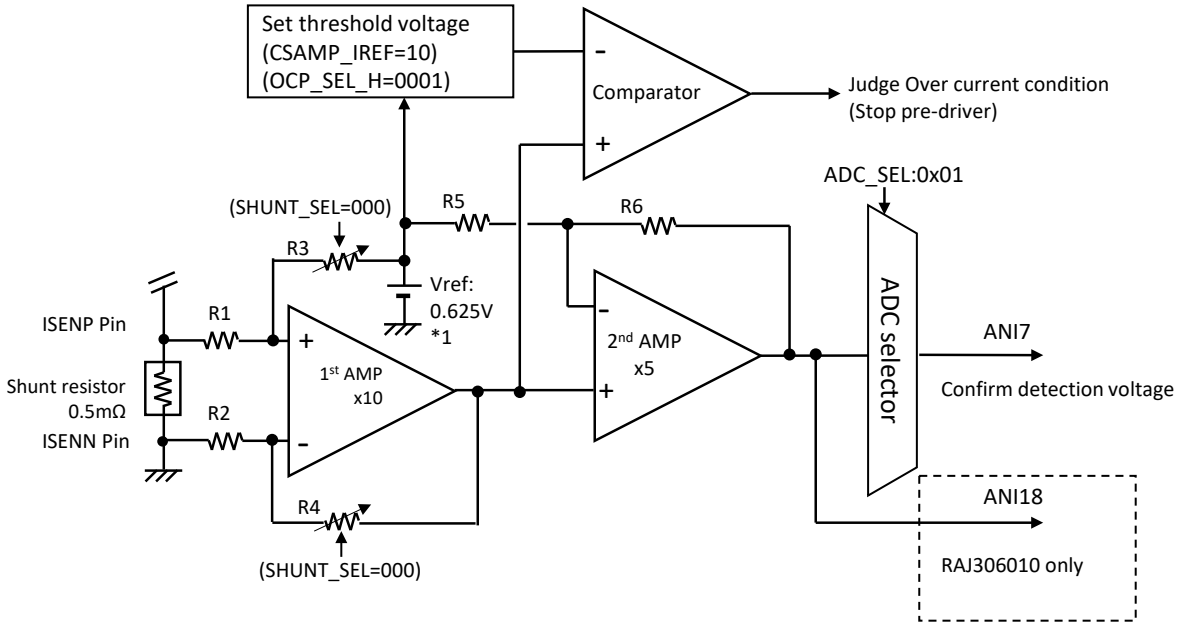
●SHUNT_SEL bit--- 000 (detected voltage x 50 times)
●CSAMP_IREF bit ---10 (threshold voltage x 5 times)
●CSAMP_ATT bit ---1 (threshold voltage x 1 time)
●OCP_SL_H bit ---0001 (detected voltage is decided as 0.08V)

The detected current is as follows.

●Detected current 160[A] = 0.08[V] / 0.5[m ohm]

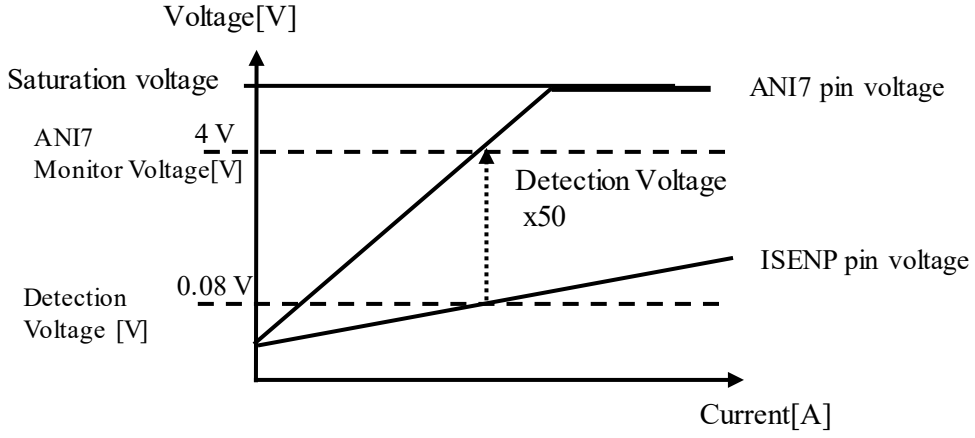
The waveform example at this time is shown below.

Figure 2-19 Equivalent circuit of CS AMP



*1: In case of setting as follows.
CSAMP_TRIM5="1" and CSA="1" at "CSAMP_TRIM" register.
(This setting is recommended value when using over current detection function))

Figure 2-20 Pin voltage level of ISENP pin and ANI7 pin



2.5.6 Charge Pump Block

The charge pump circuit generates high side drive gate voltage (VGT) and low side drive gate voltage (VGB). When using this function, it is necessary to release power saving by PS_ALL_N bit, PS_CPREG_N bit, and PS_CP_N bit.

Registers involved are as follows.

- ●Charge Pump Setting Register1 (CPSET1)
  When PS_CP_N is “1”, setting change on CPSET is prohibited.
- ●Charge Pump Setting Register2 (CPSET2)
- ●ALARM Status Register1 (ALMSTS1)
- ●ALARM Operation Setting Register1 (ALMOPE1)
- ●ALARM Pin Output Setting Register1 (ALMOUT1)
- ●ALARM Status Monitor Register1 (ALMRAW1)

When using the charge pump function, do the setting in the following order.

Figure 2-21 Flowchart: Charge pump

<R>

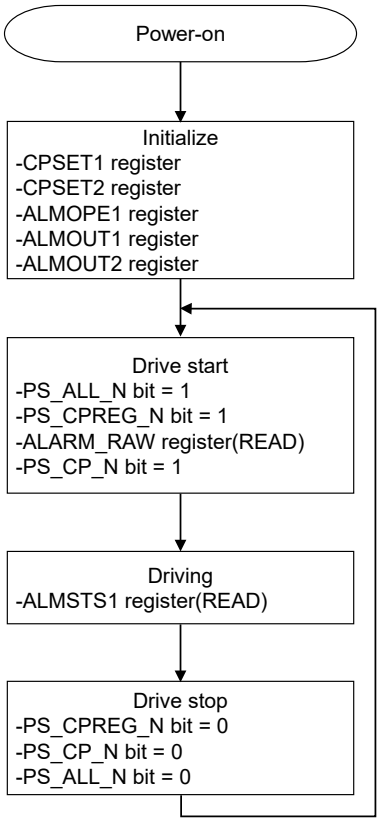
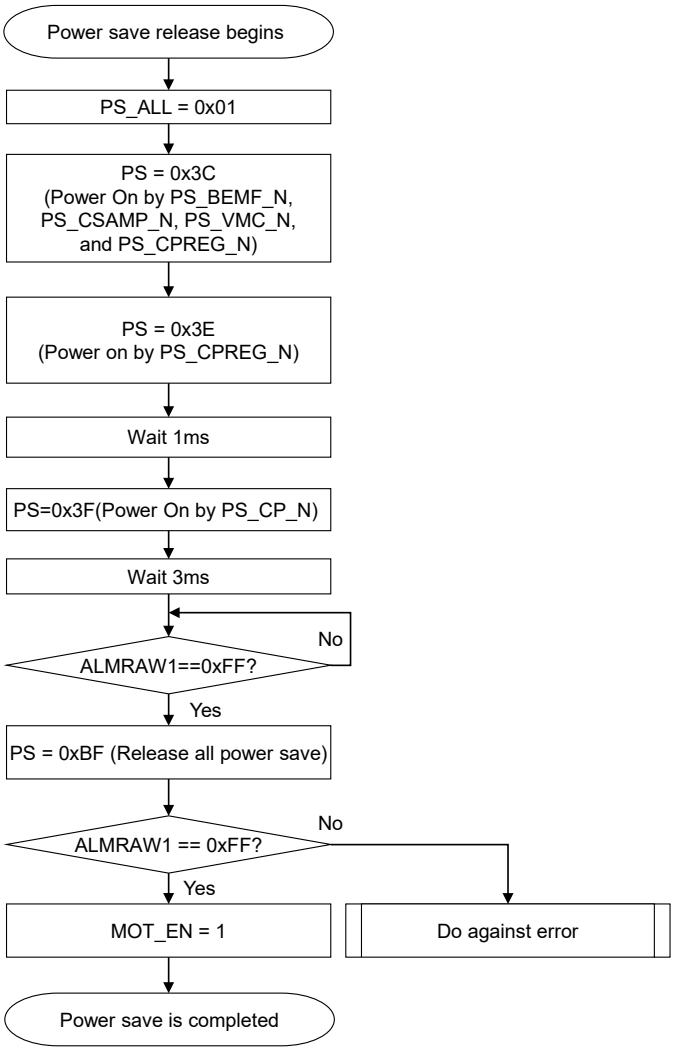


Figure 2-22 Flowchart of release power save



2.5.6.1 ALARM Status Register1 (ALMSTS1)

The charge pump has overvoltage and low voltage detection function.

- The VGB low voltage is detected when VGB is less than 7.6V. The VGB_UVP_N bit is set to "0".
- The VGB overvoltage is detected when VGB is more than 18V. The VGB_OVP_N bit is set to "0".
- The VGT low voltage is detected when it is below “VM +7V”. The VGT_UVP_N bit is set to "0".
- The VGT overvoltage 1 is detected when voltage is over “VM +18V”.
  The VGT_OVP1_N bit is set to “0”.
- The VGT overvoltage 2 and when over 48V. The VGT_OVP2_N bit is set to “0”.
  The VGT overvoltage 2 threshold depends on the product.
  RAJ306001: 48V or more, RAJ306010: 60V or more

The detected result is output to the ALARM pin and can be confirmed by reading the ALMSTS1 register.

Each detection voltage is the same for the double boost function and the non-boost function.

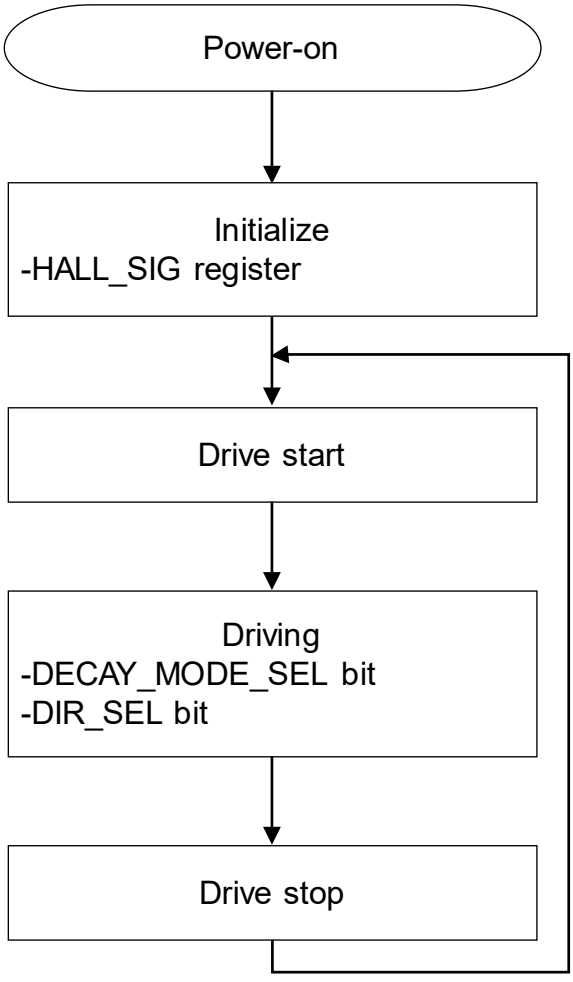
2.5.7 Commutation Block

Set the motor control method setting with the following registers.

- Motor Drive Control Setting Register (DRIVE_SET/DECAY_MODE)
- Hall Signal Processing Setting Register (HALL_SIG)

The registers setting order are shown below.

Figure 2-23 Flowchart: commutation drive mode setting



There are “PWM control” and “Commutation control” as the method of motor control, and PWM control is selected as the initial value.

In commutation control, current flows through the body diode of external MOSFET in the same direction as PWM control. Figure 2-24 and Figure 2-25 show the current path of both PWM and commutation control.

Figure 2-26 shows PWM waveform and commutation waveform.

At the commutation control, the circuit masks the gray portion against the PWM waveform.

Figure 2-24 Current path of PWM control

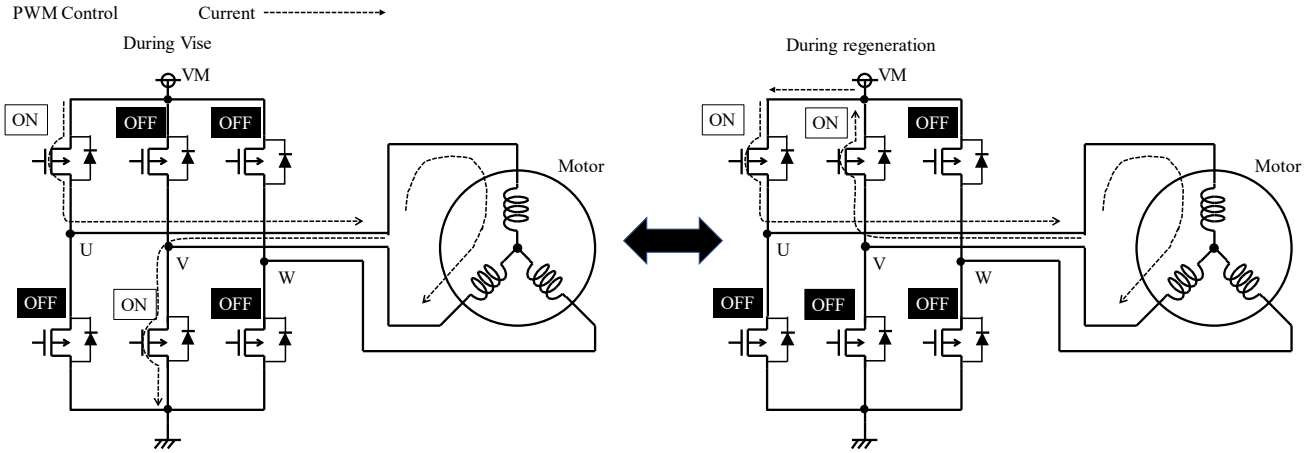


Figure 2-25 Current path of commutation control

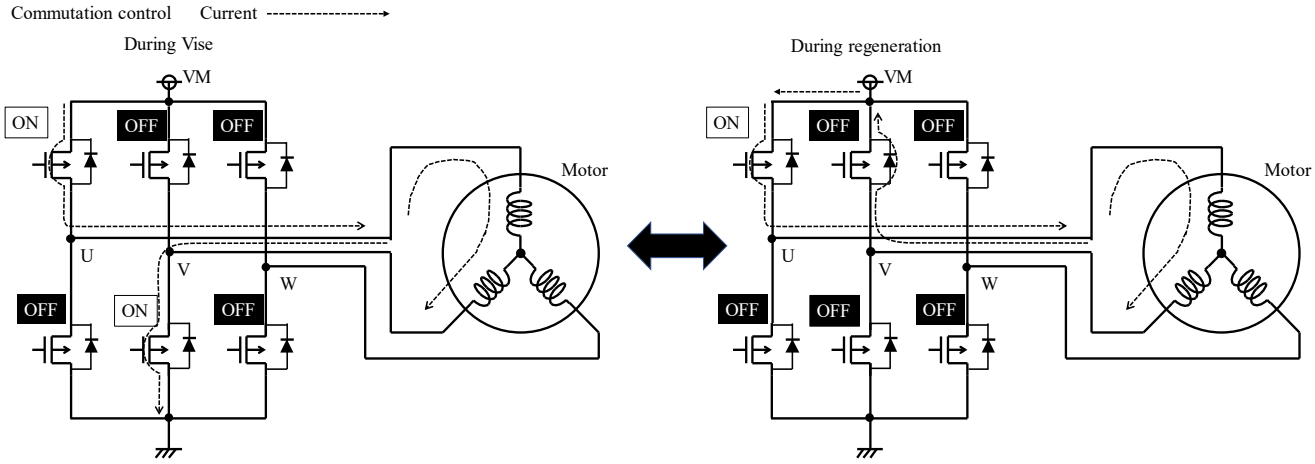
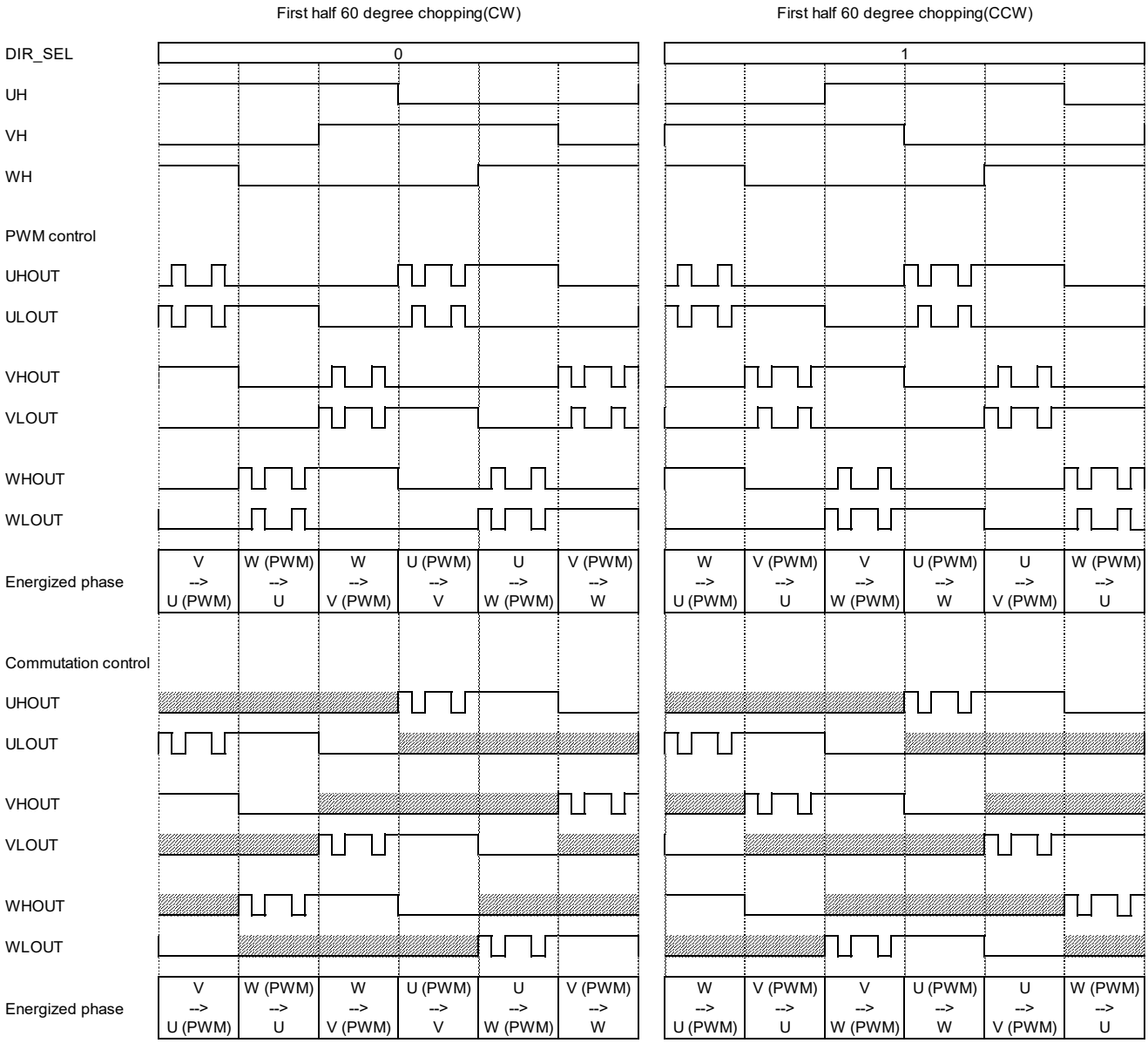


Figure 2-26 PWM control waveform and Commutation control waveform



2.5.8 TSD (Thermal Shut Down) Block

Regardless of the power save register, the TSD circuit starts its operation when the supply voltage is applied to the VM terminal.

When the junction temperature exceeds 150degree C overheating is detected, and the driving operation of Pre-Driver is stopped, and the power supply from the built-in 5V regulator is stopped.

When the junction temperature decreases 140degree C, the power supply of the 5V regulator is restarted. At this time, the Pre-Driver register holds the state before TSD detection.

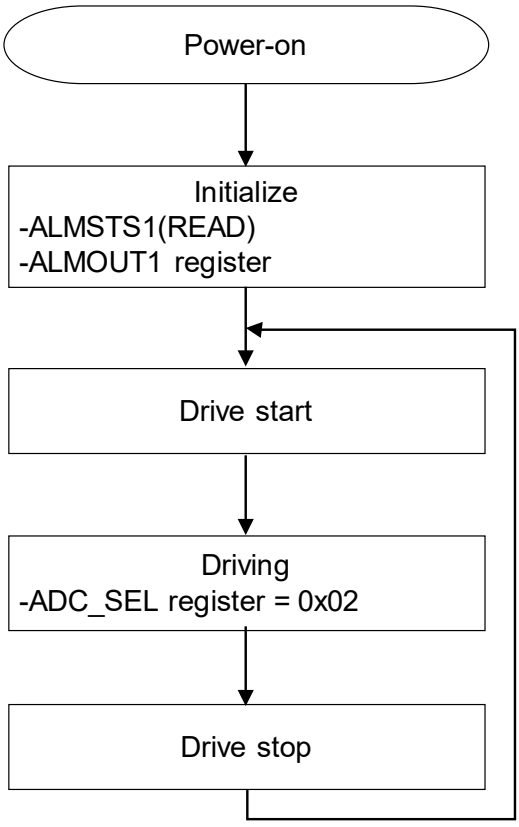
In addition, the junction temperature of the chip can be monitored by selecting TSD with the ADC_SEL register.

The registers involved are as follows.

- ADC Selector Register (ADC_SEL)
- ALARM Status Register1 (ALMSTS1)
- ALARM Pin Output Setting Register1 (ALMOUT1)

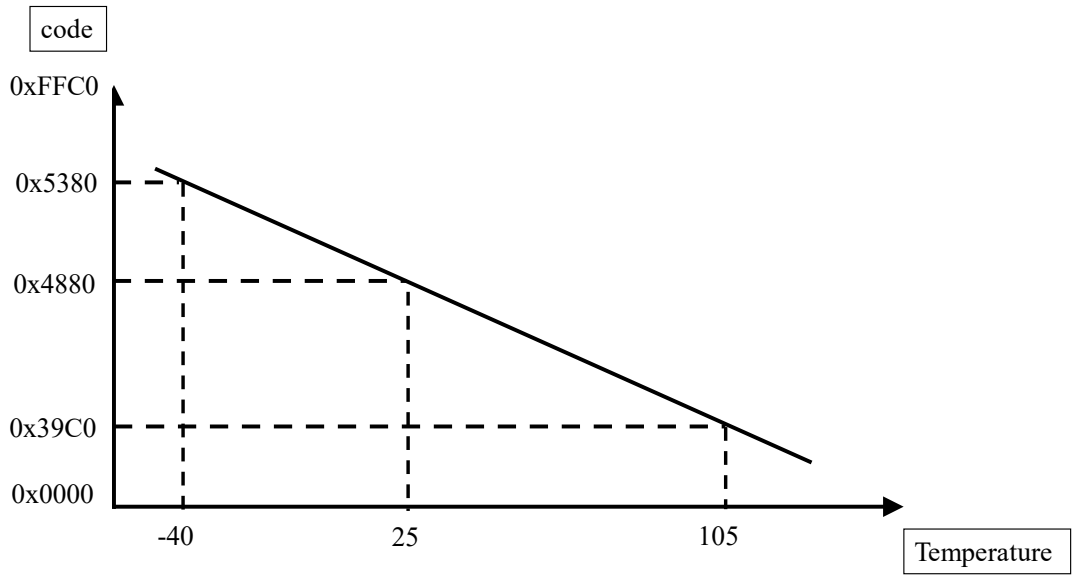
The registers setting order are shown below.

Figure 2-27 Flowchart: TSD



By setting the ADC Selector Register (ADC_SEL) to 0x02, the code output from the ANI7 pin can be monitored.
The relationship between code output from ADC_SEL and temperature is shown below.

Figure 2-28 TSD circuit and ADC result (ADCR register code)



Note. The code value in the graph is derived from the average result.
The formula for obtaining the temperature per bit is as follows.

(-40 - 105) / (0x5380 – 0x39C0) = -0.022 [degC/code]

<R>
The correction value for 25 degC (TSD_25) is stored in the address 0xeffef of RL78/G1F. The format is signed 8 bits.
When reading the temperature information via ANI7, calculate as follows.

Tj_now = (ADC result – (0x4880 + TSD_25 * 64)) * -0.022 + 25 [degC]

And Address 0xeffef is located in the far area, so access to this area should be far accessed using a pointer.
For the trimming data storage area, refer to “2.5.11 Trimming Register”.

2.5.9 Voltage Monitor (VMC) Block

The voltage monitor (VMC) section outputs a signal obtained by attenuating the VM voltage. The attenuation gain (RVM) is 1/9.23 times for RAJ306001 and 1/12.92 times for RAJ306010.

Registers involved are as follows.

- ADC Selector Register (ADC_SEL)
- ALARM Status Register2 (ALMSTS2)
- ALARM Pin Output Setting Register2 (ALMOUT2)
- Power Save Control Setting Register (PS_ALL)
- By Function Power Save Control Setting Register (PS)

By setting the ADC Selector Register (ADC_SEL) to 0x00 (default value), the VMC output can be inputted to the ADC in RL78/G1F.

The voltage obtained by multiplying the VM voltage by 1/RVM due to resistor division in the circuit is inputted to the RL78/G1F port ANI7 and converted to a digital code by the 10-bit ADC in RL78/G1F.

The maximum VM voltage that can be monitored depends on the product. For RAJ306001 it will be about 36.87V and for RAJ306010 it will be about 51.62V.

At this time, the maximum value of the digital code output by the 10-bit AD in RL78/G1F is about 0xCC80.Below is a graph showing the block diagram of the VMC circuit and the relationship between VM and ADC (ADCR).

Figure 2-29 Equivalent circuit of VMC

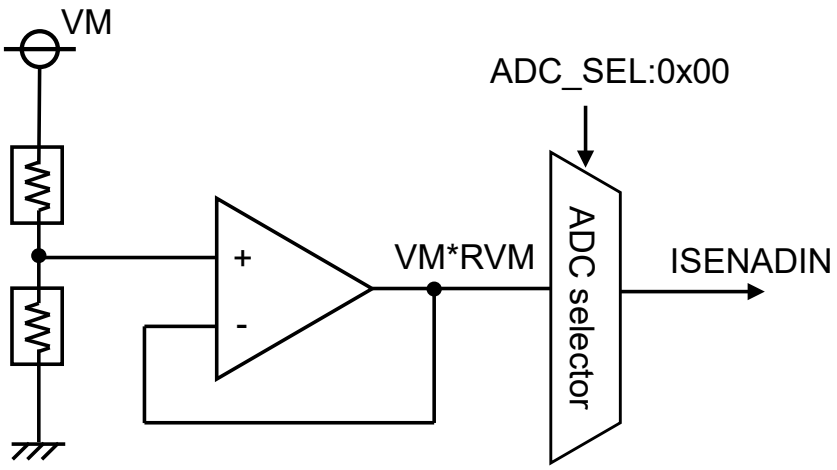
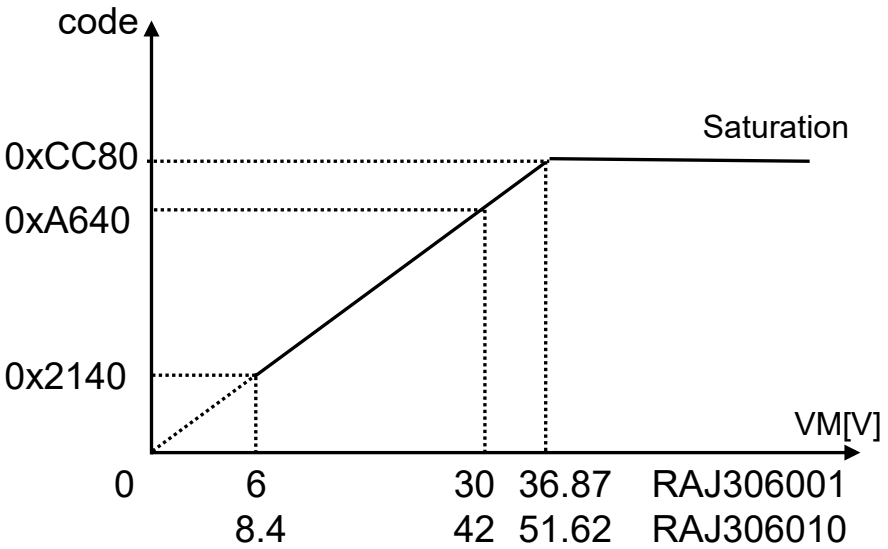


Figure 2-30 Relation of VM terminal voltage and ADC

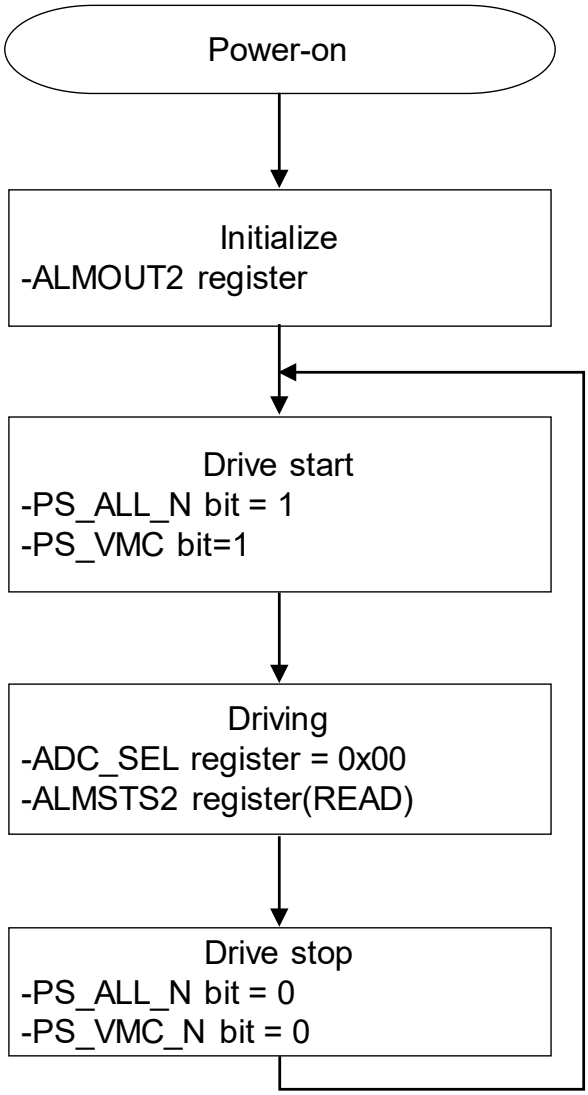
<R>



The register setting order is as follows.

Figure 2-31 Flowchart: VMC

<R>



2.5.10 BEMF Amp Block

BEMF Amp is a differential amplifier used for BEMF voltage measurement. BEMF AMP outputs 1.0 times the input differential voltage that is half the voltage of VREG5 (5V regulator) as the center.

When measuring BEMF, it outputs the difference voltage from the voltage of Vn (Virtual Neutral Point) made from COMMON (motor midpoint) voltage or U / V / W phase voltage and one selected phase voltage among U / V / W phase voltage.

Figure 2-32 Equivalent circuit of BEMF

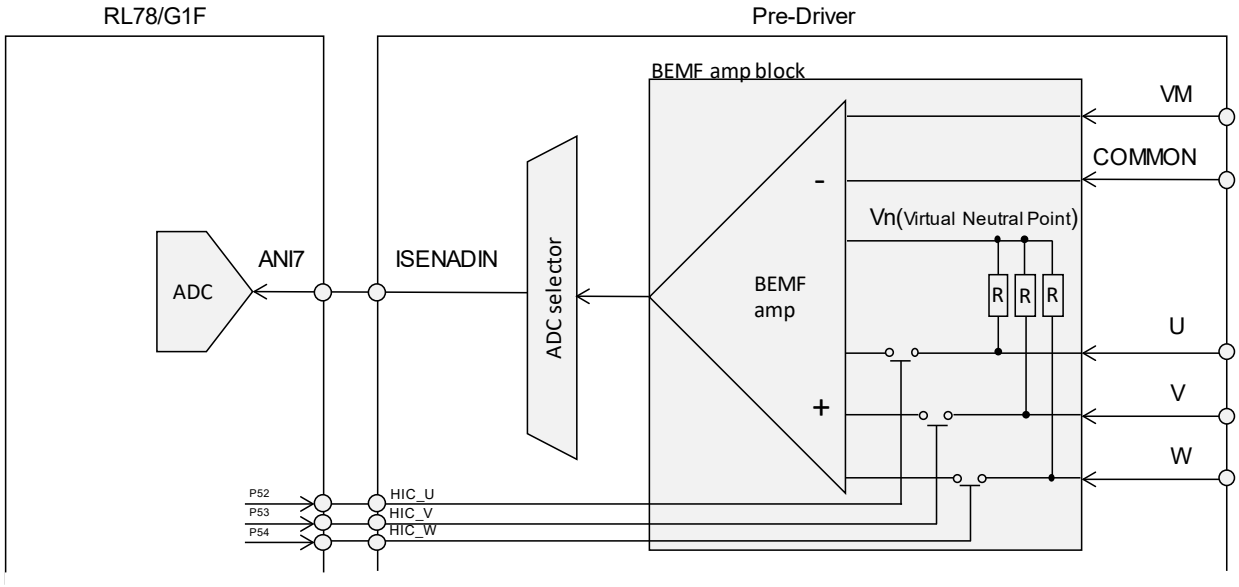
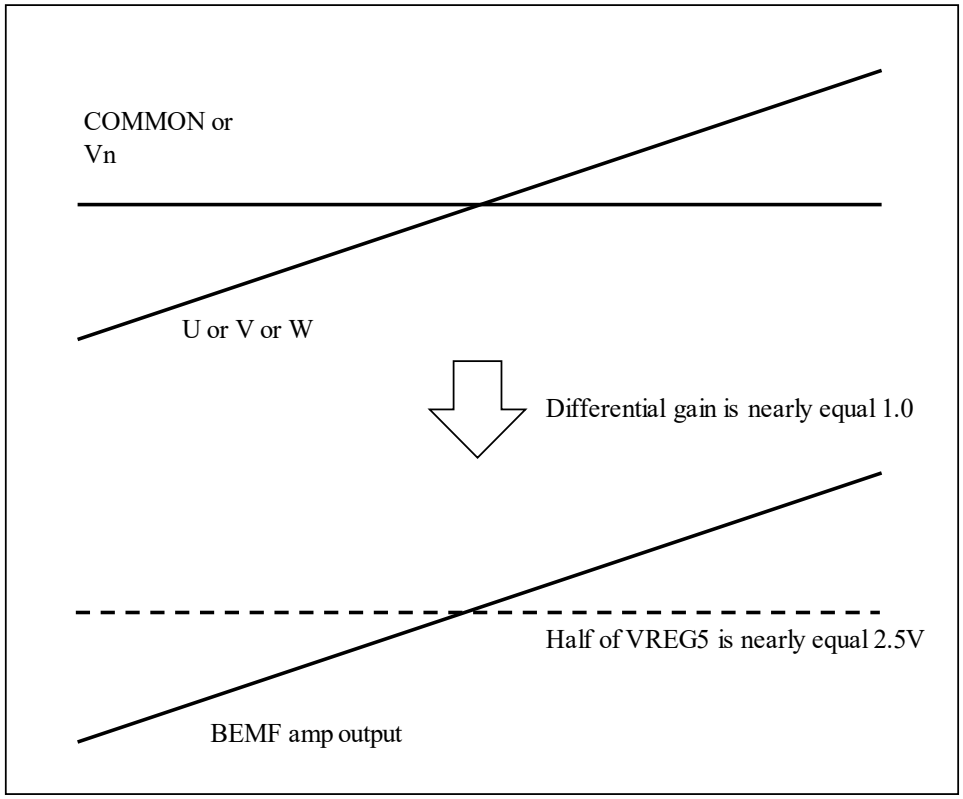


Figure 2-33 Relationship of BEMF Input Voltage and output voltage (ANI7)



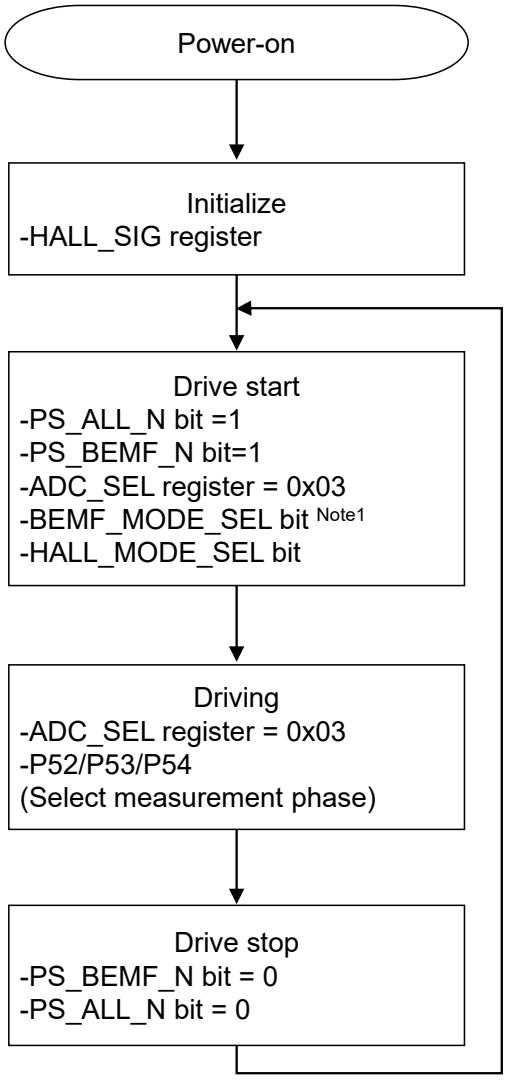
The registers involved are as follows.

- ADC Selector Register (ADC_SEL)
- Hall Signal Processing Setting Register (HALL_SIG)
- Power Save Control Setting Register (PS_ALL)
- By Function Power Save Control Setting Register (PS)
- Motor Drive Control Setting Register (DRIVE_SET)

Register setting order is as follows.

Figure 2-34 Flowchart: BEMF AMP

<R>



Note 1:RAJ306001 and RAJ306010 have different specifications when measuring BEMF amplifier output with ADC using ANI7 of RL78/G1F.

- RAJ306001

  -ADC_CH_SEL bit :"3"

  -BEMF_MODE_SEL bit : "1"

- RAJ306010

  -ADC_CH_SEL bit : "3"

  -BEMF_MODE_SEL bit : When the BEMF amplifier output from WH pin "1", when not in output "0"
  The RAJ306010 can output and monitor the BEMF amplifier signal from the WH pin by setting the BEMF_MODE_SEL bit.
  When outputting the BEMF amplifier signal, set the BEMF_MODE_SEL bit to "1". However, be careful that when outputting the BEMF amplifier signal from the WH terminal, if an external circuit is attached, it will also affect the output to ANI17.

2.5.11 Trimming Register Block

The trimming information of Pre-Driver are stored into the trimming region of RL78/G1F.

By using trimming data, the accuracy of VREG5's 5V output, and the CS amplifier's detect level can be increased.

Address 0xeffef is located in the far area, so access to this area should be far accessed using a pointer.

Access example by C-language: (* (__ far const uint 8 _ t *) (0xEFFECU));

Table 2-6 shows the trimming data storage region of RL78/G1F and the stored trimming data.

Table 2-41 RL78/G1F trimming data storage region

		BIT							
		7	6	5	4	3	2	1	0
SYMBOL [ADDRESS]	TRIM_DATA0 [0xeffec]	VREG5_TRIM_3 - VREG5_TRIM_0 (4bit)				CSAMP_TRIM_3 - CSAMP_TRIM_0 (4bit)			
	TRIM_DATA1 [0xeffed]	X	X	X	BGR_TRIM_4 - BGR_TRIM_0				
	TRIM_DATA2 [0xeffee]	X	X	X	BFAMP_TRIM_5 - BFAMP_TRIM_1				
	TRIM_DATA3 [0xeffef]	TSD_25_7 - TSD_25_0							

The following registers are related to the trimming.

- ●Charge Pump Trimming Register (CP_TRIM)
- ●5V Regulator Voltage Setting Register (VREG5_TRIM)
- ●External MOSFET Current Sensing AMP Setting Register (CSAMP_TRIM)
- ●Trimming Protect Register (TRIM_PT)
- ●Trimming Data Enable Register (TRIM_EN)
- ●High Accuracy BGR Temperature Correction Register (BGR_TRIM)
- ●BUFFAMP Absolute Value Correction Register (BFAMP_TRIM)

2.5.11.1 Built-in 5V Regulator Trimming

The registers that are related to the trimming of the built-in 5V regulator are the VREG5_TRIM register, TRIM_PT register, TRIM_EN register, BGR_TRIM register, and BFAMP_TRIM register. After the confirmation of the communication, please perform the initialization with the following procedures.

1.Trimming Protect release (TRIM_PT = 0x95)
2.BGR setting (BGR_TRIM = TRIM_DATA1 & 0x1F)
3.Buffer amplifier setting (BFAMP_TRIM = (TRIM_DATA2<<1) & 0x3E)
4.Valid the trimming data (TRIM_EN = 0x01)
5.Trimming Protect setting (TRIM_PT = 0x00)
6.VREG5 Absolute Value correction (VREG5_TRIM = (TRIM_DATA0 >> 4) | 0x20)

2.5.11.2 CS Amplifier Trimming

The register related to the CS amplifier trimming is the CSAMP_TRIM register. Please perform the following setting after the setting of the built-in 5V regulator.

1.CS Amplifier trimming (CSAMP_TRIM = (TRIM_DATA0 & 0x0f) | 0x20)

2.5.11.3 Charge Pump Trimming

There is a CP_TRIM register that acts as a trimming register for the charge pump.

When there is no special instruction, do not change from the initial value (00h).

1.Charge Pump trimming (CP_TRIM = 0x00): Optional

CHAPTER 3 RL78/G1F

3.1 Outline of RL78/G1F built in RAJ306000 series

RAJ306000 Series has built-in RL78/G1F of 64pin(R5F11BLEGFB) as MCU. However, built-in RL78/G1F has usage restrictions. This chapter describes the setting of register, restrictions and notes on RL78/G1F for using of this IC. For detailed information on each function, refer to the “RL78/G1F User’s Manual Hardware (R01UH0516E).

Peripheral functions with restrictions are shown below.

- PIN FUNCTIONS
- CLOCK GENERATOR
- TIMER ARRAY UNIT
- TIMER RJ
- TIMER RD
- TIMER RG
- REAL-TIME CLOCK
- 12-BIT INTERVAL TIMER
- CLOCK OUTPUT/BUZZER OUTPUT CONTROLLER
- WATCHDOG TIMER
- A/D CONVERTER
- D/A CONVERTER
- COMPARATOR (CMP)
- PROGRAMMABLE GAIN AMPLIFIER
- SERIAL ARRAY UNIT
- IrDA
- DATA TRANSFER CONTROLLER (DTC)
- EVENT LINK CONTROLLER (ELC)
- INTERRUPT FUNCTIONS
- KEY INTERRUPT FUNCTIONS
- POWER-ON-RESET CIRCUIT
- VOLTAGE DETECTOR
- OPTION BYTE
- ON-CHIP DEBUG FUNCTION

Peripheral functions without restrictions are shown below.

- TIMER RX
- SERIAL INTERFACE IICA
- STANDBY FUNCTION
- RESET FUNCTION
- SAFETY FUNCTION
- REGULATOR
- FLASH MEMORY
- BCD CORRECTION CIRCUIT
- WATCH DOG TIMER

3.2 Register setting of RL78/G1F for using RAJ306000 Series

Use below setting for Peripheral I/O redirection register 0 to 3 (PIOR0, PIOR1, PIOR2, PIOR3).

Table 3-1 Peripheral I/O redirection register 0 (PIOR0)

<R>

Peripheral I/O redirection register 0(PIOR0)			
Bit name	Value	Function	Note
PIOR07	0	Assign INTP8 function to P42.	-
		Assign INTP10 function to P76.	-
		Assign INTP11 function to P77.	-
	1	Assign INTP8 function to P00.	-
		Assign INTP10 function to P01.	-
		Assign INTP11 function to P20.	-
PIOR06	0	Cannot be used.	Set to 0.
PIOR05	0	Cannot be used.	Set to 0.
PIOR04	0	Assign PCLBUZ1 function to P141.	-
		Assign INTP5 function to P16.	P16 is used as timer RD.
PIOR03	0	Assign PCLBUZ0 function to P140.	-
	1	Assign PCLBUZ0 function to P31.	-
PIOR02	0	Assign SCLA0 function to P60.	-
		Assign SDAA0 function to P61.	-
PIOR01	0	Assign RxD2 function to P14.	P14 is used as timer RD.
		Assign TxD2 function to P13.	P13 is used as timer RD.
		Assign SCL20/SCK20 function to P15.	P15 is used as timer RD.
		Assign SDA20/SI20 function to P14.	P14 is used as timer RD.
		Assign SO20 function to P13.	P13 is used as timer RD.
		Assign TxD0/SO00 function to P51.	SO00(CSI00) is used for communication with Pre-Driver.
		Assign RxD0/SI00 function to P50.	SI00(CSI00) is used for communication with Pre-Driver.
		Assign SCL00 function to P30.	P30 is used as CSI00.
		Assign SDA00 function to P50.	P50 is used as CSI00.
		Assign SCK00 function to P30.	SCK00(CSI00) is used for communication with Pre-Driver.
PIOR00	1	Assign INTP1 function to P52.	INTP1 is used to receive interrupt by HIC_U.
		Assign INTP2 function to P53,	INTP2 is used to receive interrupt by HIC_V.
		Assign INTP3 function to P54.	INTP3 is used to receive interrupt by HIC_W.
		Assign INTP4 function to P55.	INTP4 is used to receive interrupt by ALARM.
		Assign INTP9 function to P43.	-

<R>

Table 3-2 Peripheral I/O redirection register 1 (PIOR1)

Peripheral I/O redirection register 1(PIOR1)			
Bit name	Value	Function	Note
PIOR13, PIOR12	10	Assign TRJO0 function to P00.	TRJO0 pin is not used. CSI00 function is used with P50 pin and P30 pin.
PIOR11, PIOR10	11	Assign TRJIO0 function to P06.	TRJIO0 is used as system-clock [4MHz] for Pre-Driver.

<R> Table 3-3 Peripheral I/O redirection register 2 (PIOR2)

Peripheral I/O redirection register 2(PIOR2)			
Bit name	Value	Function	Note
PIOR27	0	Can not be used.	Set to 0.
PIOR26	0	Assign TRDIOD0 function to P14.	-
PIOR25	0	Assign TRDIOD1 function to P10.	-
PIOR24	0	Assign TRDIOC1 function to P11.	-
PIOR23	0	Assign TRDIOB1 function to P12.	-
PIOR22	0	Assign TRIOA1 function to P13.	-
PIOR21	0	VCOUT1 is no assignment.	This bit is used in combination with PIOR32 bit Since P70 is an unoutput terminal, the VCOUT1 function cannot be used regardless of PIOR32.
	1	Assign VCOUT1 function to P31.	
PIOR20	0	VCOUT10 is no assignment.	Since both P71 and P120 are non-output terminals, the VCOUT0 function cannot be used separately for setting.
	1	VCOUT10 is no assignment.	

<R> Table 3-4 Peripheral I/O redirection register 3 (PIOR3)

Peripheral I/O redirection register 3(PIOR3)			
Bit name	Value	Function	Note
PIOR32	0	VCOUT1 output to port pins is disabled (fixed to low level)	This bit is used in combination with PIOR 21 bit Since P70 is an unoutput terminal, the VCOUT0 function cannot be used when PIOR21 is 1.
	1	VCOUT1 output to port pins is enabled (output from pins specified in PIOR21 bit)	
PIOR31	0	VCOUT0 output to port pins is disabled (fixed to low level)	Since both P71 and P120 are non-output terminals, the VCOUT0 function cannot be used separately for setting.
	1	VCOUT0 output to port pins is enabled (output from pins specified in PIOR20 bit)	

3.3 Restriction of RL78/G1F

3.3.1 PIN FUNCTIONS

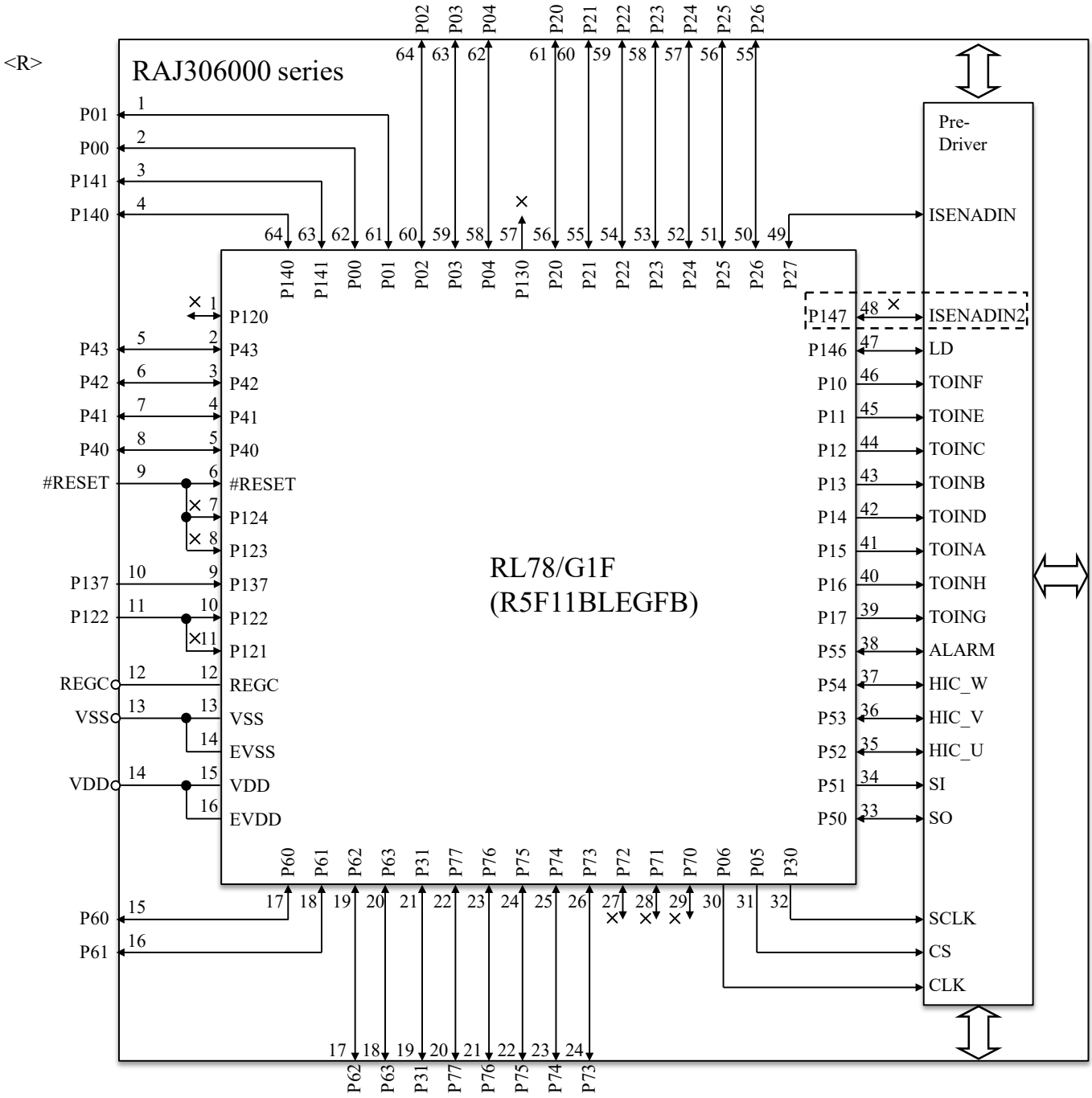
3.3.1.1 Pin configuration of RL78/G1F

This product incorporates the RL78/G1F 64Pin product (R5F11BLEGFB) as a pre-driver controller MCU.

Figure 3-1 shows the pin configuration of RL78/G1F(64pin).

"x" means unconnected pins. So do the settings according to Table 3-9.

Figure 3-1 Pin configuration of RL78/G1F



3.3.1.2 PIN FUNCTION of RL78/G1F

RAJ306000 Series using RL78/G1F 64pin version, however RAJ306000 Series have some restriction. Some pins are no connection or internal connection. Show the pin function of RL78/G1F.

Table 3-5 Pin function of RL78/G1F (1/4)

PORT name	Function name	RAJ3060xx	Note
P20	ANI0	external pin	
P21	ANI1	external pin	
P22	ANI2	external pin	
P23	ANI3	external pin	
P24	ANI4	external pin	
P25	ANI5	external pin	
P26	ANI6	external pin	
P27	ANI7	Internal connection	ANI7 is internally connected to the ISENADIN terminal.
P03	ANI16	external pin	
P02	ANI17	external pin	
<R> P147	ANI18	not available /Internal connection	RAJ306001 : Not available. This pin is open. RAJ306010 : Internal connection with ISENADIN2 of Pre-Driver.
P120	ANI19	not available	P120 is no output terminal.
P10	ANI20	not available	P10 is used as timer RD
P11	ANI21	not available	P11 is used as timer RD
P12	ANI22	not available	P12 is used as timer RD
P13	ANI23	not available	P13 is used as timer RD
P14	ANI24	not available	P14 is used as timer RD
P22	ANO0	external pin	
P23	ANO1	external pin	
P137	INTP0	external pin	
P52	INTP1	Internal connection	P52 is internally connected to the HIC-U terminal. Set to 1 for PIOR00 bit.
P53	INTP2	Internal connection	P53 is internally connected to the HIC-V terminal. Set to 1 for PIOR00 bit.
P54	INTP3	Internal connection	P54 is internally connected to the HIC-W terminal. Set to 1 for PIOR00 bit.
P55	INTP4	Internal connection	P55 is internally connected to the ALARM terminal. Set to 1 for PIOR00 bit.
P16,(P12)	INTP5	not available	Select with PIOR04 bit. Both P16 and P12 are used for timer RD.
P140	INTP6	external pin	
P141	INTP7	external pin	
P42,(P00)	INTP8	external pin	Select with PIOR07 bit.
P43	INTP9	external pin	Set to 1 for PIOR00 bit.
P76,(P01)	INTP10	external pin	Select with PIOR07 bit.
P77,(P20)	INTP11	external pin	Select with PIOR07 bit.
P14	IrRxD	not available	P14 is used as timer RD.
P13	IrTxD	not available	P13 is used as timer RD.
P22	IVCMP0	external pin	

xx = 01,10

Table 3-6 Pin function of RL78/G1F (2/4)

<R>

PORT name	Function name	RAJ3060xx	Note
P147	IVREF0	not available /Internal connection	RAJ306001 : Not available. This pin is open. RAJ306010 : Internal connection with ISENADIN2 of Pre-Driver.
P02	IVCMP10	external pin	
P03	IVCMP11	external pin	
P20	IVCMP12	external pin	
P21	IVCMP13	external pin	
P70	KR0	not available	P70 is no output terminal.
P71	KR1	not available	P71 is no output terminal.
P72	KR2	not available	P72 is no output terminal.
P73	KR3	external pin	
P74	KR4	external pin	
P75	KR5	external pin	
P76	KR6	external pin	
P77	KR7	external pin	
P140,(P31)	PCLBUZ0	external pin	Select with PIOR03 bit.
P141,(P55)	PCLBUZ1	external pin	Select with PIOR04 bit. P55 is not available. Because P55 is no output terminal.
P22	PGAI	external pin	
P23	PGAGND	external pin	
REGC	REGC	external pin	
P30	RTC1HZ	not available	P30 is used as CSI00.
RESET	RESET	external pin	
P50,(P16)	RxD0	not available	P50 is used as CSI00. P16 is used as timer RD.
P03	RxD1	external pin	
P14	RxD2	not available	P14 is used as timer RD. Set PIOR01 bit to 0 (For allocation of CSI00).
P30	SCK00	Internal connection	P30 is internally connected to the SCLK terminal.
P75	SCK01	external pin	
P04	SCK10	external pin	
P10	SCK11	not available	P10 is used as timer RD.
P15	SCK20	not available	P15 is used as timer RD.
P70	SCK21	not available	P70 is no output terminal.
P60	SCLA0	external pin	Set to 1 for PIOR02 bit.
P30	SCL00	not available	P30 is used as CSI00.
P75	SCL01	external pin	
P04	SCL10	external pin	
P10	SCL11	not available	P10 is used as timer RD.
P15	SCL20	not available	P15 is used as timer RD.

xx = 01,10

Table 3-7 Pin function of RL78/G1F (3/4)

PORT name	Function name	RAJ3060xx	Note
P70	SCL21	not available	P70 is no output terminal.
P61	SDAA0	external pin	Set to 1 for PIOR02 bit.
P50	SDA00	not available	P50 is used as CSI00.
P74	SDA01	external pin	
P03	SDA10	external pin	
P11	SDA11	not available	P11 is used as CSI00.
P14	SDA20	not available	P14 is used as CSI00.
P71	SDA21	not available	P71 is no output terminal.
P50	SI00	Internal connection	P50 is internally connected to the SO terminal. Set to 0 for PIOR01 bit.
P74	SI01	external pin	
P03	SI10	external pin	
P11	SI11	not available	P11 is used as timer RD.
P14	SI20	not available	P14 is used as timer RD.
P71	SI21	not available	P71 is no output terminal.
P51	SO00	Internal connection	P51 is internally connected to the SI terminal. Set to 0 for PIOR01 bit.
P73	SO01	external pin	
P02	SO10	external pin	
P12	SO11	not available	P12 is used as timer RD.
P13	SO20	not available	P13 is used as timer RD.
P72	SO21	not available	P72 is no output terminal.
P62	SSI00	external pin	This function is not used in RAJ306000.
P00	TI00	external pin	
P16	TI01	not available	P16 is used as timer RD.
P17	TI02	not available	P17 is used as timer RD.
P31	TI03	external pin	
P01	TO00	external pin	
P16	TO01	not available	P16 is used as timer RD.
P17	TO02	not available	P17 is used as timer RD.
P31	TO03	external pin	
P06	TRJIO0	Internal connection	P06 is internally connected to the CLK terminal. Set to 1 for PIOR10 bit and PIOR11 bit.
P00	TRJO0	external pin	This function is not used in RAJ306000. Set to 0 for PIOR12 bit and set to 1 for PIOR11 bit.
P17	TRDCLK	Internal connection	This function is not used in RAJ306000.
P17	TRDIOA0	Internal connection	P17 is internally connected to the TOING terminal.
P15	TRDIOB0	Internal connection	P15 is internally connected to the TOINA terminal.
P16	TRDIOC0	Internal connection	P16 is internally connected to the TOINH terminal.

xx = 01,10

Table 3-8 Pin function of RL78/G1F (4/4)

PORT name	Function name	RAJ3060xx	Note
P14	TRDIOD0	Internal connection	P14 is internally connected to the TOIND terminal. Set to 1 for PIOR26 bit.
P13	TRDIOA1	Internal connection	P13 is internally connected to the TOINB terminal. Set to 1 for PIOR22 bit.
P12	TRDIOB1	Internal connection	P12 is internally connected to the TOINC terminal. Set to 1 for PIOR23 bit.
P11	TRDIOC1	Internal connection	P11 is internally connected to the TOINE terminal. Set to 1 for PIOR22 bit.
P10	TRDIOD1	Internal connection	P10 is internally connected to the TOINF terminal. Set to 1 for PIOR25 bit.
P50	TRGIOA	not available	P50 is used as CSI00.
P51	TRGIOB	not available	P51 is used as CSI00.
P00	TRGCLKA	external pin	
P01	TRGCLKB	external pin	
P51	TxD0	not available	P51 is used as CSI00.
P02	TxD1	external pin	
P13	TxD2	not available	P13 is used as a timer RD. Set PIOR01 bit to 0.
P120,(P71)	VCOUT0	not available	P120 and P71 are no output terminal. Set to 0 for PIOR20 bit and PIOR31 bit.
P31	VCOUT1	Internal connection	To assign function to P31, set to 1 for PIOR21 and set to 0 for PIOR32. Not assing this function , set to 0 for PIOR21 and PIOR32.
P121	X1	not available	P121 is no output terminal.(Internally connected with P122.)
P122	X2	not available	P121 is no output terminal.(Internally connected with P122.)
P122	EXCLK	external pin	
P124	EXCLKS	not available	P124 is no output terminal.(Internally connected with RESET.)
P123	XT1	not available	P123 is no output terminal.(Internally connected with RESET.)
P124	XT2	not available	P124 is no output terminal.(Internally connected with RESET.)
VDD	VDD	external pin	
VDD	EVDD0	Internal connection	Common with VDD pin.
P20	AV_{REFP}	external pin	
P21	AV_{REFM}	external pin	
VSS	VSS	external pin	
VSS	EVSS0	Internal connection	Common with VSS pin.
P50	TOOLRxD	not available	P50 is used as CSI00.
P51	TOOLTxD	not available	P51 is used as CSI00.
P40	TOOL0	external pin	

xx = 01,10

3.3.1.3 Connection of Unused Pins

The following shows pin processing of unused pins.

<R>

Table 3-9 Connection of unused pins according to the state of pre-driver (1/2)

Pin name	Pin number	Connection	Recommended processing
P00	62	external	Input mode : Independently connect to VDD or VSS via resistor. Output mode : Leave open.
P01	61		
P02	60		
P03	59		
P04	58		
P20	56		
P21	55		
P22	54		
P23	53		
P24	52		
P25	51		
P26	50		
P31	21		
P40	5		
P41	4		
P42	3		
P43	2		
P60	17	external	Input mode : Independently connect to VDD or VSS via resistor. Output mode : Set the port's output latch to 0 and leave the pins open, or set the port's output latch to 1 and independently connect the pins to VDD or VSS via resistor.
P61	18		
P62	19		
P63	20		
P70	29	OPEN	Select output.
P71	28		
P72	27		
P73	26	external	Input mode : Independently connect to VDD or VSS via resistor. Output mode : Leave open.
P74	25		
P75	24		
P76	23		
P77	22		
P120	1	OPEN	Select output.
P121	11	external	Set to input. This pin is common with P122 pin.
P122	10	external	Input mode : Connect to VDD or VSS via resistance.
P123	8	external	Set to input. This pin is common with reset pin.
P124	7		
P130	57	OPEN	Select output.
P137	9	external	Input mode : Connect to VDD or VSS via resistance.
P140	64	external	Input mode : Connect to VDD or VSS via resistance. Output mode :Leave open.
P141	63		
P147	48	OPEN	Select output. Note 1
REGC	12	external	Connect to VSS via a capacitor(0.47uF to 1uF)
RESET	6	external	Connect to VDD direct or via resistance.

Note1 P147 is connected to ISENADIN2 terminal only for RAJ306010. Please follow the settings on this page for RAJ306001.

Table 3-10 Connection of unused pins according to the state of pre-driver (2/2)

Pin name	Pin number	Connection	Recommended processing	
			During clock supply.	When stopping clock or VM supply.
P05	31	Internal	Output mode : Output CS signal for CSI00	Set to 0 at output latch and select output mode.
P06	30		Set TRJIO0 and output 4MHz clock	
P10	46		Select timer RD or GPIO output.	
P11	45			
P12	44			
P13	43			
P14	42			
P15	41			
P16	40			
P17	39			
P30	32		Select SCK00(CSI00) function.	
P50	33		Select SI00(CSI00) function	
P51	34		Select SO00(CSI00) function.	
P52	35		When HALL_MODE_SEL=0 : Select INTP function. When HALL_MODE_SEL=1 : Select output mode.	
P53	36			
P54	37			
P27	49		Select ANI7 function.	
P147	48		Select input mode.*Note[1]	Please set either one. -Set to 0 at output latch and select output mode. -Set Pull-Up and use it as an input function.
P146	47		Select input mode.	Set the input port.
P55	38		Select INTP4 function.	

Note.1:Only RAJ306010 P147 is connected to the ISENADIN 2 terminal. Set RAJ306001 according to Table 3-9

3.3.2 CLOCK GENERATOR

Table 3-11 shows the spec of clock.

Table 3-11 Clock pin

Pin name	RAJ3060xx
X1,X2 pins	-
EXCLK pin	P122
XT1, XT2 pins	-
EXCLKS pin	-

Note1.This IC has built-in RL78/G1F of 64pin. However, X1 pin, XT1 pin, XT2 pin, and EXCLKS pin are no available. Because these pins are not output.

3.3.3 TIMER ARRAY UNIT

Table 3-12 shows input and output pin for TIMER ARRAY UNIT.

When timer input and timer output are shared by the same pin, either function can be used.

Table 3-12 Timer I/O Pins provided

		RAJ3060xx
Unit 0	Channel 0	TI00,TO00
	Channel 1	-
	Channel 2	-
	Channel 3	TI03/TO03

3.3.4 TIMER RJ

Timer RJ should be used to supply the system clock (4MHz) to Pre-Driver.

3.3.5 TIMER RD

Please use Timer RD by (1) Complementary PWM mode, (2) Reset synchronous PWM mode or (3) Timer mode as PWM function.

However, when using the Timer mode, it is necessary to change the terminal connection of RL78/G1F and the Pre-Driver by setting the “SELSIG_U register”, “SELSIG_V register”, “SEL_SIG_W register” and “PWM_SEL bit” of “HALL_SIG register”.

And When using the built-in dead-off time adjustment function in Pre-Driver, it is unnecessary for the timer RD to control the short circuit prevention time.

<R> .t is prohibited to set Hi-Z of output at pulse forced cutoff control by following registers.

1.Timer RD digital filter function select register (TRDDF0, TRDDF1)

2.PWMOPA cutoff control register (OPDF0, OPDF1)

The reason is that the input level of pre-driver would not be fixed.

3.3.6 TIMER RG

Function by using TRGIOA pin and TRGIOB pin cannot be used. Because TRGIOA pin and TRGIOB pin are used to communication to Pre-Driver. So, these two terminals cannot be used for Timer RG.

3.3.7 REAL-TIME CLOCK

The subsystem clock cannot be used as a clock source. Because XT1 pin, XT2 pin and EXCLKS Pin are not outputted. Only constant-period interrupt interval is available with Low-speed OCO (On chip oscillator) clock.

3.3.8 12-BIT INTERVAL TIMER

The subsystem clock cannot be used as a clock source. Because XT1 pin, XT2 pin and EXCLKS Pin are not outputted. Select Low-speed OCO, when use this function.

3.3.9 CLOCK OUTPUT/BUZZER OUTPUT CONTROLLER

PCLBUZ0 function cannot be assigned to P31 pin.

PCLBUZ1 function cannot be assigned to P55 pin, too.

3.3.10 WATCHDOG TIMER

When using the interval interrupt of the watchdog timer, please keep the following procedure to reset the watchdog timer counter.

1. Set the WDTIMK bit in interrupt mask flag register 0 (MK0L) to 1 before clearing the counter of the watchdog timer.
2. Clear the counter of the watchdog timer.
3. Wait at least 80u sec.
4. Clear the WDTIIF bit in interrupt request flag register 0 (IF0L) to 0.
5. Clear the WDTIMK bit in interrupt mask flag register 0 (MK0L) to 0.

For details of this limitation, refer to the technical update (TN-RL*-A086A/E) of RL78/G1F.

3.3.11 A/D CONVERTER

Channel below cannot be used as a channel of A / D converter.

ANI18, ANI19, ANI20, ANI21, ANI22, ANI23, ANI24

And low-voltage mode also cannot be used.

3.3.12 D/A CONVERTER

The operation of the D / A converter is not guaranteed. (Not tested with this product.)

3.3.13 COMPARATOR (CMP)

The operation of the comparator is not guaranteed. (Not tested with this product.)

3.3.14 PROGRAMMABLE GAIN AMPLIFIER (PGA)

The operation of the programmable gain amplifier is not guaranteed. (Not tested with this product.)

3.3.15 SERIAL ARRAY UNIT (SAU)

This IC uses CSI00 to communicate to Pre-Driver as Table 3-13. And the SSI00 terminal function is not used by the CSI00 control. So please set to 0 on the SSIE00 bit.

Table 3-13 Serial Array unit usage restrictions

Unit	Cannel	CSI	UART	Simplicity IIC
0	0 [PKG internal connect]	CSI00 (Slave select not available) [PKC internal connect]		
	1	CSI01		IIC01
	2	CSI10	UART1(TxD1)	IIC10
	3		UART1(RxD1)	
1	0			
	1			

3.3.16 IrDA

This function cannot be used in this IC.

3.3.17 DATA TRANSFER CONTROLLER (DTC)

Due to the pin configuration, there are factors that cannot be used as the DTC activation factor in this IC.

3.3.18 EVENT LINK CONTROLLER (ELC)

Due to the pin configuration, there are factors that cannot be used as the ELC activation factor in this IC.

3.3.19 INTERRUPT FUNCTIONS

Due to the pin configuration, there are factors that cannot be used as the Interrupt activation factor in this IC.

3.3.20 KEY INTERRUPT FUNCTION

KR0, KR1 and KR2 pin cannot be used in this IC

3.3.21 POWER-ON-RESET CIRCUIT

Set one of the following values at user option byte (000C1H/010C1H) in this IC.
- -0x61(Interrupt mode)
- -0x62(Interrupt and reset mode)
- -0x63(reset mode)

3.3.22 OPTION BYTE

Set one of the following values at user option byte (000C1H/010C1H) in this IC.
- -0x61(Interrupt mode)
- -0x62(Interrupt and reset mode)
- -0x63(reset mode)

3.3.23 FLASH MEMORY

Do not support FLASH memory access by dedicated UART
(TOARTTxD terminal and TOOLRxD terminal).

CHAPTER 4 Sequence Example

4.1 Start-up Sequence

4.1.1 Built-in 5V regulator

With the use of the built-in 5V regulator, the sequence example is shown below when starting up.

1. Start supplying 5V regulator. (VM applied)
2. Initialize the timer RJ, serial array unit (CSI00), timer RD, and other peripheral functions.
3. Start the timer RJ and serial array unit.
4. Perform the initial settings of the pre-driver.
   a. Trimming setting. (5V regulator, CS amplifier)
   b. Initial setting. (PWM, HALL signal connection selection, slew rate setting)
   c. Release power-save. (PS_ALL=1, PS=0xBF) * For details, refer to "2.5.6 Charge pump section".
   d. Permit motor drive. (MOT_EN bit = 1U)
5. Start timer RD.

4.2 Stop Sequence

4.2.1 STOP mode

1. Stop Timer RD.
2. Stop Pre-Driver.
   a. Stop motor drive. (MOT_EN bit = 0U)
   b. Set power-save mode. (PS_PRE_N = 0, PS_CPREG_N = 0, PS_CP_N = 0)
3. Stops the operation of timer RJ, serial array unit (CSI00), and other various functions.
4. Set masks for interrupts of peripheral functions not used for release.
5. Set the PORT for STOP. (Refer to "3.3.1.3 Pin processing")
6. Set STOP release interrupt
7. Execute STOP instruction.

4.2.2 SNOOZE mode

With the use of the A/D converter (ANI6) and the 12-bit interval timer (100ms), the example of the SNOOZE operation is shown below.

1. Stop timer RD.
2. Stop Pre-Driver.
   a. Prohibit motor drive. (MOT_EN bit = 0U)
   b. Set power-save mode. (PS_PRE_N = 0, PS_CPREG_N = 0, PS_CP_N = 0)
3. Stops the operation of timer RJ, serial array unit (CSI00), and other various functions.
4. Set masks for interrupts of peripheral functions not used for release.
5. Set PORT mode for SNOOZ.
6. Set the 12-bit interval timer. (return setting)
   a. Set 12-bit interval timer input clock supply. (RTCEN = 1U)
   b. Stop operating the 12-bit interval timer. (ITMC = 0x0000)
   c. Set 12-bit interval timer interrupt. (ITMK = 1U, ITIF = 0U)
   d. Set the cycle of 12-bit interval timer. (ITMC = 0x05DB)
7. Set A/D converter. (recovery setting)
   a. Supply clock for A/D converter. (ADC_EN = 1)
   b. Stop AD conversion. (ADM = 0x00, ADMK = 1U, ADIF = 0U)
   c. Set the interrupt priority of AD conversion. (ADPR1 = 1U, ADPR0 = 1U)
   d. Set AD conversion channel for recovery. (PMC2 = 0x40, PM2 = 0x40)
   e. Set the select mode.
      Set the conversion clock.
      Set the conversion start time.
      Set the comparator operation. (ADM0 = 0x31)
   f. Selects hardware trigger wait mode.
      Select one-shot conversion mode.
      Select AD conversion by INTIT factor. (ADM1 = 0xE3)
   g. Select VDD or VSS as the reference for A/D conversion.
      Select the interrupt method for comparator operation.
      Select 10-bit precision. (ADM2 = 0x00)
   h. Set return threshold. (ADUL = 0xB3, ADLL = 00)
   i. Set the target conversion channel. (ADS = 1)
8. Starting of A/D conversion.
   a. Stop conversion of AD converter. (ADCS = 0U, ADCE = 0U)
   b. Allow the AD converter interrupt. (ADIF = 0U, ADMK = 0U)
   c. Select snooze mode. (AWC = 1U)
   d. Allows the operation in the compare mode. (ADCE = 1U)
9. Start 12-bit interval timer. (ITMC| = 0x8000)
10. Execute STOP instruction.

CHAPTER 5 Attention to use

5.1 Operation in high temperature

Assuming temperature profile which this IC is used for household appliance motor, electric power tool, etc. is as follows.

[RAJ306001GFN / RAJ306010GFN]

High temp. environment:	55degC < Ta <= 85degC	2.4hrs/day
Not High temp. environment:	-40degC < Ta <= 55degC	21.6hrs/day

[RAJ306001ZGFN / RAJ306010ZGFN]

High temp. environment1:	85degC < Ta <= 105degC	0.5hrs/day
High temp. environment2:	55degC < Ta <= 85degC	3.5hrs/day
Not High temp. environment:	-40degC <= Ta <= 55degC	20.0hrs/day

APPENDIX A REVISION HISTORY

A. 1 Major Revisions in This Edition (REV.2.02) from REV2.00

Page	Description	Classification
Chapter1 Outline		
P.2	Typo Function of terminal diagram Pin1: INT0 ⟶ INTP10	(a)
P.8	Chang to the explanation of the connection destination of the VGT capacitor according to the model name.	(c)
Chapter2 Pre-Driver		
P17	Fix the register map table.	(a)
P.30	Typo the setting when SHUNT_SEL = 101b.	(c)
P.38	Typo the description of VREG6P5 in Table 2-29.	(a)
P.44	Typo item number: 2.5.1.3 → 2.5.1.1	(a)
P.63	Delete unnecessary description.	(a)
Chapter3 RL78/G1F		
P.66	Typo in Table 3-3 and Table 3-4.	(a)
P.73	Modify Table 3-10 to match the Japanese manual.	(c)
P.75	Change the description of DAC, Comparator, PGA from unusable to untested nodame operation guarantee.	(c)
P.77	Correct 4.2.1 to correct description.	(a)
Chapter5 CHAPTER 5 Attention to use		
P.79	Typo 85degC version RAJ306010 : RAJ306010ZGFN→ RAJ306010GFN	(a)

Remark "Classification" in the above table classifies revisions as follows.
(a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note, (d): Addition/change of package, part number, or management division, (e): Addition/change of related documents

A. 2 Major Revisions in REV.2.00 from REV1.06

Page	Description	Classification
How to Use This Manual		
P.d	"RAJ306001" and "RAJ306010" are added to the target products. "RAJ306000" notation changed to "RAJ306000 series" notation.	(d)
Chapter1 Outline		
P.1,2,6, 7,8,10	"RAJ306000" notation changed to "RAJ306000 series" notation.	(b)
P.1	"RAJ306001" and "RAJ306010" operating voltage specifications added.	(b)
P.2	Changed terminal diagram to QFN package.	(d)
P.4	Table 1-2 WH terminal: Added BEMF amplifier signal output function for RAJ306010	(b)
P.8	Figure 1-4 Addition of specifications for connection destination of smoothing capacitor C2	(b)
P.9	Deleted description of back electromotive force measurement	(b)
P.9	Figure 1-5 Change the expression of SINK phase to the description of conductiong phase	(c)
Chapter2 Pre-Driver		
P.11, P.12	Figure 2-1,2 The following RAJ306010 terminal connection specifications have been added. Pre-driver ISENADIN2 pin and RL78/G1F P147 pin connection	(b)
P.12	Changes in specifications for UH, VH, and WH pin processing during sensorless control and changes in Figure 2-2	(b)
P.13	Table 2-1 Added BEMF amplifier signal output function from WH terminal function for RAJ306010	(b)
P.14	Table 2-2 Added current sense amplifier signal output from ISENADIN2 pin for RAJ306010	(b)
P.15	Table 2-3 Added ISENADIN2 terminal specifications	(b)
P.17	Table 2-4 Added read value for each product of WHO_AM_I register.	(b)
P.18 to 62	Changes in figures and table numbers	(a)
P.23	Added that the specifications differ for each product in the BEMF_MODE_SEL bit description.	(b)
P.23	Removed back electromotive force measurement from HALL_MODE_SEL bit description	(b)
P.24	Table 2-12 Added BEMF_MODE_SEL bit specifications for each product.	(b)
P.25	Table 2-13 Added the specifications of ALARM detection and and release threshold of VGT_OVP2_N bit for RAJ306010.	(b)
P.26	Table 2-14 Added the following description to the OCP_OPE_N bit description as a restriction when the protection processing execution is prohibited. "Set the OCP_WAIT bit of the ERROR_WAIT register to a value other than "00".	(c)
P.27	Table 2-15 Added the specifications of ALARM detection and and release threshold of VGT_OVP2_ ALE_N bit in RAJ306010.	(b)

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Page	Description	Classification
Chapter2 Pre-Driver		
P.40	Table 2-33 Added the specifications of ALARM detection and and release threshold of VGT_OVP2_ RAW_N bit for RAJ306010.	(b)
P.41	Table 2-35 Added read value for each product of WHO_AM_I register	(b)
P.46	2.5.3 Removed back electromotive from the explanation of Hall IC comparator.	(b)
P.51	Figure 2-19 Added current sense amplifier output (ISENADIN2 pin) as a dedicated specification for RAJ306010	(b)
P.53	Added the specifications of ALARM detection and and release threshold of VGT_OVP2_N bit for RAJ306010.	(b)
P.55	Figure 2-26 Change the waveform of 120 degree energization waveform to 60 degree PWM in the first half	(c)
P.58	RAJ306010 voltage monitor (VMC) section specifications added	(b)
P.61	Added the setting method of BEMF amplifier signal output for each product. Added notes on BEMF amplifier output measurement for RAJ306010. Figure 2-69 Revised the flowchart. Removed back electromotive force measurement by HALL-IC	(b)
Chapter3 RL78/G1F		
P.64,65, 67 to 71	“RAJ306000” notation changed to “RAJ306000 series” notation.	(b)
P.67	Figure 3-1 Added description of ISENADIN2	(b)
P.68,69	Table 3-5,6 Changed specifications of P147 due to addition of RAJ306010	(b)
P70	Table 3-3,4 Changed the description of PIOR20, PIOR21, PIOR31, PIOR32	(c)
P72,73	Table 3 9,10 ●Changed specifications of P147 due to addition of RAJ306010. ●Changed the processing of P55 and P146 according to Table 2-3	(b)
P77,78	Modified the format.	(c)
Chapter 5 Package Drawings		
P.79	RAJ306001, RAJ306010 usage conditions added	(b)

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A. 3 Revision History of Preceding Editions

Here is the revision history of the preceding editions. Chapter indicates the chapter of each edition.

(1/1)

Revision	Section	Page	Description	Classification
	How to	P.d	Recommendations for detailed usage of RL78 / G1F microcomputer are updated.	(c)
	Ch.1	P.1	Typo Chip temperature → Chip temperature (Pre-Driver)	(c)
		P.2	Typo Figure1-1 ●TRJO0 is deleted from Pin2 function. ●TRJIO0 is deleted from Pin7 function. ●At Pin61, AVREPP→AVREFP	(a)
		P.2	Following pin name is removed ●P02:IVCMP10, P03:IVCMP11, P20:IVCMP12, P21:IVCMP13,P22:ANO0/PGAI/IVCMP0, P23: ANO1/PGAGND, P31:VCOUT1	(b)
		P.3	Table 1-1 ●TRJO0 is deleted from Pin2 ●CSI00 is deleted from Pin17	(a)
		P.5	Table 1-3 ●Add INTP11 at Pin61	(a)
		P.6, P.8	Recommend capacitor value is removed. The values are written on data sheet. Refer to it.	(c)
		P.6	1.3.1 Power Supply Modify Note1	(c)
		P.8	Figure 1-4, modify C2 connection Table 1-4, Add enable/disable double boost	(b)
		P.8	Figure 1-5 Update (adding CW condition)	(b)
		P10	In 1.5 How to select the external MOSFET Add the description not to insert the resistance on gate line of External MOSFET.	(c)
	Ch.2	All	Refine of “2.4 Pre-Driver register” and “2.5 Pre-Driver Function (Setting / Usage) Same explanation on 2.4 and 2.5 is combined to 2.4 to be able to understand easily.	(c)
		All	External pin of Per-Driver diagram is deleted. It is written on data sheet. Refer to it.	(c)
		All	Typo bit name ●PS_CP_REG→PS_CPREG_N ●PS_CP→PS_CP_N ●OCPWAIT→OCP_WAIT	(a)
		P.11	Typo Figure 2-1 Typo, LD connection is changed P147 to P146	(a)
		P.12	Figure 2-2 Typo, LD connection is changed P147 to P146 Add hall inputs terminal at no-use.	(a)

Revision	Section	Page	Description	Classification
		P.15	Figrure 2-3 ●Typo, LD connection is change from P147 to P146 ●Add recommend MCU sequence when no-clock supply.	(a)
		P.17	Table 2-4 Revise and modify as follows ●delete typo ●WHO_AM_I bit name ●BGR_TRIM, and BFAMP_TRIM initial value	(a)
		P.18	Figure 2-5 Modify VGT Capacitor is connected form GND to VM	(b)
		P.23	2.4.6 ●Modify bit description of HALL_MODE_SEL, HALL_POLA, and HALL_SEL	(a)
		P.24	Figure 2-13 ●Add HALL_POLA bit and HALL_SEL	(a)
		P.25	Figure 2-14 ●Typo R/W→R	(a)
		P.28	Figure 2-18 ●Typo R/W→R	(a)
		P.28	Typo bit name CS_SET→CS_SET1	(a)
		P.30	Figure 2-22 ●Revise CS_SET2 value is changed 100→101	(a)
		P.31	Figure 2-24 Judge criteria for motor locked	(c)
		P.31	Figure 2-25 ●Typo R/W→R	(a)
		P.33	Figure 2-27 ●Typo bitn name DT_REG →DT_REG_N	(a)
		P.33	2.4.1.8 Add explanation for DRIVE_SET	(c)
		P.34	2.4.1.9 Add explanation for IDRCNT_H/IDRCNT_L	(c)
		P.38	Typo bit name PS_CPREG_N[1] → PS_CPREG_N	(a)
		P.40	Figure 2-39 ●Typo R/W→R	(a)
		P.41	Figure 2-40 ●Typo R/W→R Figure 2-41 ●Typo R/W→R	(a)
		P.42	Figure 2-44 ●Typo value for reset: FFh→00H Figure 2-45 ●Typo value for reset: FFh→00H	(a)
		P.43	Figure 2-46 ●Typo bit name DT_AUTO_N→DT_REG_N	(a)
		P.43	2.5.1 Add not for Pre-Driver	(c)
		P.44	Figure 2-42 Typo Protect release code 0010101→10010101	(a)

Revision	Section	Page	Description	Classification
		P.45	2.5.2, modify 5V regulator explanation	(c)
		P.46	2.5.4 Add explanation for Hall IC comparator	(c)
		P.46	Figure 2 49 ●Typo bit name HALL_SIG → PS_HALL_N	(a)
		P.47	Figure 2-50 Add waveform example.	(c)
		P.49	Figure 2-51 ●Typo bit PS_CPREG_N→PS_CSAMP_N	(a)
		P.50	2.5.5.2 Add note for CSAMP_TRIM5, and CSAMP_TRIM4 bit	(c)
		P.51	Figure 2-54 ●Add Vref voltage	(b)
		P.52	Figure 2-56 Typo	(a)
		P.52	Figure 2-57 Revise flowchart.	(a)
		P.53	Figure 2-58 ●Typo bit name DECAY_MODE→DECAY_MODE_SEL	(a)
		P.54	Figure 2-59, and Figure 2-60 Typo	(a)
		P.58	Figure 2-65 Add value at VM=6V and 30V	(c)
		P.59	Figure 2-66 ●Typo bit name PS_VMC→PS_VMC_N	(a)
		P.61	Figure 2-69 ●Typo bit name HALL_SIG→PS_BEMF_N ●Add note for DIR_SEL	(a)
		P.63	Modify Example code	(a)
	Ch.3	P.64	Add restrictions item ●WATCHDOG TIMER ●D/A CONVERTER	(b)
		P.65	Table 3-1 ●Typo PIOR02 value ●Delete PIOR04 bit (No-use) ●Delete note of PIOR02 bit Table 3-2 ●Add TRJO0 can not be used.	(a)
		P.66	Table 3-3 ●Typo, revise setting values from PIOR26 to PIOR 22 Table 3-4 ●Typo, revise VCOUT1 assign	(a)
		P.67	Figure 3-1 ●Modify connetction from LD P147 -> P146.	(a)
		P.68	Table 3-5 ●Typo P147 status is changed internal to No-use.	(a)
		P.69	Table 3-6 ●Typo note of SCLA0	(a)
		P.71	Talbe 3-8 ●Typo Note from P14 to P10	(a)

Revision	Section	Page	Description	Classification
			●Typo P31 status is changed internal to external.	
		P.72, P.73	Table 3-9 Modify recommend	(a)
		P.74	3.3.5 Modify description of timer RD	(b)
		P.75	3.3.6 Modify description of timer RG	(a)
		P.75	3.3.10 Add description of Watchdog Timer	(c)
		P.75	Add constraints of no-guarantee for D/A CONVERTER, COMPARATOR (CMP), PROGRAMMABLE GAIN AMPLIFIER (PGA)	(b)
		P.76	3.3.11 A/D Converter Following is added. low-voltage mode also can not be used.	(b)
	Ch.5	P.79	Add temperature profile on RAJ306000ZGFT	(b)
		Delete	Package dimension is removed.	(c)

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