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Renesas Electronics Corporation

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CUSTOMER NOTIFICATION

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QB-78K0RKX3
(Control Code: E, F, G, H, J, K, L, M)

Operating Precautions

Be sure to read this document before using the product.

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Operating Precautions for QB-78K0RKX3

This document describes the following items. Refer to the user's manual for cautions on using an in-circuit emulator.

- Restrictions not applicable to the target device but applicable to an in-circuit emulator
- Restrictions applicable to both the target device and an in-circuit emulator but the correction is planned only for the in-circuit emulator

Also refer to the following documents for the restrictions in the target device.

- User's manual of target device
- Restrictions notification document for target device

1. Product Version

The product versions of NEC Electronics in-circuit emulators are indicated by a control code. The control code is the second digit from the left in the 10-digit serial number. If the product has been upgraded, the control code can be checked by selecting [About] from the [Help] menu while the ID78K0R-QB is running. "X" in version information "IECUBE **** X F/W: V* **" is the control code.

Figure 1. Checking Control Code (Label on QB-78K0RKX3)

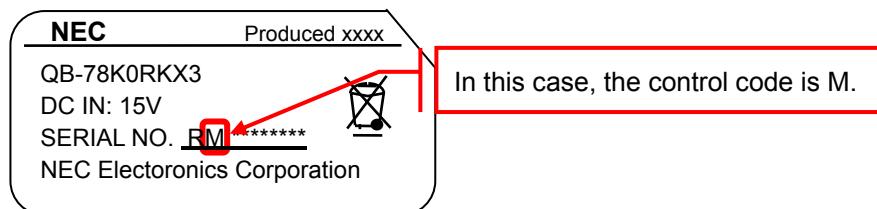
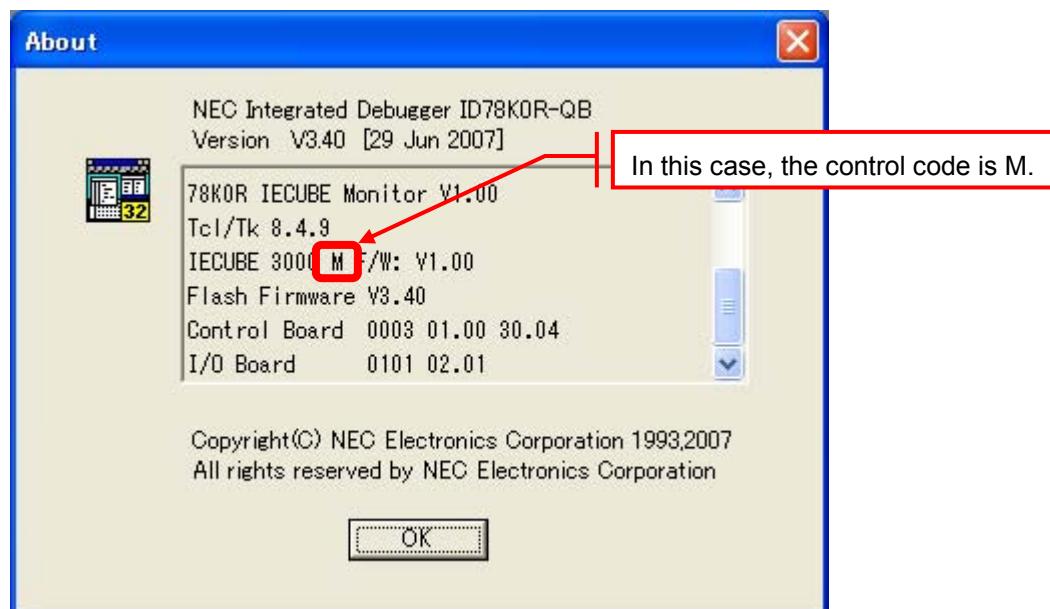


Figure 2. Checking Control Code (ID78K0R-QB)



2. Supported Devices

(1) Emulation environment for -A devices^{Note}

Use a QB-78K0RKX3 with control code L or later when performing emulation of an -A device.

Emulation of -A devices is not available when a QB-78K0RKX3 with control code K or earlier is used. (Use the QB-78K0RKX3 with the latest control code.)

(2) Emulation environment for non-A devices^{Note}

Emulation of non-A devices is available only when a QB-78K0RKX3 with control code K is used.

(If not, the QB-78K0RKX3 must be upgraded to control code K.)

Contact an NEC Electronics sales representative or a distributor from whom you purchased this product for how to update the control code.

Note Identification of -A devices and non-A devices

"A" in the part number indicates whether the product has been revised and this classifies devices as -A or non-A.

The parts of part number “μPD78F1166AGF-GAS-AX” are explained below, as an example.

Family type	Part number	Revised	Package type custom code/speed class, pin type, etc.		Lead-free
μPD	78F1166	A	GF	- GAS	-AX

3. Product History

No.	Restrictions and Added/Changed Specifications	Control Code							
		E	F	G	H	J	K	L	M
1	Restriction whereby trace information or pass count becomes invalid after execution of manipulation instruction for the operation speed mode control register (OSMC)	x	o	o	o	o	o	o	o
2	Restriction on reset control flag register (RESF)	o	x	x	o	o	o	o	o
3	Restriction whereby invalid display of the BCDCY bit during a break	x	x	x	o	o	o	o	o
4	Restriction on break before execution	x	x	x	o	o	o	o	o
5	Restriction whereby stack overflow or stack underflow illegally occurs	x	x	x	o	o	o	o	o
6	Restriction whereby invalid data may be fetched or read from external memory	x	x	x	o	o	o	o	o
7	Restriction whereby word misalign access illegally occurs	x	x	x	o	o	o	o	o
8	Restriction on downloading programs	x	x	x	x	o	o	o	o
9	Restrictions on coverage function	x	x	x	x	o	o	o	o
10	Restriction related to block erase function during self-programming	x	x	x	x	x	o	o	o
11	Restriction whereby invalid operations occur if there is a ROM instruction several instructions before an instruction for which a "break before execution" is set	x	x	x	x	x	o	o	o
12	Restriction whereby a fail-safe break for uninitialized RAM occurs when an interrupt is generated during flash self-programming	x	x	x	x	x	o	o	o
13	Support for interrupt servicing during self-programming	x	x	o	o	o	o	o	o
14	Support of 78K0R/Kx3 (μ PD78F11xxA)	x	x	x	x	x	x	o	o
15	Restriction on trace data when an interrupt occurs	x	x	x	x	x	x	x	o
16	Restriction on program execution on RAM	x	x	x	x	x	x	x	o

-: Not relevant, x: Applicable, o: Corrected

4. Details on Bugs and Specification Changes

No. 1 Restriction whereby trace information or pass count becomes invalid after execution of a manipulation instruction for the operation speed mode control register (OSMC)

[Description]

After bit 0 (FSEL) of the operation speed mode control register (OSMC) is set to 1 by using an instruction, the following illegal operations may occur.

- (1) Trace information near the instruction is displayed redundantly.
- (2) The pass count is not counted normally if an event (instruction or access) is set near the instruction.

[Workaround]

There is no workaround.

[Correction]

This issue has been corrected in products with control code F and later.

No. 2 Restriction on reset control flag register (RESF)

[Description]

Even if data in the reset control flag register (RESF) is read by using a memory manipulation instruction, the RESF register is not reset to 00H. The RESF register can normally be reset to 00H by using a _RESET input or the power-on-clear (POC) circuit.

[Workaround]

There is no workaround.

[Correction]

This issue has been corrected in products with control code H and later.

No. 3 Restriction whereby invalid display of the BCDCY bit during a break

[Description]

If a break occurs after the BCDCY bit (bit 0 of the BCD correction carry register) is cleared to 0 as a result of an addition or subtraction instruction, the BCDCY bit may show “1”. This bug only affects the display, not the program.

[Workaround]

There is no workaround.

[Correction]

This issue has been corrected in products with control code H and later.

No. 4 Restriction on break before execution

[Description]

If a break before execution is set to an area that has been overwritten by flash self-programming, the subsequent program execution may become invalid.

[Workaround]

There is no workaround.

[Correction]

This issue has been corrected in products with control code H and later.

No. 5 Restriction whereby stack overflow or stack underflow illegally occurs

[Description]

If execution of a stack manipulation instruction (such as the RET instruction) conflicts with DMA transfer, the stack detection function operates illegally; consequently, a fail-safe break for stack overflow or stack underflow may occur.

[Workaround]

Implement the following setting so as to disable detection of stack overflows and stack underflows.

- Open the Configuration dialog box and click the [Detail] button to open the Fail-Safe Break dialog box.
Clear the Stack Underflow and Stack Overflow check boxes.

[Correction]

This issue has been corrected in products with control code H and later.

No. 6 Restriction whereby invalid data may be fetched or read from external memory

[Description]

If an external memory address whose lower 16 bits match “00D0H” or “00D2H” is accessed, invalid data may be fetched or read from external memory.

[Workaround]

There is no workaround.

[Correction]

This issue has been corrected in products with control code H and later.

No. 7 Restriction whereby word misalign access illegally occurs

[Description]

If processing of 16-bit DMA transferring conflicts with accessing of an odd address in a data memory space by an instruction, a word misalign access is illegally detected; consequently, a fail-safe break occurs.

[Workaround]

Implement the following setting so as to disable detection of word misalign accesses.

- Open the Configuration dialog box, click the [Detail] button to open the Fail-Safe Break dialog box, and then clear the “Word Miss-align Access” check box.

[Correction]

This issue has been corrected in products with control code H and later.

No. 8 Restriction on downloading programs

[Description]

When downloading a program using the ID78K0R-QB, the error message “F0200: Verification error occurred. Failed in writing memory. (0xxxxxx)” may be output. In such a case, downloading of the program was not completed normally, nor was the program written to the memory of the QB-78K0RKX3 normally.

[Workaround]

Retry downloading the program until the error no longer occurs.

[Correction]

This issue has been corrected in products with control code J and later.

No. 9 Restrictions on coverage function

[Description]

The following restrictions (a) to (c) concerning the coverage function exist.

- (a) The coverage measurement function (C0 coverage) measures not only ROM fetch but also ROM read.
- (b) When the read access status is displayed by the access monitor function on the Memory window, the window displays not only the ROM read status but also the ROM fetch status.
- (c) The general-purpose register value displayed in the Memory window may become invalid after accessing of a RAM area to which the general-purpose register is assigned. In addition, the Register window display may be invalid during program execution.

[Workaround]

- (a) There is no workaround. This issue has been corrected in products with control code J and later so as to measure ROM fetch only.
- (b) There is no workaround. This issue has been corrected in products with control code J and later so as to display ROM read only.
- (c) There is no workaround. This issue has been corrected in products with control code J and later.

The modification for the above items affects integrated debugger ID78K0R-QB and IECUBE self-diagnostic tool IEQBUTL, so be sure use them in the following combination.

Control Code	Integrated Debugger ID78K0R-QB	IECUBE Self-Diagnostic Tool IEQBUTL
E, F, G, H	V3.20	V2.11
J and later	V3.30 and later	V2.13 and later

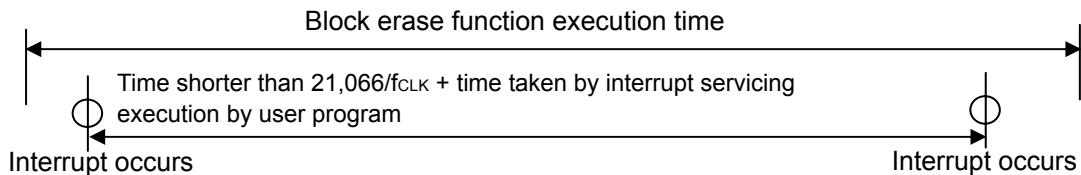
[Correction]

This issue has been corrected in products with control code J and later.

No. 10 Restriction related to block erase function during self-programming

[Description]

An erase error may occur if an interrupt occurs multiple times in an interval shorter than “ $21,066/f_{CLK} + \text{time taken by interrupt servicing execution by user program}$ ” when the block erase function (`_FlashBlockErase`) is being executed during self-programming. The “time taken by interrupt servicing execution by user program” is the time from when execution branches to a vector reference address, interrupt servicing execution by user program, and until when execution returns to the block erase function (see figure below).



[Workaround]

There is no workaround.

[Correction]

This issue has been corrected in products with control code K and later.

No. 11 Restriction whereby invalid operations occur if there is a ROM instruction several instructions before an instruction for which a “break before execution” is set

[Description]

If there is an instruction to read the ROM area several instructions before an instruction for which a “break before execution” is set (up to nine instructions in case of an 8-bit instruction), the break may not occur, or the program may not operate correctly.

If the instruction subject to the break does not extend over a 4-byte boundary^{Note}, the instruction is not replaced and the break does not occur.

If the instruction subject to the break extends over a 4-byte boundary^{Note}, only the code immediately before the boundary is replaced. As a result, the instruction becomes invalid and may loop.

Note The 4-byte boundaries are portions shown as red dotted lines in the following figure.

[Workaround]

There is no workaround.

[Correction]

This issue has been corrected in products with control code K and later.

No. 12 Restriction whereby a fail-safe break for uninitialized RAM occurs when an interrupt is generated during flash self-programming

[Description]

When an interrupt is generated by the program during flash self-programming, a fail-safe break for uninitialized RAM (Uninitialize Memory Read) may occur.

[Workaround]

Implement the following setting so as to disable detection of Read From Uninitialized RAM.

- Open the Configuration dialog box, click the [Detail] button to open the Fail-Safe Break dialog box, and then clear the “Read From Uninitialize RAM” check box.

[Correction]

This issue has been corrected in products with control code K and later.

No. 13 Support for interrupt servicing during self-programming

[Description]

Interrupt servicing during self-programming is now supported.

[Correction]

This function is supported in products with control code G and later. The QB-78K0RKX3 with control code F and earlier versions include firmware installed in 78K0R/Kx3 Ver. 2.1, so the device restriction “interrupts during self-programming not supported” is still applicable.

No. 14 Support of 78K0R/Kx3 (μ PD78F11xxA)

[Description]

The 78K0R/Kx3 (μ PD78F11xxA) is now supported.

[Correction]

This change has been implemented in products with control code L and later.

The QB-78K0RKX3 control code L or later versions do not support the 78K0R/Kx3 (μ PD78F11xx).

Consult an NEC Electronics sales representative or distributor if downgrading is necessary.

A common device file is provided for all 78K0R/Kx3 products (μ PD78F11xx and μ PD78F11xxA).

No. 15 Restriction on trace data when an interrupt occurs

[Description]

If a read access or write access is performed immediately before occurrence of an interrupt, this access may not be reflected to the trace result.

[Workaround]

There is no workaround.

[Correction]

This issue has been corrected in products with control code M and later.

An example of trace data before and after the correction of this restriction is shown below.

The diagram illustrates the trace data comparison between 'Before correction' and 'After correction' for the QB-78K0RKX3 operating precautions. It features two tables of trace data with annotations explaining the changes made by the correction.

[Before correction]

_ A 131064 0:00:00.516 208 000 01065	AA02	M1			
_ A 131065 0:00:00.516 209 000			F3FFE	9700	W
_ A 131066 0:00:00.516 209 500 0002E	4A01FF	VECT	F3FFC	1067	W
_ A 131067 0:00:00.516 211 500 0014A	84	M1			INC E
_ A 131068 0:00:00.516 212 000 0014B	4C0F	M1			CMP A,#0FH
_ A 131069 0:00:00.516 212 500 0014D	8A02	M1			MOV A,[DE+2H]
_ A 131070 0:00:00.516 213 000			F450D	83	R

A callout box points to the instruction at address 131065: "A read access by this MOV instruction is not reflected to the trace result." An oval highlights the instruction: **MOVW AX,[DE+2H]**.

[After correction]

_ A 131063 0:00:00.258 053 000 01065	AA02	M1			
<u>_ A 131064 0:00:00.258 053 500</u>			F450C	8312	R
_ A 131065 0:00:00.258 054 000			F3FFE	9700	W
_ A 131066 0:00:00.258 054 500 0002E	4A01FF	VECT	F3FFC	1067	W
_ A 131067 0:00:00.258 056 500 0014A	84	M1			INC E
_ A 131068 0:00:00.258 057 000 0014B	4C0F	M1			CMP A,#0FH
_ A 131069 0:00:00.258 057 500 0014D	8A02	M1			MOV A,[DE+2H]
_ A 131070 0:00:00.258 058 000			F450D	83	R

A large downward arrow points from the 'Before correction' table to the 'After correction' table. Callout boxes point to the instruction at address 131064 in both tables. The first callout in the 'Before correction' table states: "This line shows the result of the read access by 'MOVW AX, [DE+2H]'". The second callout in the 'After correction' table states: "A read access by this MOV instruction is reflected to the trace result." An oval highlights the instruction: **MOVW AX,[DE+2H]**.

No. 16 Restriction on program execution on RAM

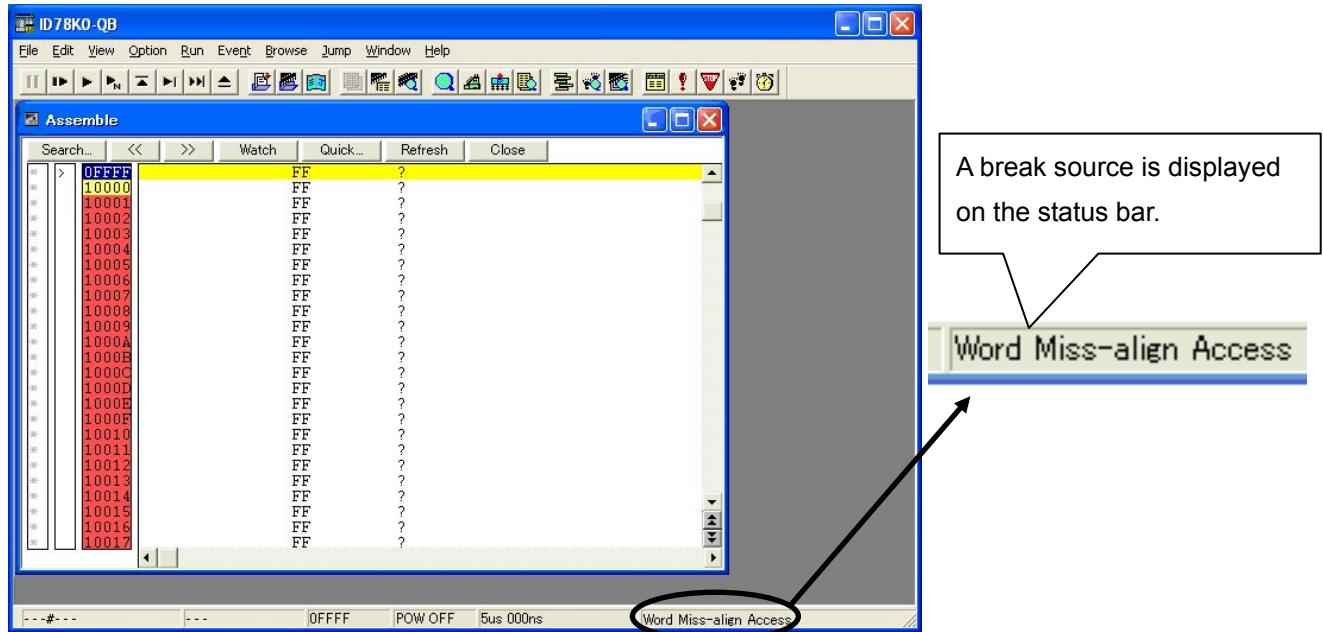
[Description]

When a branch instruction is executed on RAM and if the branch destination is an odd address located in RAM, a fail-safe break due to a word misalign access occurs.

[Workaround]

Clear the check box for the [Word Miss-align Access] in the Fail-Safe Break dialog box in the ID78K0R-QB.

A break source can be checked in the status bar in the ID78K0R-QB, as shown below.



[Correction]

This issue has been corrected in products with control code M and later.