Introduction

The evaluation board is designed to help the customer evaluate the 5P49V6901, the latest addition to the family of programmable devices in IDT's Timing portfolio. When the board is connected to a PC running IDT Timing Commander™Software through USB, the device can be configured and programmed to generate frequencies with best-in-class performances.

Board Overview

Use Figure 1 and Table 1 to identify: power supply jacks, USB connector, input and output frequency SMA connectors.

Figure 1. 5P49V6901 EVB Overview

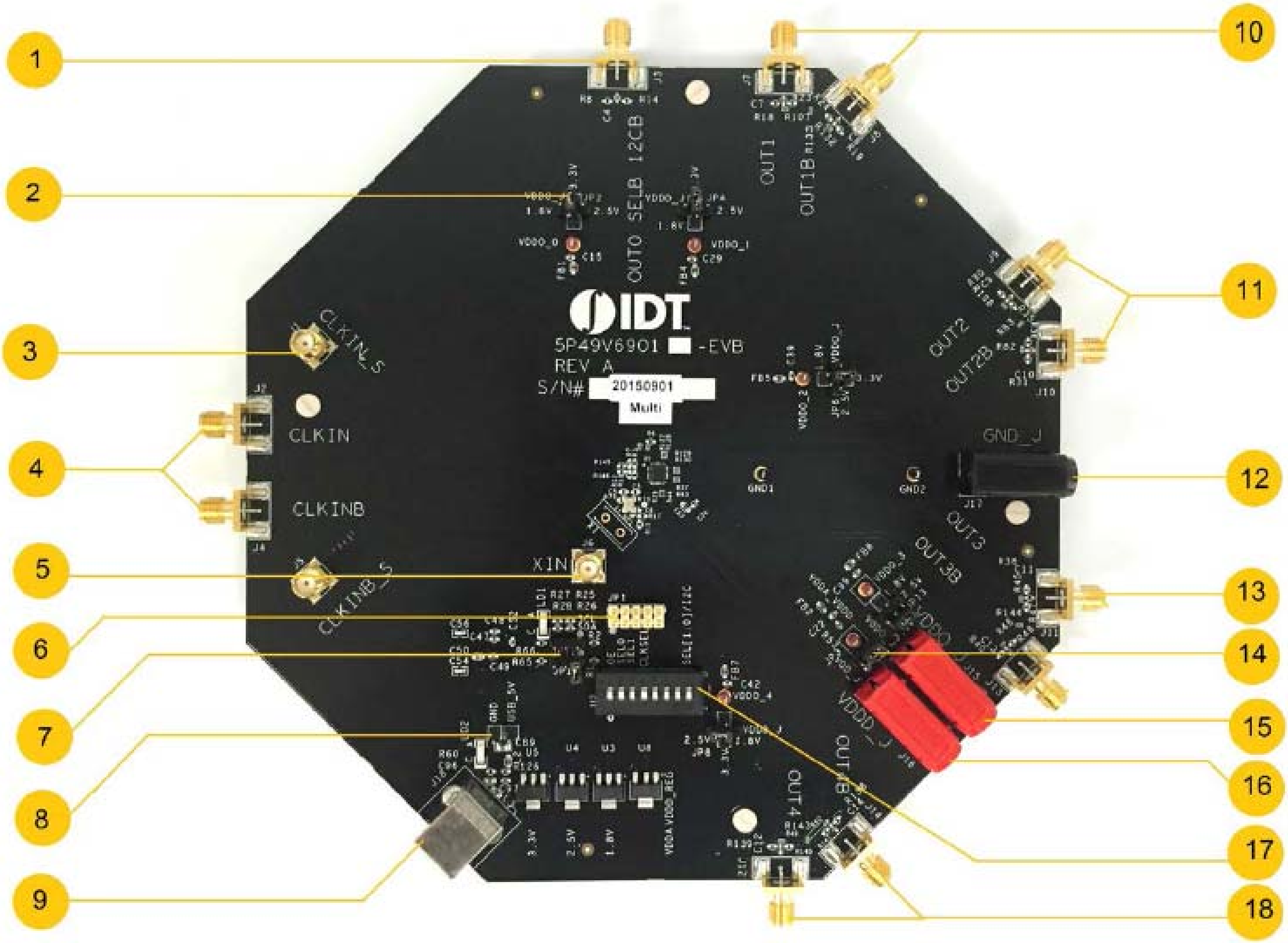


Table 1: 5P49V6901 EBV Pins and Functions

Item	Name	On-Board Connector Label	Function
1	Output 0	J3	Single ended buffered output of input reference clock
2	Output Voltage Power Supply Selector	JP2, JP4, JP6, JP13, JP8	4-way header to select a power supply method for outputs 0, 1, 2, 3 and 4. The center pin is the output voltage. Use the jumper to select 3.3V, 2.5V, 1.8V or VDDO_J supply. VDDO_J is the voltage from J16
3	CLKIN_S	J1	SMA Pair used to monitor differential input CLKIN with CLKINB_S
4	Clock Input	J2/J4	Used as primary differential clock input
5	Xin	J6	Used as primary single ended clock input. Maximum full swing limited to 1.2V
6	Aardvark Connector	JP1	For Aardvark connection
7	Interface Mode Selector	JP11/JP12	Used to select either I2C mode or Hardware select mode
8	Input Voltage Regulator	GND/USB_5V	Used to input 5V supply in hardware select mode
9	USB Interface	J18	Used for connection with a PC and for interaction with the IDT Timing Commander Software.
10	Output 1	J7/J8	Can be one differential output pair or two individual single ended outputs
11	Output 2	J10/J9	Can be one differential output pair or two individual single ended outputs
12	Ground Jack	J17	Used for grounding. If J15 and/or J16 is used for power supply, this jack functions as the power return.
13	Output 3	J13/11	Can be one differential output pair or two individual single ended outputs
14	Input Voltage Power Supply Selector	JP3	Provides selection of VDDA_VDDD supply from regulators or VDDD_J supply from J16
15	Output Voltage Jack	J15	Connect 3.3V, 2.5V or 1.8V for the output voltage of the device
16	Power Supply Jack	J16	Connect 3.3V power supply for the core voltage of the device
17	DIP Switch	U2	S1: Output Enable(OE/SD) S2: Sel0 S3: Sel1 S4: CLKSEL S8: Sel [1:0] ; Default: I2C mode
18	Output 4	J12/14	Can be one differential output pair or two individual single ended outputs

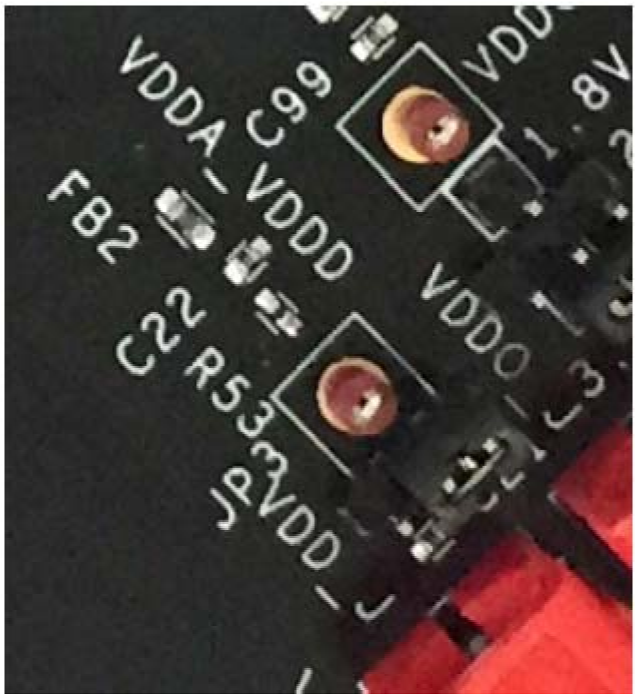
Board Power Supply

• Power Supply Options

Bench Power Supply – An external power supply can be used to supply a 3.3V, 2.5V or 1.8V supply. To supply VDDD_J with a bench power supply, connect power to J16. Concurrently, place the jumpers in JP3 to connect VDDA_1 to VDD_J.

USB Power Supply – When the board is connected to a PC through a USB cable, on-board voltage regulators will generate a 3.3V for the device. In this case, place the jumpers in JP3 to connect VDDA_1 to VDDA_VDDD. See JP3 jumper position for VDDA_1 in the Figure 2. USB power source is recommended for ease of use.

Figure 2. Connecting VDDA_VDDO_REG and VDD_REG using jumper will select power source from on-board regulators powered by USB; Connecting the VDD_J and VDD_REG using jumper will select external bench power supply



• Output Clock Voltages

Similar to VDDA_1 having two sources, each output voltage is also provided with two sources to choose from: Bench power supply or USB power supply connection. The selection is made by a 4-way header as shown in Figure 3 below. Selection of VDDO_J will enable external power supply (J15 and J16 are connected to external power supply); Selection of 3.3V, 2.5V or 1.8V will enable the on-board voltage regulators powered by USB port.

Figure 3. In the 4-way header, the central pin is the output and the other pins are 1.8V, 2.5V, 3.3V and VDDO_J (from J15) respectively. Jumper settings are selected according to the output voltage required for outputs 0, 1, 2 and 3.

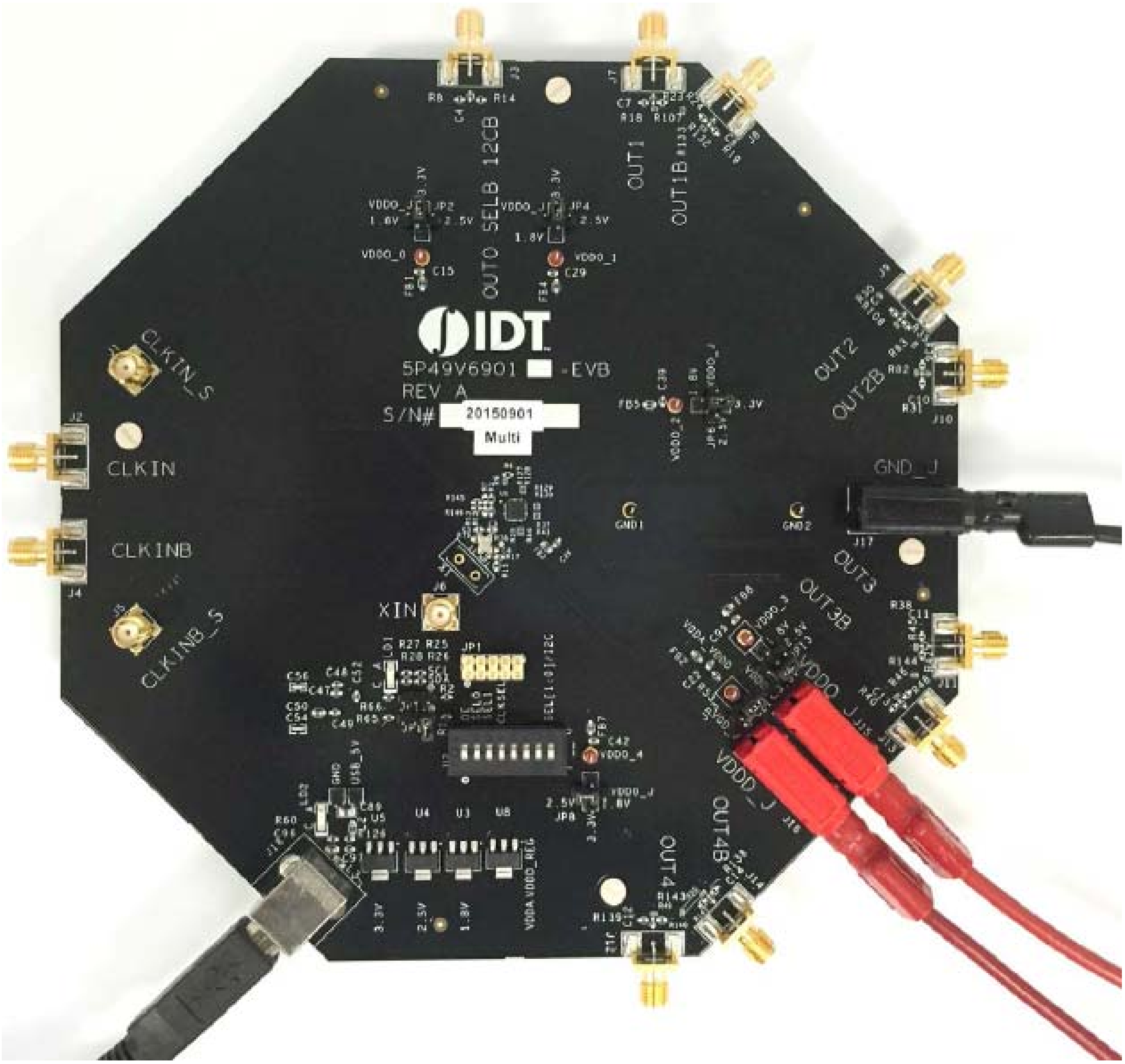
Connecting the Board

The board is connected to a PC through a USB connector for configuring and programming the device, as shown in Figure 4 below. The USB interface will also provide +5V power supply to the board, from which on-board voltage regulators generate +3.3V for the core and +3.3V, +2.5V or +1.8V voltages for the for different outputs.

The board can also be powered by a bench power supply by connecting two banana jacks J15, J16 for output and core voltages, respectively. Please see board power supply section for details.

Note: The USB port only supports USB 2.0; USB 3.0 is not supported at this time.

Figure 4. Connecting 5P49V6901 – EVB USB Port for Communications with Timing Commander Software and input voltage supplies



On-Board Crystal

A 25MHz crystal is installed on the board.

NOTE: For the 5P49V6901, the clock input is given through J2 and J4 SMA connections.

Board Default Frequency Output

When 25MHz crystal is installed, the device will have the following default outputs: OUT0 = 25MHz, OUT1=100MHz.

Configuration and Setup

Use the following steps to setup the board using I^2C and start the configuration of the board.

1. Set SEL pin (pin 8) of dip switch (U2) to "0" to select I2C mode.

2. Connect J18 to a USB port of the PC using the supplied cable.

3. Launch VC6 Timing Commander Software (refer to VersaClock 6 Timing Commander User Guide - Getting Started Step 1~7).
4. Following the Getting Started steps in the Timing Commander software, an I^2C connection is established between the GUI software and VC6 chip.
5. Select "Open Settings File" if you have existing settings or "New Settings File" and select 5P49V6901 evaluation board. In the same screen, browse for a personality file, by clicking on the button at the bottom right, to be used with the evaluation board.
6. Connect to the EVB by clicking on the microchip icon located at the top right of the Timing Commander.

7. Once connected, new options will be available on a green background indicating that the EVB has successfully connected with the board. Write the settings to the chip by clicking on the write all registers to the chip option.

8. All intended outputs should now be available for measurement.

Board Schematics

Evaluation board schematics are shown on the following pages.

Figure 5. 5P49V6901 VersaClock 6 Evaluation Board Schematics – Page 1

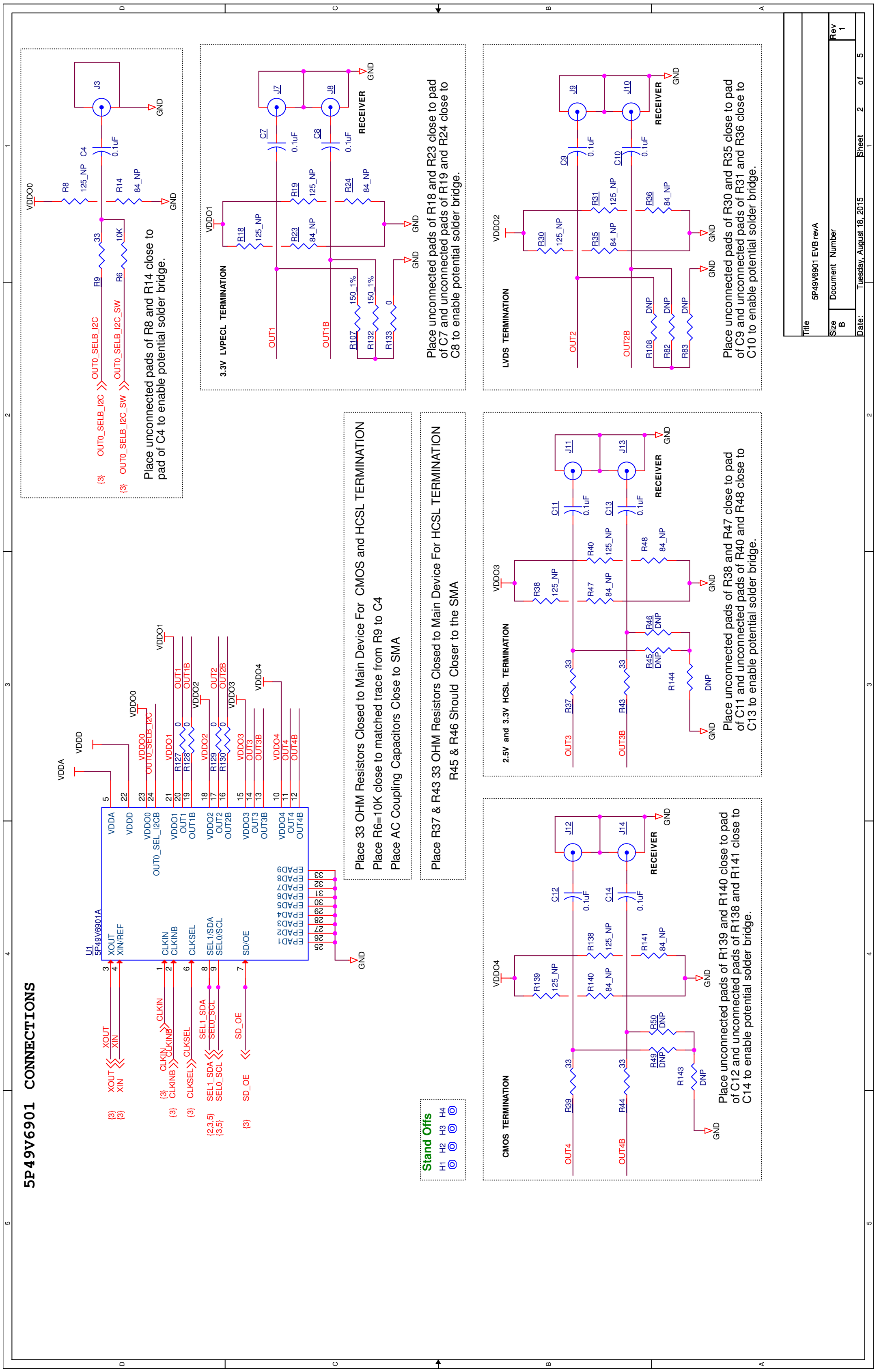


Figure 6. 5P49V6901 VersaClock 6 Evaluation Board Schematics – Page 2

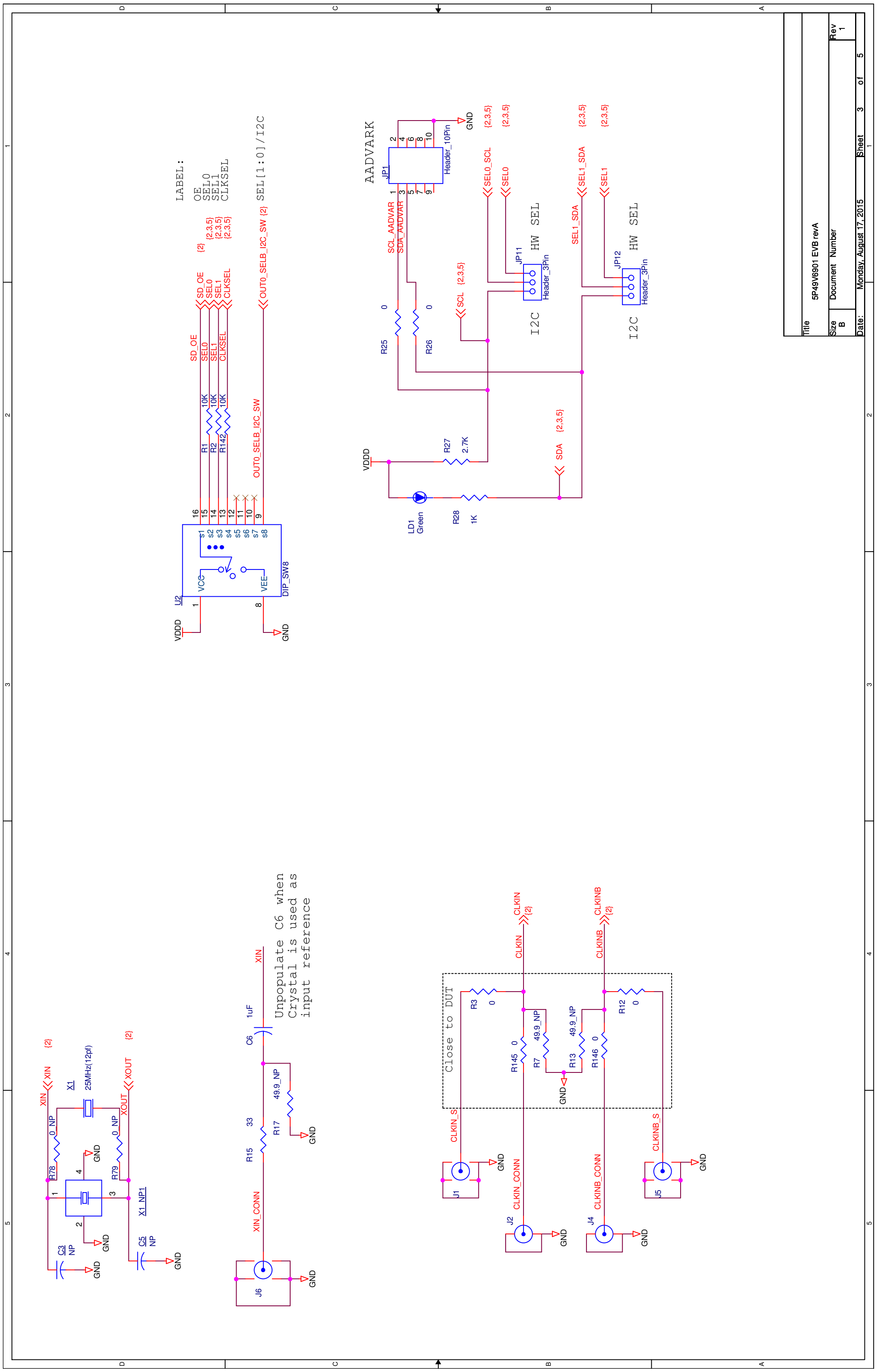


Figure 7. 5P49V6901 VersaClock 6 Evaluation Board Schematics – Page 3

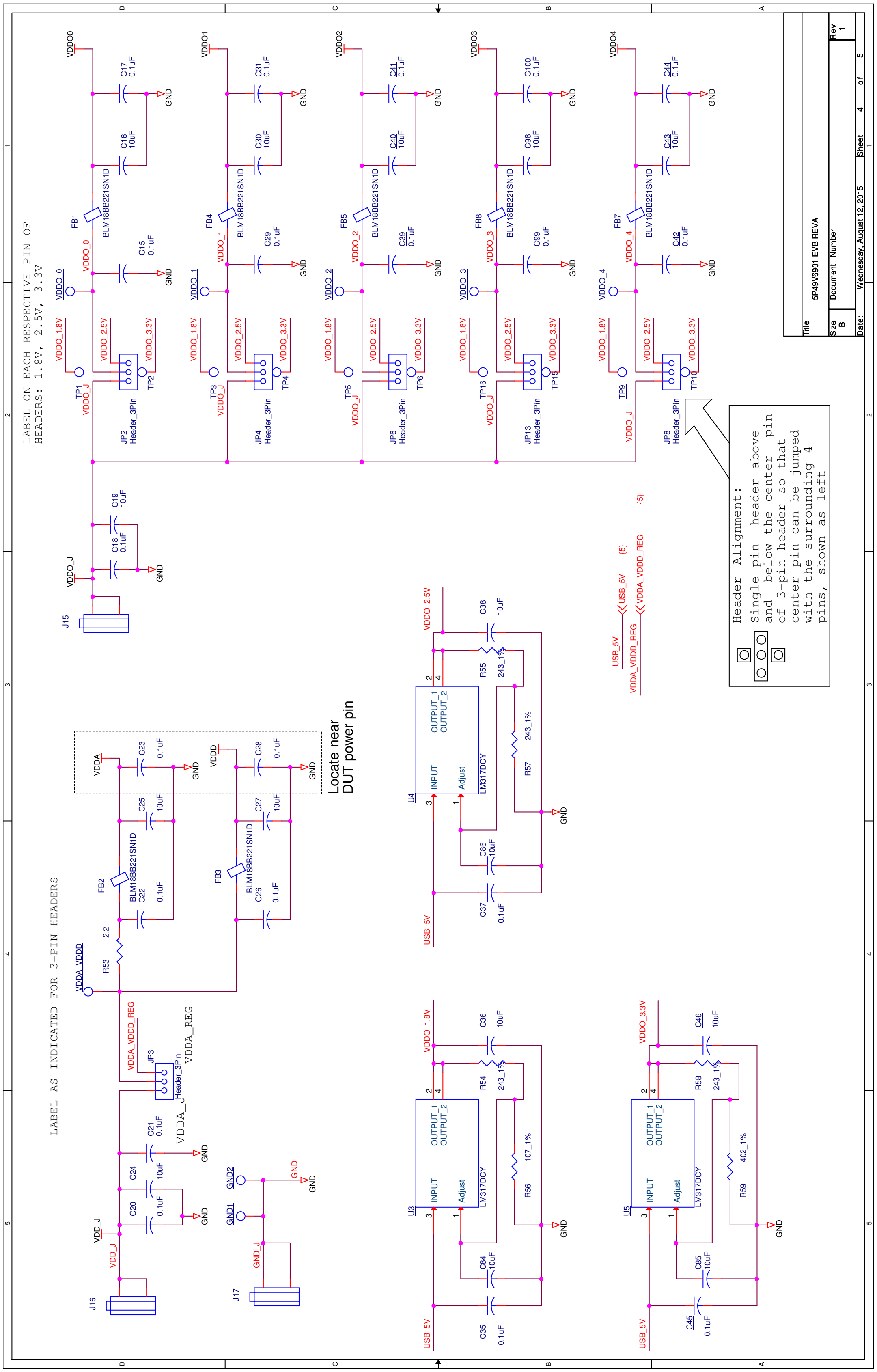
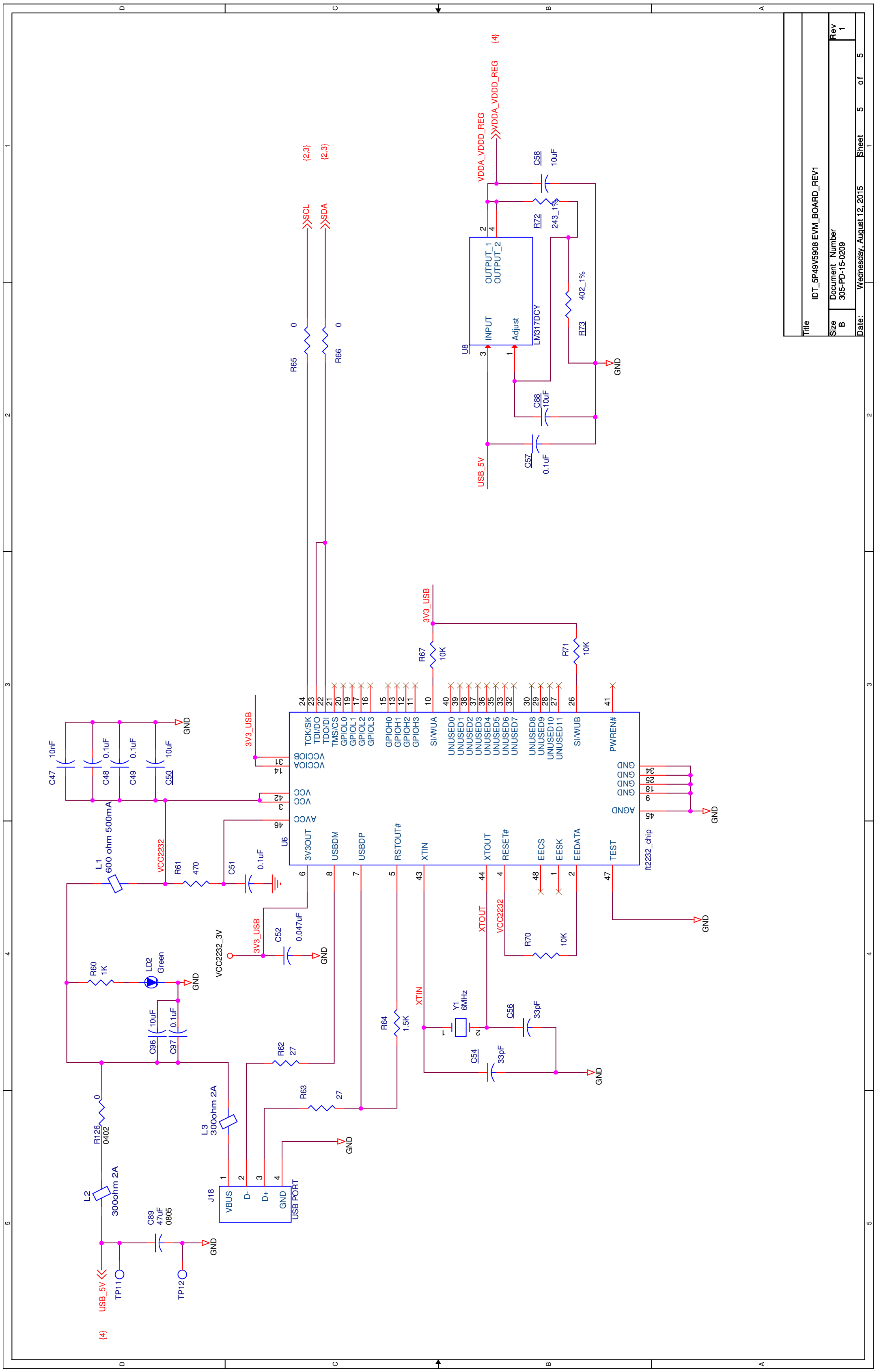


Figure 8. 5P49V6901 VersaClock 6 Evaluation Board Schematics – Page 4



Signal Termination Options

Termination options for OUTPUT 1 - 4 for the 5P49V6901 evaluation board are displayed in Figure 9. The termination circuits are designed to optionally terminate the output clocks in LVPECL, LVDS, LVCMOS and HCSL signal types by populating (or not-populating) some resistors. DC or AC coupling of these outputs are also supported.

Tables 2 – 5 tabulate component installations to support LVPECL, HCSL, LVCMOS and LVDS signal types for OUTPUT1 – 4on the 5P49V6901 evaluation board.Please note that by doing so, the output signals will be measured and terminated by an oscilloscope with a 50Ω internal termination.

Figure 9. Output Termination Options

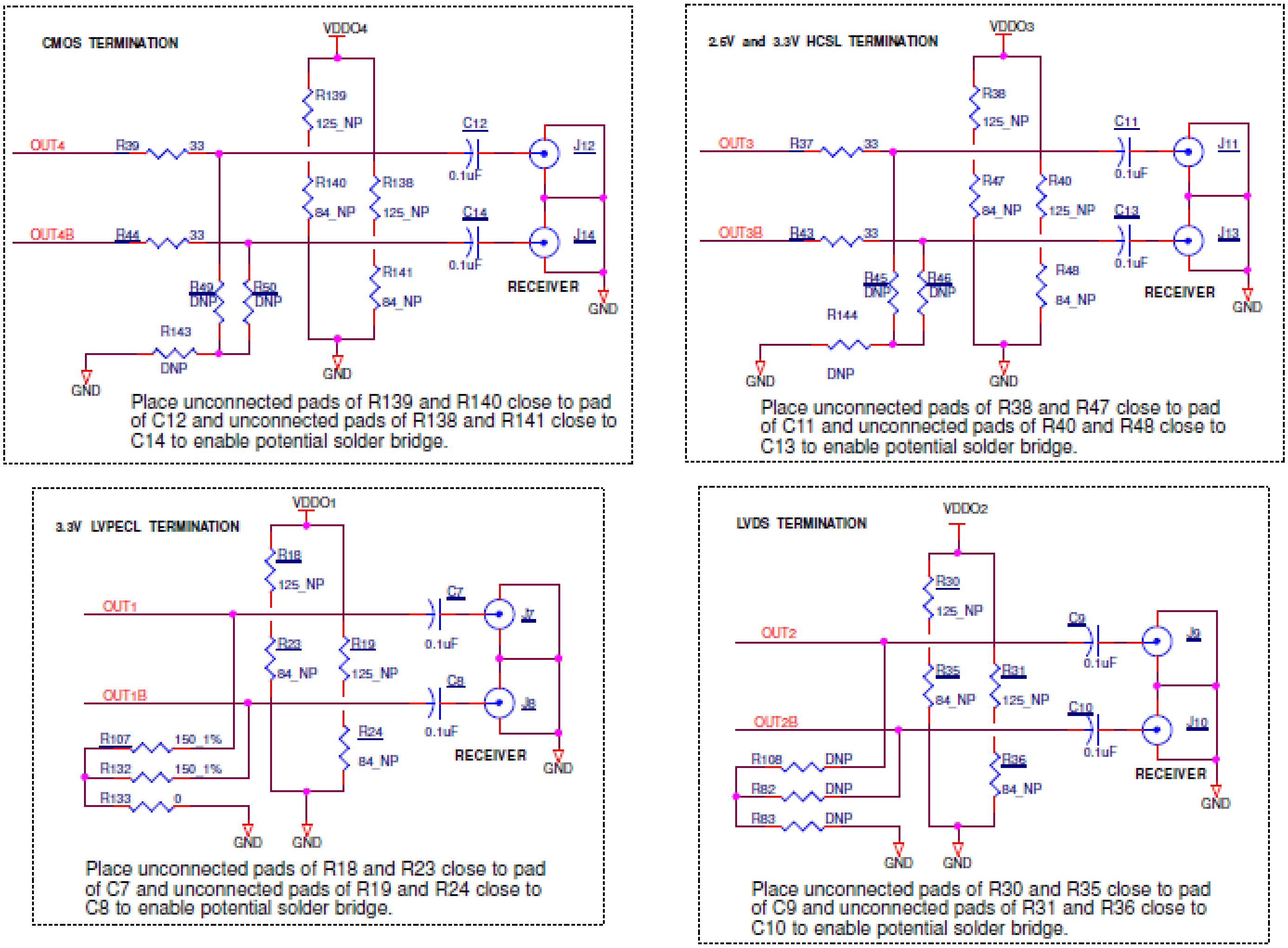


Table 2: Termination Options for OUTPUT1

Signal Type	Series Resistors: R127, R128	150-ohm pull-down: R107, R132	0-ohm pull-down series resistor: R133	Series Capacitor: C7, C8	Resistor Network: R18, R19, R23, R24
LVPECL	0 Ω	Installed	Installed	0.1 µF	Not installed

Table 3: Termination Options for OUTPUT2

Signal Type	Series Resistors: R129, R130	150-ohm pull-down: R108, R82	0-ohm pull-down series resistor: R83	Series Capacitor: C9, C10	Resistor Network: R30, R31, R35, R36
LVDS	0 Ω	Not installed	Not installed	0.1 µF	Not installed

Table 4: Termination Options for OUTPUT3

Signal Type	Series Resistors: R37, R43	150-ohm pull-down: R45, R46	0-ohm pull-down series resistor: R144	Series Capacitor: C11, C13	Resistor Network: R38, R40, R47, R48
HCSL	33 Ω	Not installed	Not installed	0 Ω	Not installed

Table 5: Termination Options for OUTPUT4

Signal Type	Series Resistors: R39, R44	150-ohm pull-down: R49, R50	0-ohm pull-down series resistor: R143	Series Capacitor: C12, C14	Resistor Network: R139, R138, R140, R141
LVCMOS	33 Ω	Not installed	Not installed	0.1 µF	Not installed

The 5P49V6901MULTI board has default terminations of LVPECL on OUT1, LVDS on OUT2, HCSL on OUT3 and LVCMOS on OUT4. The 5P49V6901LVPECL, 5P49V6901HCSL, 5P49V6901LVDS and 5P49V6901LVCMOS variants have respective terminations on all outputs. Use tables 2 – 5, to change the output terminations on the 5P49V6901 boards as per requirement.

As noted, 4-resistor network is not installed in Table 2 – 5 because oscilloscope with internal 50Ω termination is utilized for signal termination and measurement. If an AC-coupled, stand-alone LVPECL output is needed (without oscilloscope connections), the 4-resistor network needs to be installed accordingly (seeTable 6 below).

Table 6: Resistor Network Termination for LVPECL for OUTPUT1

Signal Type	Series Resistors: R127, R128	150-ohm pull-down: R107, R132	0-ohm pull-down series resistor: R133	Series Capacitor: C7, C8	Resistor Network: R18, R19, R23, R24
LVPECL	0 Ω	Installed	Installed	0.1 µF	R18 = R19 = 125Ω R23 = R24 = 84Ω

Orderable Part Numbers

The following evaluation board part numbers are available for order.

Table 7: Orderable Part Numbers

Part Number	Description
EVKVC6-6901ALL	5P49V6901 Evaluation board with one output of each type of signal termination
EVKVC6-6901LVDS	5P49V6901 Evaluation board with all outputs terminated as LVDS
EVKVC6-6901HCSL	5P49V6901 Evaluation board with all outputs terminated as HCSL
EVKVC66901LPECL	5P49V6901 Evaluation board with all outputs terminated as LVPECL
EVKVC66901LCMOS	5P49V6901 Evaluation board with all outputs terminated as LVCMOS

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