To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

RENESAS

MOS INTEGRATED CIRCUIT

μPD16708

300-OUTPUT TFT-LCD GATE DRIVER

DESCRIPTION

The μPD16708 is a TFT-LCD gate driver equipped with 300-output lines. It can output a high-gate scanning voltage in response to CMOS level input because it provided with a level-shift circuit inside the IC circuit.

FEATURES

- CMOS level input (2.3 to 3.6 V)
- 300 outputs + 2 pins (Fixed to V_{EE})
- High-withstanding-voltage output (V_{DD2} to V_{EE} = amplitude: 40 V MAX.)
- COG mounting possible

ORDERING INFORMATION

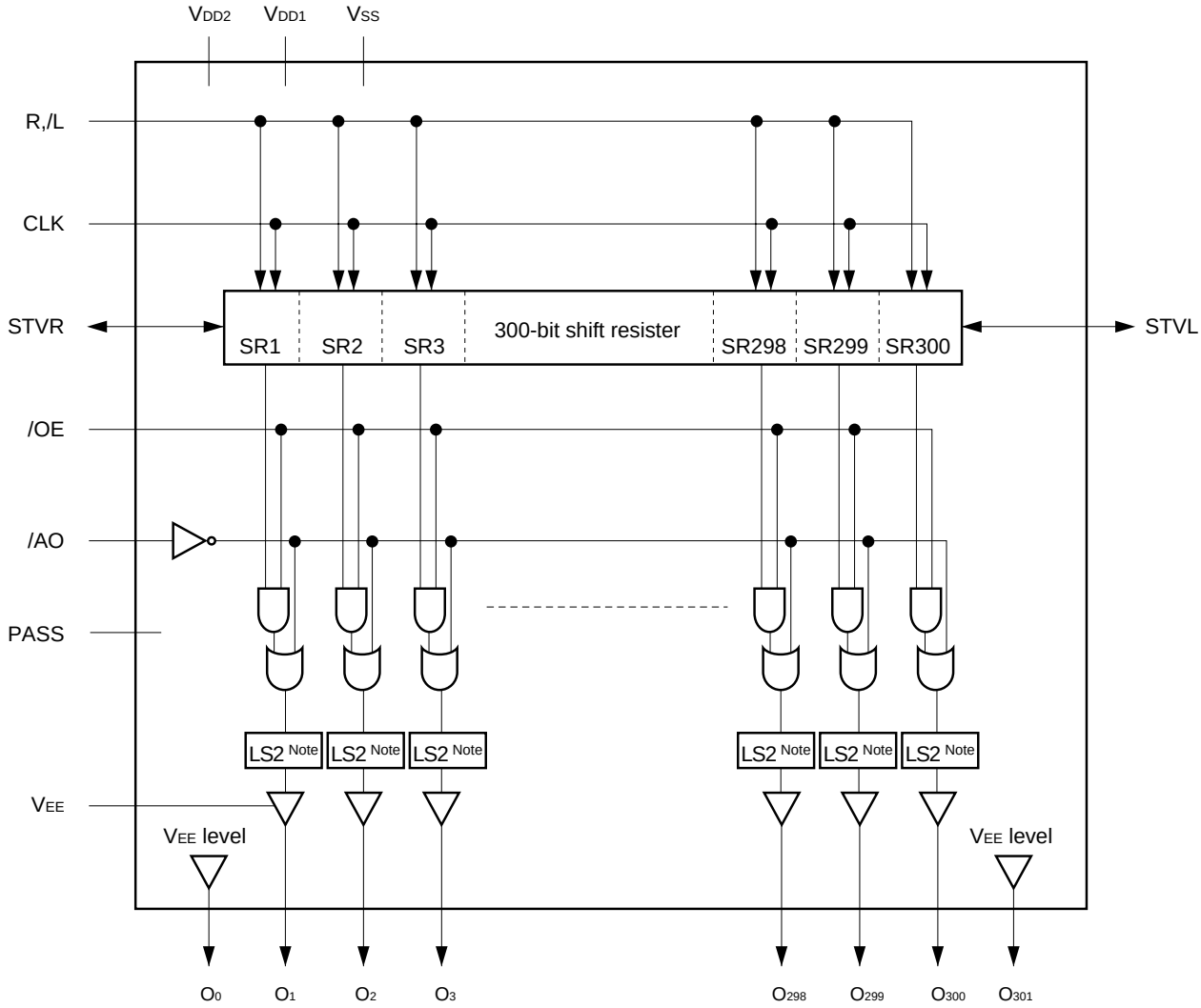
Part Number	Package
μPD16708P	Chip

Remark Purchasing the above chip entails the exchange of documents such as a separate memorandum or product quality, so please contact one of our sales representatives.

Document No. S16071EJ6V0PM00 (6th edition)
Date Published January 2003 NS CP (K)
Printed in Japan

The mark ★ shows major revised points.

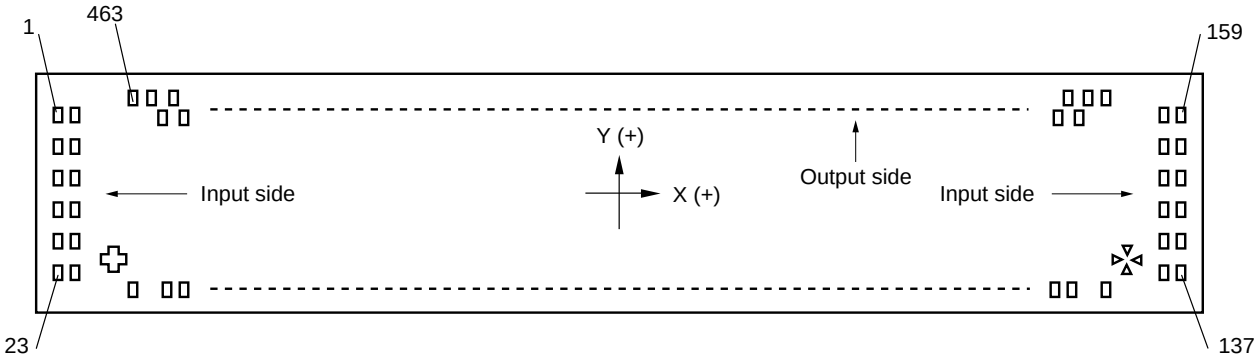
★ 1. BLOCK DIAGRAM



Note LS2 shifts CMOS level and output level (V_{DD2} to V_{EE}).

Remark /xxx indicates active low signal.

2. PIN CONFIGURATION (Bump Surface)



• Chip size: (1.14 ± 0.02) x (18.03 ± 0.02) mm^2 (After sawing)

• Alignment mark coordinate (mark center, unit: μm)

X	Y	Shape of alignment mark
–8545	–400	Type A
8545	–400	Type B

Refer to the figure below for more detail.

• Alignment mark

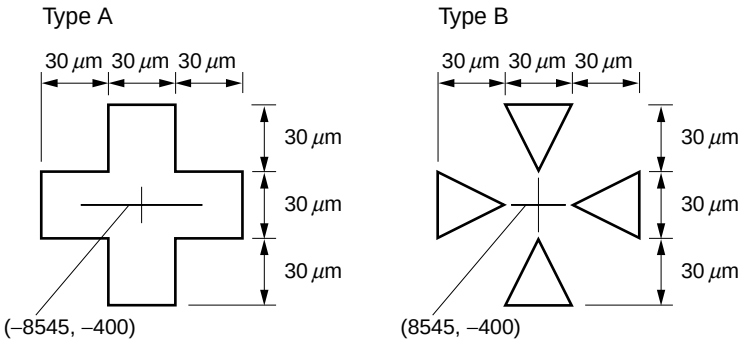


Table 2–1. Pad Coordinate (1/5)

PAD No.	PAD Name	X[μm]	Y[μm]	Bump Size (X:Y)[μm]
1	PASS	-8849.0	409.0	50:50
2	PASS	-8779.0	409.0	50:50
3	VEE	-8849.0	334.0	50:50
4	VEE	-8779.0	334.0	50:50
5	VEE	-8849.0	259.0	50:50
6	VEE	-8779.0	259.0	50:50
7	VEE	-8849.0	184.0	50:50
8	VEE	-8779.0	184.0	50:50
9	/OE	-8849.0	109.0	50:50
10	/OE	-8779.0	109.0	50:50
11	/AO	-8849.0	34.0	50:50
12	/AO	-8779.0	34.0	50:50
13	VDD2	-8849.0	-41.0	50:50
14	VDD2	-8779.0	-41.0	50:50
15	VDD1	-8849.0	-116.0	50:50
16	VDD1	-8779.0	-116.0	50:50
17	R,/L	-8849.0	-191.0	50:50
18	R,/L	-8779.0	-191.0	50:50
19	VSS	-8849.0	-266.0	50:50
20	VSS	-8779.0	-266.0	50:50
21	CLK	-8849.0	-341.0	50:50
22	CLK	-8779.0	-341.0	50:50
23	STVL	-8849.0	-416.0	50:50
24	STVL	-8779.0	-416.0	50:50
25	DUMMY	-8415.0	-437.0	60:90
26	DUMMY	-7722.0	-437.0	60:90
27	DUMMY	-7618.0	-437.0	60:90
28	DUMMY	-7514.0	-437.0	60:90
29	DUMMY	-7410.0	-437.0	60:90
30	DUMMY	-7306.0	-437.0	60:90
31	DUMMY	-7202.0	-437.0	60:90
32	DUMMY	-7098.0	-437.0	60:90
33	DUMMY	-6994.0	-437.0	60:90
34	DUMMY	-6890.0	-437.0	60:90
35	DUMMY	-6786.0	-437.0	60:90
36	DUMMY	-6682.0	-437.0	60:90
37	DUMMY	-6578.0	-437.0	60:90
38	DUMMY	-6474.0	-437.0	60:90
39	DUMMY	-6370.0	-437.0	60:90
40	DUMMY	-6266.0	-437.0	60:90
41	DUMMY	-6162.0	-437.0	60:90
42	DUMMY	-6058.0	-437.0	60:90
43	DUMMY	-5954.0	-437.0	60:90
44	DUMMY	-5850.0	-437.0	60:90
45	DUMMY	-5746.0	-437.0	60:90
46	DUMMY	-5642.0	-437.0	60:90
47	DUMMY	-5538.0	-437.0	60:90
48	DUMMY	-5434.0	-437.0	60:90
49	DUMMY	-5330.0	-437.0	60:90
50	DUMMY	-5226.0	-437.0	60:90

PAD No.	PAD Name	X[μm]	Y[μm]	Bump Size (X:Y)[μm]
51	DUMMY	-5122.0	-437.0	60:90
52	DUMMY	-5018.0	-437.0	60:90
53	DUMMY	-4914.0	-437.0	60:90
54	DUMMY	-4810.0	-437.0	60:90
55	DUMMY	-4706.0	-437.0	60:90
56	DUMMY	-4602.0	-437.0	60:90
57	DUMMY	-4498.0	-437.0	60:90
58	DUMMY	-4394.0	-437.0	60:90
59	DUMMY	-4290.0	-437.0	60:90
60	DUMMY	-2106.0	-437.0	60:90
61	DUMMY	-2002.0	-437.0	60:90
62	DUMMY	-1898.0	-437.0	60:90
63	DUMMY	-1794.0	-437.0	60:90
64	DUMMY	-1690.0	-437.0	60:90
65	DUMMY	-1586.0	-437.0	60:90
66	DUMMY	-1482.0	-437.0	60:90
67	DUMMY	-1378.0	-437.0	60:90
68	DUMMY	-1274.0	-437.0	60:90
69	DUMMY	-1170.0	-437.0	60:90
70	DUMMY	-1066.0	-437.0	60:90
71	DUMMY	-962.0	-437.0	60:90
72	DUMMY	-858.0	-437.0	60:90
73	DUMMY	-754.0	-437.0	60:90
74	DUMMY	-650.0	-437.0	60:90
75	DUMMY	-546.0	-437.0	60:90
76	DUMMY	-442.0	-437.0	60:90
77	DUMMY	-338.0	-437.0	60:90
78	DUMMY	-234.0	-437.0	60:90
79	DUMMY	-130.0	-437.0	60:90
80	DUMMY	-26.0	-437.0	60:90
81	DUMMY	78.0	-437.0	60:90
82	DUMMY	182.0	-437.0	60:90
83	DUMMY	286.0	-437.0	60:90
84	DUMMY	390.0	-437.0	60:90
85	DUMMY	494.0	-437.0	60:90
86	DUMMY	598.0	-437.0	60:90
87	DUMMY	702.0	-437.0	60:90
88	DUMMY	806.0	-437.0	60:90
89	DUMMY	910.0	-437.0	60:90
90	DUMMY	1014.0	-437.0	60:90
91	DUMMY	1118.0	-437.0	60:90
92	DUMMY	1222.0	-437.0	60:90
93	DUMMY	1326.0	-437.0	60:90
94	DUMMY	1430.0	-437.0	60:90
95	DUMMY	1534.0	-437.0	60:90
96	DUMMY	1638.0	-437.0	60:90
97	DUMMY	1742.0	-437.0	60:90
98	DUMMY	1846.0	-437.0	60:90
99	DUMMY	1950.0	-437.0	60:90
100	DUMMY	2054.0	-437.0	60:90

Table 2–1. Pad Coordinate (2/5)

PAD No.	PAD Name	X[μm]	Y[μm]	Bump Size (X:Y)[μm]
101	DUMMY	4238.0	-437.0	60:90
102	DUMMY	4342.0	-437.0	60:90
103	DUMMY	4446.0	-437.0	60:90
104	DUMMY	4550.0	-437.0	60:90
105	DUMMY	4654.0	-437.0	60:90
106	DUMMY	4758.0	-437.0	60:90
107	DUMMY	4862.0	-437.0	60:90
108	DUMMY	4966.0	-437.0	60:90
109	DUMMY	5070.0	-437.0	60:90
110	DUMMY	5174.0	-437.0	60:90
111	DUMMY	5278.0	-437.0	60:90
112	DUMMY	5382.0	-437.0	60:90
113	DUMMY	5486.0	-437.0	60:90
114	DUMMY	5590.0	-437.0	60:90
115	DUMMY	5694.0	-437.0	60:90
116	DUMMY	5798.0	-437.0	60:90
117	DUMMY	5902.0	-437.0	60:90
118	DUMMY	6006.0	-437.0	60:90
119	DUMMY	6110.0	-437.0	60:90
120	DUMMY	6214.0	-437.0	60:90
121	DUMMY	6318.0	-437.0	60:90
122	DUMMY	6422.0	-437.0	60:90
123	DUMMY	6526.0	-437.0	60:90
124	DUMMY	6630.0	-437.0	60:90
125	DUMMY	6734.0	-437.0	60:90
126	DUMMY	6838.0	-437.0	60:90
127	DUMMY	6942.0	-437.0	60:90
128	DUMMY	7046.0	-437.0	60:90
129	DUMMY	7150.0	-437.0	60:90
130	DUMMY	7254.0	-437.0	60:90
131	DUMMY	7358.0	-437.0	60:90
132	DUMMY	7462.0	-437.0	60:90
133	DUMMY	7566.0	-437.0	60:90
134	DUMMY	7670.0	-437.0	60:90
135	DUMMY	8415.0	-437.0	60:90
136	STVR	8770.0	-416.0	50:50
137	STVR	8840.0	-416.0	50:50
138	CLK	8770.0	-341.0	50:50
139	CLK	8840.0	-341.0	50:50
140	VSS	8770.0	-266.0	50:50
141	VSS	8840.0	-266.0	50:50
142	R,/L	8770.0	-191.0	50:50
143	R,/L	8840.0	-191.0	50:50
144	VDD1	8770.0	-116.0	50:50
145	VDD1	8840.0	-116.0	50:50
146	VDD2	8770.0	-41.0	50:50
147	VDD2	8840.0	-41.0	50:50
148	/AO	8770.0	34.0	50:50
149	/AO	8840.0	34.0	50:50
150	/OE	8770.0	109.0	50:50

PAD No.	PAD Name	X[μm]	Y[μm]	Bump Size (X:Y)[μm]
151	/OE	8840.0	109.0	50:50
152	VEE	8770.0	184.0	50:50
153	VEE	8840.0	184.0	50:50
154	VEE	8770.0	259.0	50:50
155	VEE	8840.0	259.0	50:50
156	VEE	8770.0	334.0	50:50
157	VEE	8840.0	334.0	50:50
158	PASS	8770.0	409.0	50:50
159	PASS	8840.0	409.0	50:50
160	DUMMY	7878.0	459.0	60:45
161	O0	7826.0	364.0	60:45
162	O1	7774.0	459.0	60:45
163	O2	7722.0	364.0	60:45
164	O3	7670.0	459.0	60:45
165	O4	7618.0	364.0	60:45
166	O5	7566.0	459.0	60:45
167	O6	7514.0	364.0	60:45
168	O7	7462.0	459.0	60:45
169	O8	7410.0	364.0	60:45
170	O9	7358.0	459.0	60:45
171	O10	7306.0	364.0	60:45
172	O11	7254.0	459.0	60:45
173	O12	7202.0	364.0	60:45
174	O13	7150.0	459.0	60:45
175	O14	7098.0	364.0	60:45
176	O15	7046.0	459.0	60:45
177	O16	6994.0	364.0	60:45
178	O17	6942.0	459.0	60:45
179	O18	6890.0	364.0	60:45
180	O19	6838.0	459.0	60:45
181	O20	6786.0	364.0	60:45
182	O21	6734.0	459.0	60:45
183	O22	6682.0	364.0	60:45
184	O23	6630.0	459.0	60:45
185	O24	6578.0	364.0	60:45
186	O25	6526.0	459.0	60:45
187	O26	6474.0	364.0	60:45
188	O27	6422.0	459.0	60:45
189	O28	6370.0	364.0	60:45
190	O29	6318.0	459.0	60:45
191	O30	6266.0	364.0	60:45
192	O31	6214.0	459.0	60:45
193	O32	6162.0	364.0	60:45
194	O33	6110.0	459.0	60:45
195	O34	6058.0	364.0	60:45
196	O35	6006.0	459.0	60:45
197	O36	5954.0	364.0	60:45
198	O37	5902.0	459.0	60:45
199	O38	5850.0	364.0	60:45
200	O39	5798.0	459.0	60:45

Table 2–1. Pad Coordinate (3/5)

PAD No.	PAD Name	X[μm]	Y[μm]	Bump Size (X:Y)[μm]
201	O40	5746.0	364.0	60:45
202	O41	5694.0	459.0	60:45
203	O42	5642.0	364.0	60:45
204	O43	5590.0	459.0	60:45
205	O44	5538.0	364.0	60:45
206	O45	5486.0	459.0	60:45
207	O46	5434.0	364.0	60:45
208	O47	5382.0	459.0	60:45
209	O48	5330.0	364.0	60:45
210	O49	5278.0	459.0	60:45
211	O50	5226.0	364.0	60:45
212	O51	5174.0	459.0	60:45
213	O52	5122.0	364.0	60:45
214	O53	5070.0	459.0	60:45
215	O54	5018.0	364.0	60:45
216	O55	4966.0	459.0	60:45
217	O56	4914.0	364.0	60:45
218	O57	4862.0	459.0	60:45
219	O58	4810.0	364.0	60:45
220	O59	4758.0	459.0	60:45
221	O60	4706.0	364.0	60:45
222	O61	4654.0	459.0	60:45
223	O62	4602.0	364.0	60:45
224	O63	4550.0	459.0	60:45
225	O64	4498.0	364.0	60:45
226	O65	4446.0	459.0	60:45
227	O66	4394.0	364.0	60:45
228	O67	4342.0	459.0	60:45
229	O68	4290.0	364.0	60:45
230	O69	4238.0	459.0	60:45
231	O70	4186.0	364.0	60:45
232	O71	4134.0	459.0	60:45
233	O72	4082.0	364.0	60:45
234	O73	4030.0	459.0	60:45
235	O74	3978.0	364.0	60:45
236	O75	3926.0	459.0	60:45
237	O76	3874.0	364.0	60:45
238	O77	3822.0	459.0	60:45
239	O78	3770.0	364.0	60:45
240	O79	3718.0	459.0	60:45
241	O80	3666.0	364.0	60:45
242	O81	3614.0	459.0	60:45
243	O82	3562.0	364.0	60:45
244	O83	3510.0	459.0	60:45
245	O84	3458.0	364.0	60:45
246	O85	3406.0	459.0	60:45
247	O86	3354.0	364.0	60:45
248	O87	3302.0	459.0	60:45
249	O88	3250.0	364.0	60:45
250	O89	3198.0	459.0	60:45

PAD No.	PAD Name	X[μm]	Y[μm]	Bump Size (X:Y)[μm]
252	O90	3146.0	364.0	60:45
252	O91	3094.0	459.0	60:45
253	O92	3042.0	364.0	60:45
254	O93	2990.0	459.0	60:45
255	O94	2938.0	364.0	60:45
256	O95	2886.0	459.0	60:45
257	O96	2834.0	364.0	60:45
258	O97	2782.0	459.0	60:45
259	O98	2730.0	364.0	60:45
260	O99	2678.0	459.0	60:45
261	O100	2626.0	364.0	60:45
262	O101	2574.0	459.0	60:45
263	O102	2522.0	364.0	60:45
264	O103	2470.0	459.0	60:45
265	O104	2418.0	364.0	60:45
266	O105	2366.0	459.0	60:45
267	O106	2314.0	364.0	60:45
268	O107	2262.0	459.0	60:45
269	O108	2210.0	364.0	60:45
270	O109	2158.0	459.0	60:45
271	O110	2106.0	364.0	60:45
272	O111	2054.0	459.0	60:45
273	O112	2002.0	364.0	60:45
274	O113	1950.0	459.0	60:45
275	O114	1898.0	364.0	60:45
276	O115	1846.0	459.0	60:45
277	O116	1794.0	364.0	60:45
278	O117	1742.0	459.0	60:45
279	O118	1690.0	364.0	60:45
280	O119	1638.0	459.0	60:45
281	O120	1586.0	364.0	60:45
282	O121	1534.0	459.0	60:45
283	O122	1482.0	364.0	60:45
284	O123	1430.0	459.0	60:45
285	O124	1378.0	364.0	60:45
286	O125	1326.0	459.0	60:45
287	O126	1274.0	364.0	60:45
288	O127	1222.0	459.0	60:45
289	O128	1170.0	364.0	60:45
290	O129	1118.0	459.0	60:45
291	O130	1066.0	364.0	60:45
292	O131	1014.0	459.0	60:45
293	O132	962.0	364.0	60:45
294	O133	910.0	459.0	60:45
295	O134	858.0	364.0	60:45
296	O135	806.0	459.0	60:45
297	O136	754.0	364.0	60:45
298	O137	702.0	459.0	60:45
299	O138	650.0	364.0	60:45
300	O139	598.0	459.0	60:45

Table 2–1. Pad Coordinate (4/5)

PAD No.	PAD Name	X[μm]	Y[μm]	Bump Size (X:Y)[μm]
301	O140	546.0	364.0	60:45
302	O141	494.0	459.0	60:45
303	O142	442.0	364.0	60:45
304	O143	390.0	459.0	60:45
305	O144	338.0	364.0	60:45
306	O145	286.0	459.0	60:45
307	O146	234.0	364.0	60:45
308	O147	182.0	459.0	60:45
309	O148	130.0	364.0	60:45
310	O149	78.0	459.0	60:45
311	O150	26.0	364.0	60:45
312	O151	-26.0	459.0	60:45
313	O152	-78.0	364.0	60:45
314	O153	-130.0	459.0	60:45
315	O154	-182.0	364.0	60:45
316	O155	-234.0	459.0	60:45
317	O156	-286.0	364.0	60:45
318	O157	-338.0	459.0	60:45
319	O158	-390.0	364.0	60:45
320	O159	-442.0	459.0	60:45
321	O160	-494.0	364.0	60:45
322	O161	-546.0	459.0	60:45
323	O162	-598.0	364.0	60:45
324	O163	-650.0	459.0	60:45
325	O164	-702.0	364.0	60:45
326	O165	-754.0	459.0	60:45
327	O166	-806.0	364.0	60:45
328	O167	-858.0	459.0	60:45
329	O168	-910.0	364.0	60:45
330	O169	-962.0	459.0	60:45
331	O170	-1014.0	364.0	60:45
332	O171	-1066.0	459.0	60:45
333	O172	-1118.0	364.0	60:45
334	O173	-1170.0	459.0	60:45
335	O174	-1222.0	364.0	60:45
336	O175	-1274.0	459.0	60:45
337	O176	-1326.0	364.0	60:45
338	O177	-1378.0	459.0	60:45
339	O178	-1430.0	364.0	60:45
340	O179	-1482.0	459.0	60:45
341	O180	-1534.0	364.0	60:45
342	O181	-1586.0	459.0	60:45
343	O182	-1638.0	364.0	60:45
344	O183	-1690.0	459.0	60:45
345	O184	-1742.0	364.0	60:45
346	O185	-1794.0	459.0	60:45
347	O186	-1846.0	364.0	60:45
348	O187	-1898.0	459.0	60:45
349	O188	-1950.0	364.0	60:45
350	O189	-2002.0	459.0	60:45

PAD No.	PAD Name	X[μm]	Y[μm]	Bump Size (X:Y)[μm]
351	O190	-2054.0	364.0	60:45
352	O191	-2106.0	459.0	60:45
353	O192	-2158.0	364.0	60:45
354	O193	-2210.0	459.0	60:45
355	O194	-2262.0	364.0	60:45
356	O195	-2314.0	459.0	60:45
357	O196	-2366.0	364.0	60:45
358	O197	-2418.0	459.0	60:45
359	O198	-2470.0	364.0	60:45
360	O199	-2522.0	459.0	60:45
361	O200	-2574.0	364.0	60:45
362	O201	-2626.0	459.0	60:45
363	O202	-2678.0	364.0	60:45
364	O203	-2730.0	459.0	60:45
365	O204	-2782.0	364.0	60:45
366	O205	-2834.0	459.0	60:45
367	O206	-2886.0	364.0	60:45
368	O207	-2938.0	459.0	60:45
369	O208	-2990.0	364.0	60:45
370	O209	-3042.0	459.0	60:45
371	O210	-3094.0	364.0	60:45
372	O211	-3146.0	459.0	60:45
373	O212	-3198.0	364.0	60:45
374	O213	-3250.0	459.0	60:45
375	O214	-3302.0	364.0	60:45
376	O215	-3354.0	459.0	60:45
377	O216	-3406.0	364.0	60:45
378	O217	-3458.0	459.0	60:45
379	O218	-3510.0	364.0	60:45
380	O219	-3562.0	459.0	60:45
381	O220	-3614.0	364.0	60:45
382	O221	-3666.0	459.0	60:45
383	O222	-3718.0	364.0	60:45
384	O223	-3770.0	459.0	60:45
385	O224	-3822.0	364.0	60:45
386	O225	-3874.0	459.0	60:45
387	O226	-3926.0	364.0	60:45
388	O227	-3978.0	459.0	60:45
389	O228	-4030.0	364.0	60:45
390	O229	-4082.0	459.0	60:45
391	O230	-4134.0	364.0	60:45
392	O231	-4186.0	459.0	60:45
393	O232	-4238.0	364.0	60:45
394	O233	-4290.0	459.0	60:45
395	O234	-4342.0	364.0	60:45
396	O235	-4394.0	459.0	60:45
397	O236	-4446.0	364.0	60:45
398	O237	-4498.0	459.0	60:45
399	O238	-4550.0	364.0	60:45
400	O239	-4602.0	459.0	60:45

Table 2–1. Pad Coordinate (5/5)

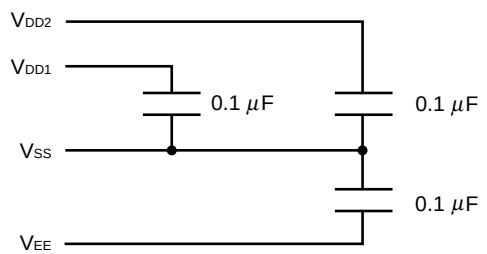
PAD No.	PAD Name	X[μm]	Y[μm]	Bump Size (X:Y)[μm]
401	O240	-4654.0	364.0	60:45
402	O241	-4706.0	459.0	60:45
403	O242	-4758.0	364.0	60:45
404	O243	-4810.0	459.0	60:45
405	O244	-4862.0	364.0	60:45
406	O245	-4914.0	459.0	60:45
407	O246	-4966.0	364.0	60:45
408	O247	-5018.0	459.0	60:45
409	O248	-5070.0	364.0	60:45
410	O249	-5122.0	459.0	60:45
411	O250	-5174.0	364.0	60:45
412	O251	-5226.0	459.0	60:45
413	O252	-5278.0	364.0	60:45
414	O253	-5330.0	459.0	60:45
415	O254	-5382.0	364.0	60:45
416	O255	-5434.0	459.0	60:45
417	O256	-5486.0	364.0	60:45
418	O257	-5538.0	459.0	60:45
419	O258	-5590.0	364.0	60:45
420	O259	-5642.0	459.0	60:45
421	O260	-5694.0	364.0	60:45
422	O261	-5746.0	459.0	60:45
423	O262	-5798.0	364.0	60:45
424	O263	-5850.0	459.0	60:45
425	O264	-5902.0	364.0	60:45
426	O265	-5954.0	459.0	60:45
427	O266	-6006.0	364.0	60:45
428	O267	-6058.0	459.0	60:45
429	O268	-6110.0	364.0	60:45
430	O269	-6162.0	459.0	60:45
431	O270	-6214.0	364.0	60:45
432	O271	-6266.0	459.0	60:45
433	O272	-6318.0	364.0	60:45
434	O273	-6370.0	459.0	60:45
435	O274	-6422.0	364.0	60:45
436	O275	-6474.0	459.0	60:45
437	O276	-6526.0	364.0	60:45
438	O277	-6578.0	459.0	60:45
439	O278	-6630.0	364.0	60:45
440	O279	-6682.0	459.0	60:45
441	O280	-6734.0	364.0	60:45
442	O281	-6786.0	459.0	60:45
443	O282	-6838.0	364.0	60:45
444	O283	-6890.0	459.0	60:45
445	O284	-6942.0	364.0	60:45
446	O285	-6994.0	459.0	60:45
447	O286	-7046.0	364.0	60:45
448	O287	-7098.0	459.0	60:45
449	O288	-7150.0	364.0	60:45
450	O289	-7202.0	459.0	60:45
451	O290	-7254.0	364.0	60:45
452	O291	-7306.0	459.0	60:45
453	O292	-7358.0	364.0	60:45
454	O293	-7410.0	459.0	60:45
455	O294	-7462.0	364.0	60:45
456	O295	-7514.0	459.0	60:45
457	O296	-7566.0	364.0	60:45
458	O297	-7618.0	459.0	60:45
459	O298	-7670.0	364.0	60:45
460	O299	-7722.0	459.0	60:45
461	O300	-7774.0	364.0	60:45
462	O301	-7826.0	459.0	60:45
463	DUMMY	-7930.0	459.0	60:45

3. PIN FUNCTIONS

Pin Symbol	Pin Name	Pad No.	I/O	Description
O_1 to O_{300}	Driver output	162 to 461	Output	These pins output scan signals that drive the vertical direction (gate lines) of a TFT-LCD. The output signals change in synchronization with the rising edge of shift clock (CLK). The driver output amplitude is V_{DD2} to V_{EE}.
O_0, O_{301}	LCD panel auxiliary	161, 462	Output	Regardless of shift data, these pins output V_{EE} level.
R,/L	Shift direction control	17, 18, 142, 143	Input	The shift direction control pin of shift register. The shift directions of the shift registers are as follows. R,/L = H (right shift) : STVR → O_1 → O_{300} → STVL R,/L = L (left shift) : STVL → O_{300} → O_1 → STVR
STVR, STVL	Start pulse	23, 24, 136, 137	I/O	These refer to the input pins of the internal shift register. The start pulse is read at the rising edge of CLK, and scan signals are output from the driver output pins. The input level is V_{DD1} to V_{SS} (logic level).
CLK	Shift clock	21, 22, 138, 139	Input	This pin inputs a shift clock to the internal shift register. The shift operation is performed in synchronization with the rising edge of this input.
/OE	Output enable	9, 10, 150, 151	Input	When these pins go low level, the driver output is fixed to V_{EE} level. The shift registers are not cleared. Refer to **4. TIMING CHART** for details.
/AO	All-on control	11, 12, 148, 149	Input	When these pins go low level, all outputs are fixed to V_{DD2}. These pins are pulled up to the V_{DD1} power supply inside the IC.
DUMMY	Dummy	25 to 135, 160, 463	–	No dummy pins are connected with other pins inside the IC.
PASS	Pass line	1, 2, 158, 159	–	Connected together internal.
V_{DD1}	Logic power supply	15, 16, 144, 145	–	2.3 to 3.6 V
V_{DD2}	Driver positive power supply	13, 14, 146, 147	–	10 to 30 V The driver output: High level
V_{SS}	Logic ground	19, 20, 140, 141	–	Connect this pin to the ground of the system.
V_{EE}	Negative power supply for internal operation and driver	3 to 8, 152 to 157	–	–10 to –3.0 V

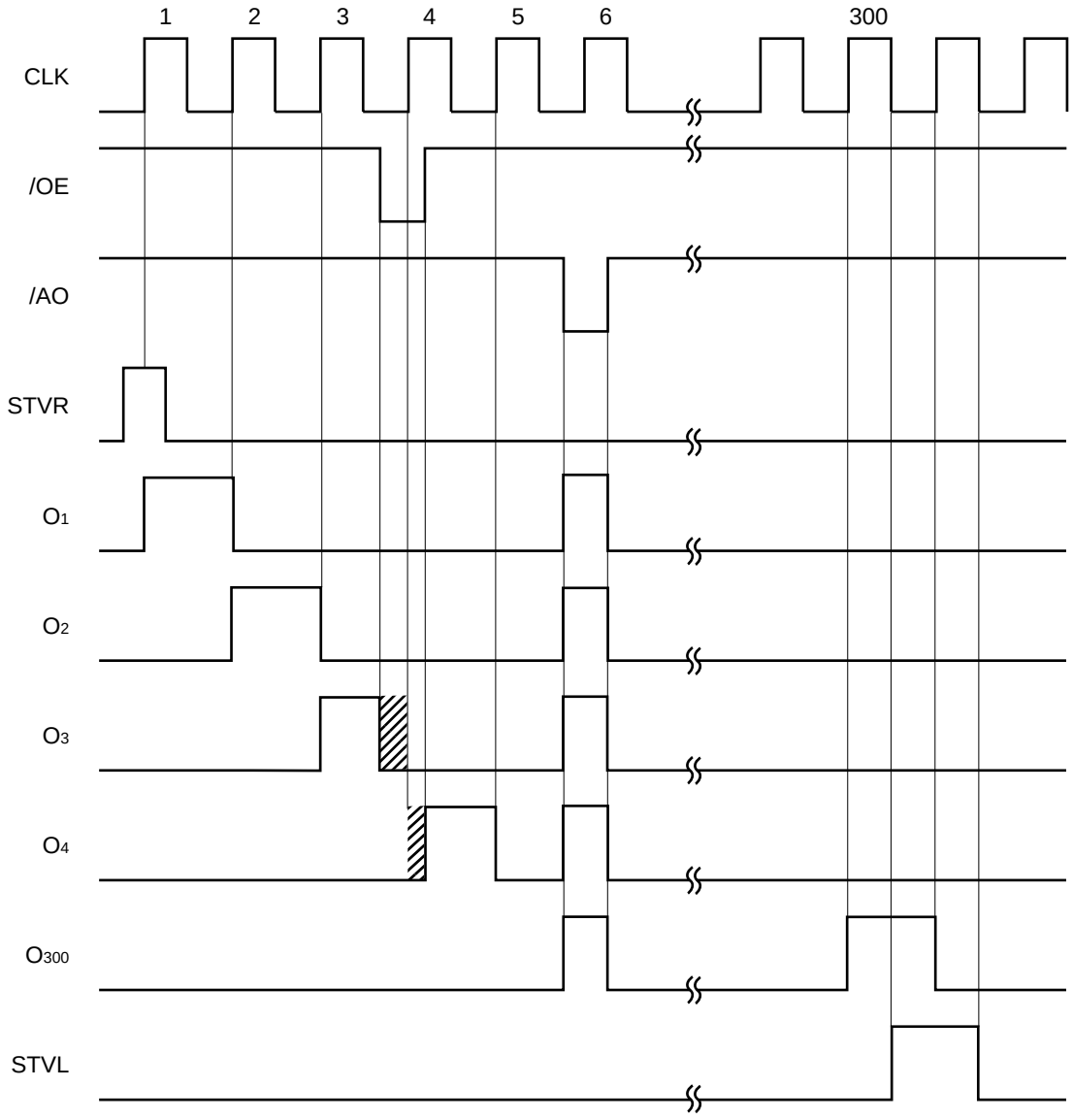
Cautions 1. To prevent latch up, turn on power to V_{DD1}, V_{EE}, V_{DD2} and logic input in this order. Turn off power in the reverse order. These power up/down sequences must be observed also during transition period.

2. Insert a capacitor of about 0.1 μF between each power line, as shown below, to secure noise margin such as V_{IH} and V_{IL}.

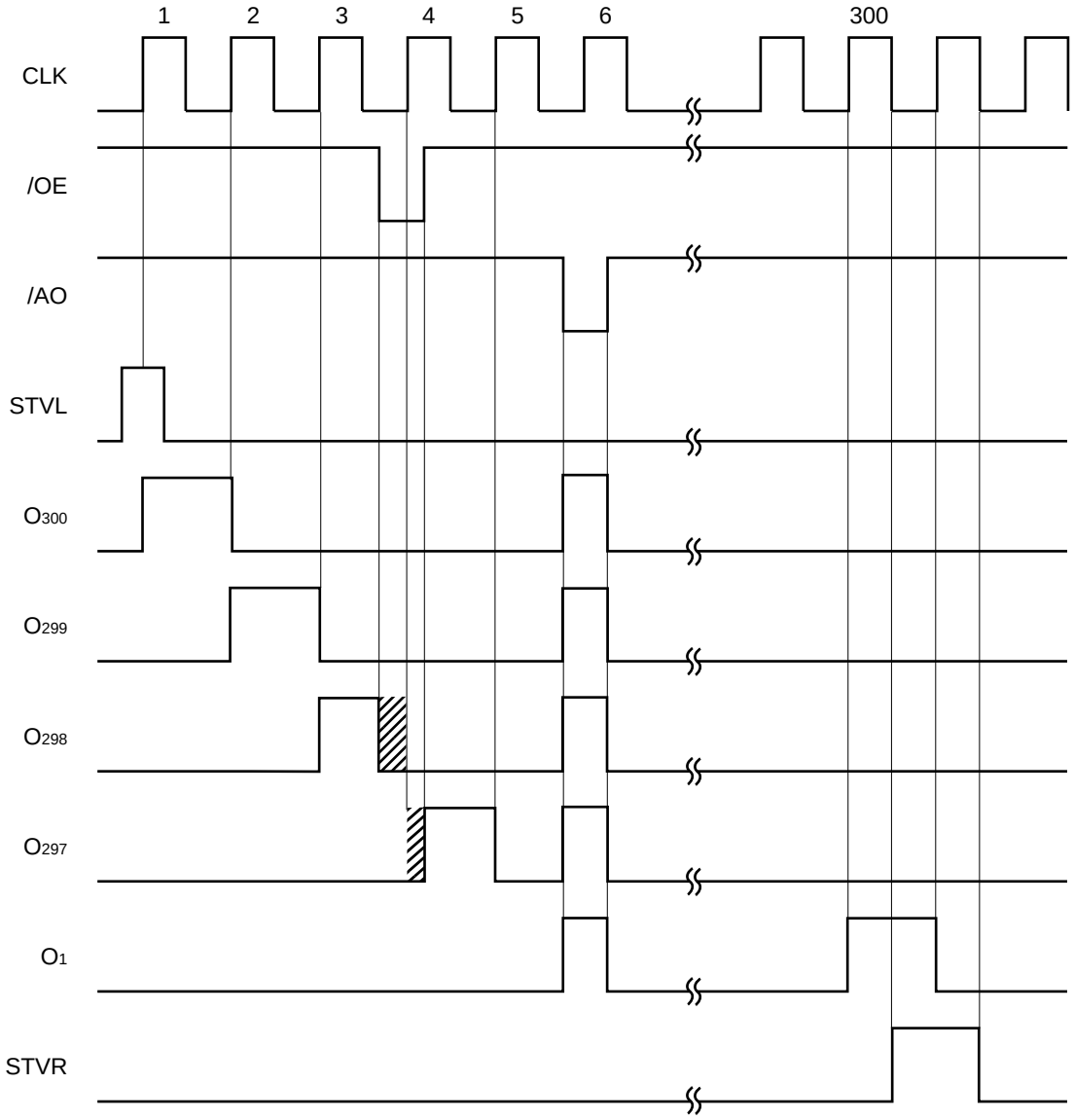


4. TIMING CHART

(1) R,/L = H



(2) R,/L = L



5. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{DD1}	–0.3 to +6.0	V
Driver positive supply voltage	V_{DD2}	–0.3 to +32	V
Internal operation negative supply voltage	V_{EE}	–17 to +0.3	V
Power supply voltage	V_{DD2} to V_{EE}	–0.3 to +41	V
Operating ambient temperature	T_A	–20 to +75	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range (T_A = –20 to +75°C, V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Logic supply voltage	V_{DD1}	V_{EE} cascade 100 Ω resistor	2.3	3.0	3.6	V
Driver positive supply voltage	V_{DD2}		10	20	30	V
Internal operation negative supply voltage	V_{EE}		–10	–6.5	–3.0	V
Power supply voltage	V_{DD2} to V_{EE}		13	26	40	V
Clock frequency	f_{CLK}				500	kHz

Electrical Characteristics (T_A = –20 to +75°C, V_{DD1} = 2.3 to 3.6 V, V_{DD2} = 10 to 30 V, V_{EE} = –10 to –3.0 V, V_{DD2} to V_{EE} = 13 to 40 V, V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH}	CLK, STVR (L) , R,/L, /OE, /AO,	0.7 V_{DD1}		V_{DD1}	V
Low-level input voltage	V_{IL}	V_{DD1} = 3.3 V	0		0.3 V_{DD1}	V
High-level driver output current	I_{OH1}	O_1 to O_{300}, V_O = V_{DD2} – 1.0 V	0.5			mA
Low-level driver output current	I_{OL1}	O_1 to O_{300}, V_O = V_{EE} + 1.0 V	–0.5			mA
High-level logic output current	I_{OH2}	STVR (L) , V_O = V_{DD1} – 0.5 V	200			μA
Low-level logic output current	I_{OL2}	STVR (L) , V_O = 0.5 V	200			μA
Pull-up impedance	R_{PU}	/AO	10	52.7	100	kΩ
Input leak current	I_{IL}	V_I = 0 V or 3.6 V, Except /AO			±1.0	μA
Static current dissipation	I_{DD1}	V_{DD1}, f_{CLK} = 50 kHz, /OE = H, No load, f_{STV} = 60 Hz		15.34	500	μA
	I_{DD2}	V_{DD2}, f_{CLK} = 50 kHz, /OE = H, No load, f_{STV} = 60 Hz		5.47	50	μA
	I_{EE}	V_{EE}, f_{CLK} = 50 kHz, /OE = H, No load, f_{STV} = 60 Hz	–550	–20.43		μA

Switching Characteristics (T_A = –20 to +75°C, V_{DD1} = 2.3 to 3.6 V, V_{DD2} = 10 to 30 V, V_{EE} = –10 to –3.0 V, V_{DD2} to V_{EE} = 13 to 40 V, V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output rise time	t_{TLH}	C_L = 300 pF, 10 to 90%			1400	ns
Output fall time	t_{THL}	C_L = 300 pF, 90 to 10%			1400	ns
STVR (L) delay time	t_{PHL1}	C_L = 15 pF,			450	ns
	t_{PLH1}	CLK → STVR (L)			450	ns
Driver output delay time	t_{PHL2}	C_L = 800 pF, CLK → O_n			1.5	μs
	t_{PLH2}				1.5	μs
/OE to driver output delay time	t_{PHL3}	C_L = 800 pF, /OE → O_n			1.5	μs
	t_{PLH3}				1.5	μs
/AO to driver output delay time	t_{PHL4}	C_L = 800 pF, /AO→ O_n			1.5	μs
	t_{PLH4}				1.5	μs

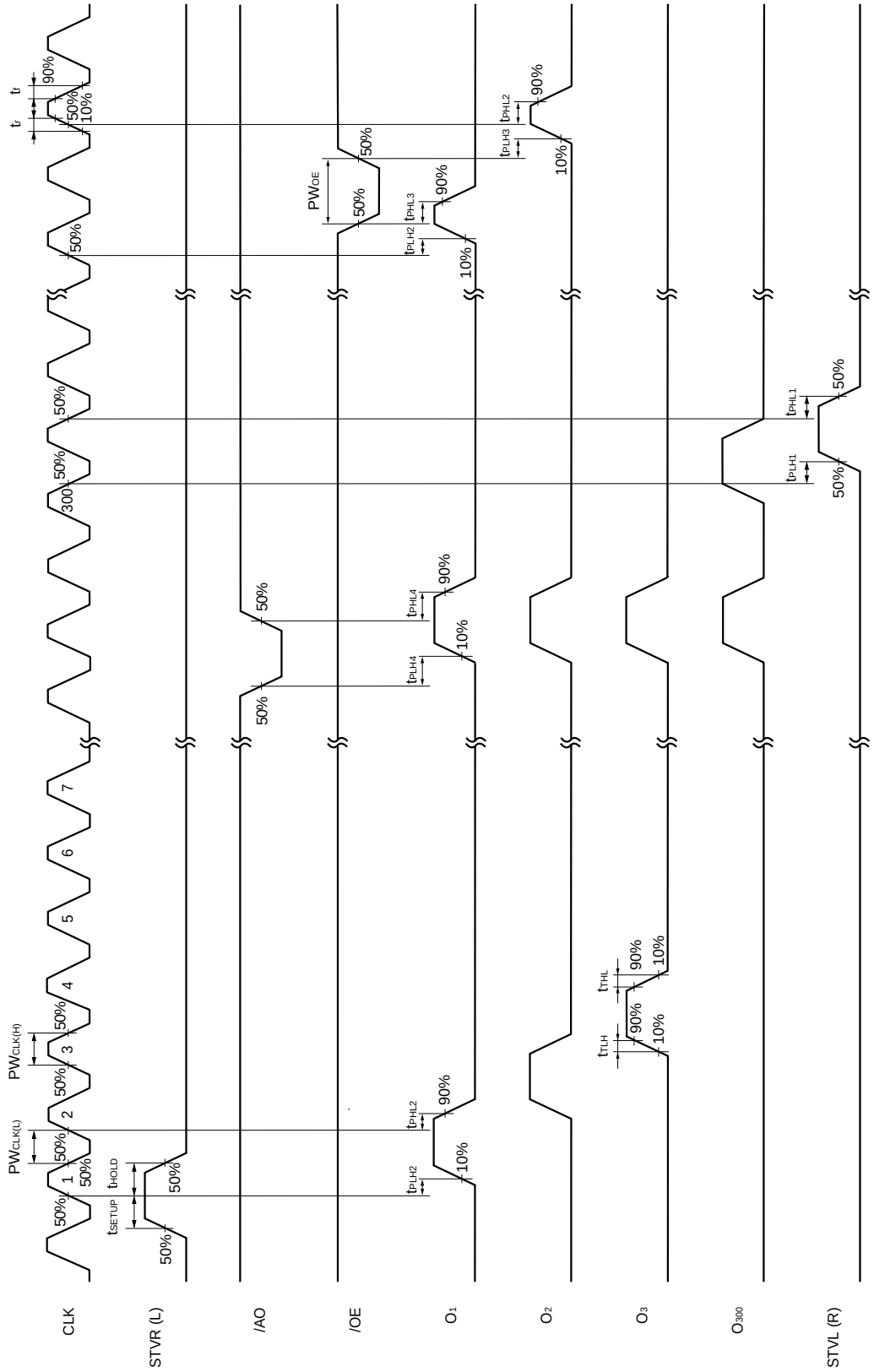
Timing Requirements (T_A = –20 to +75°C, V_{DD1} = 2.3 to 3.6 V, V_{DD2} = 10 to 30 V, V_{EE} = –10 to –3.0 V, V_{DD2} to V_{EE} = 13 to 40 V, V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock pulse high width	$PW_{CLK(H)}$		500			ns
Clock pulse low width	$PW_{CLK(L)}$		500			ns
STVR (L) setup time	t_{SETUP}	STVR (L) ↑ → CLK ↑	200			ns
STVR (L) hold time	t_{HOLD}	CLK ↑ → STVR (L) ↓	300			ns
Output enable pulse width	PW_{OE}	/OE	1.00			μs

Remark Unless otherwise specified, the input level is defined to be V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}.

Switching Characteristics Waveform (R,/L= H)

Unless otherwise specified, the input level is defined to be V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}.



NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades On NEC Semiconductor Devices (C11531E)

- **The information contained in this document is being issued in advance of the production cycle for the product. The parameters for the product may change before final production or NEC Electronics Corporation, at its own discretion, may withdraw the product prior to its production.**
- No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Electronics. NEC Electronics assumes no responsibility for any errors that may appear in this document.
- NEC Electronics does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC Electronics products listed in this document or any other liability arising from the use of such products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Electronics or others.
- Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of a customer's equipment shall be done under the full responsibility of the customer. NEC Electronics assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.
- While NEC Electronics endeavors to enhance the quality, reliability and safety of NEC Electronics products, customers agree and acknowledge that the possibility of defects thereof cannnot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC Electronics products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment and anti-failure features.
- NEC Electronics products are classified into the following three quality grades: "Standard", "Special", and "Specific". The "Specific" quality grade applies only to NEC Electronics products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of an NEC Electronics product depend on its quality grade, as indicated below. Customers must check the quality grade of each NEC Electronics products before using it in a particular application.

  "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots.

  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support).

  "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

The quality grade of NEC Electronics products is "Standard" unless otherwise expressly specified in NEC Electronics data sheets or data books, etc. If customers wish to use NEC Electronics products in applications not intended by NEC Electronics, they must contact an NEC Electronics sales representative in advance to determine NEC Electronics' willingness to support a given application.

(Note)

(1) "NEC Electronics" as used in this statement means NEC Electronics Corporation and also includes its majority-owned subsidiaries.

(2) "NEC Electronics products" means any product developed or manufactured by or for NEC Electronics (as defined above).