ISL80111, ISL80112, ISL80113

Ultra Low Dropout 1A, 2A, 3A Low Input Voltage NMOS LDOs

FN7841
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The ISL80111, ISL80112, and ISL80113 are ultra low dropout LDOs providing the optimum balance between performance, size and power consumption in size constrained designs for data communication, computing, storage and medical applications. These LDOs are specified for 1A, 2A, and 3A of output current and are optimized for low voltage conversions. Operating with a V_{IN} of 0.7V to 3.6V and with a legacy 2.9V to 5.5V on the BIAS, the V_{OUT} is adjustable from 0.5V to 3.3V. With a V_{IN} PSRR greater than 40dB at 100kHz makes these LDOs an ideal choice in noise sensitive applications. The guaranteed ±1.6% V_{OUT} accuracy overall conditions lend these parts to supplying an accurate voltage to the latest low voltage digital ICs.

An enable input allows the part to be placed into a low quiescent current shutdown mode. A submicron CMOS process is utilized for this product family to deliver best-in-class analog performance and overall value for applications in need of input voltage conversions typically below 2.5V. It also has the superior load transient regulation unique to a NMOS power stage. These LDOs consume significantly lower quiescent current as a function of load compared to bipolar LDOs.

Features

- Ultra low dropout: 75mV at 3A, (typical)
- Excellent V_{IN} PSRR: 70dB at 1kHz (typical)
- ±1.6% assured V_{OUT} accuracy for -40°C < T_J < +125°C
- Very fast load transient response
- Extensive protection and reporting features
- V_{IN} range: 0.7V to 3.6V, V_{OUT} range: 0.5V to 3.3V
- Small 10 Ld 3x3 DFN package

Applications

- Noise-sensitive instrumentation and medical systems
- Data acquisition and data communication systems
- Storage, telecommunications and server equipment
- Low voltage DSP, FPGA and ASIC core power supplies
- Post-regulation of switched mode power supplies

Related Literature

For a full list of related documents, visit our website:

- ISL80111, ISL80112, and ISL80113 device pages

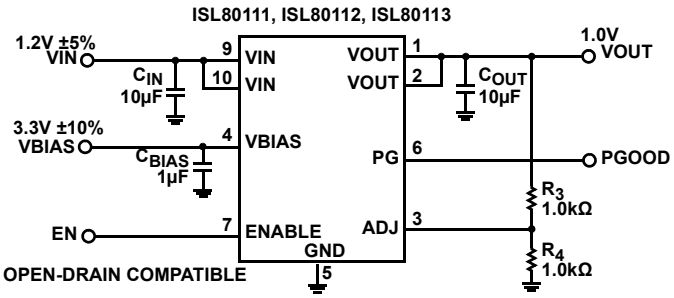


FIGURE 1. TYPICAL APPLICATION SCHEMATIC

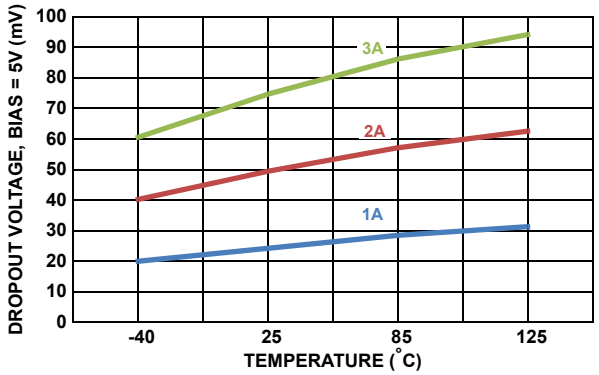


FIGURE 2. DROPOUT VOLTAGE OVER-TEMP AND I_{OUT}

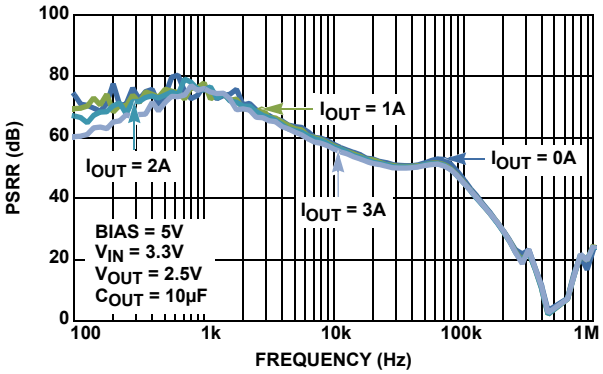


FIGURE 3. V_{IN} PSRR vs LOAD CURRENT (ISL80113)

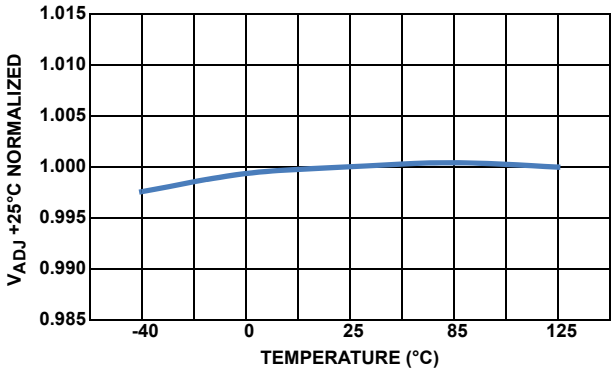


FIGURE 4. V_{ADJ} vs TEMPERATURE

Block Diagram

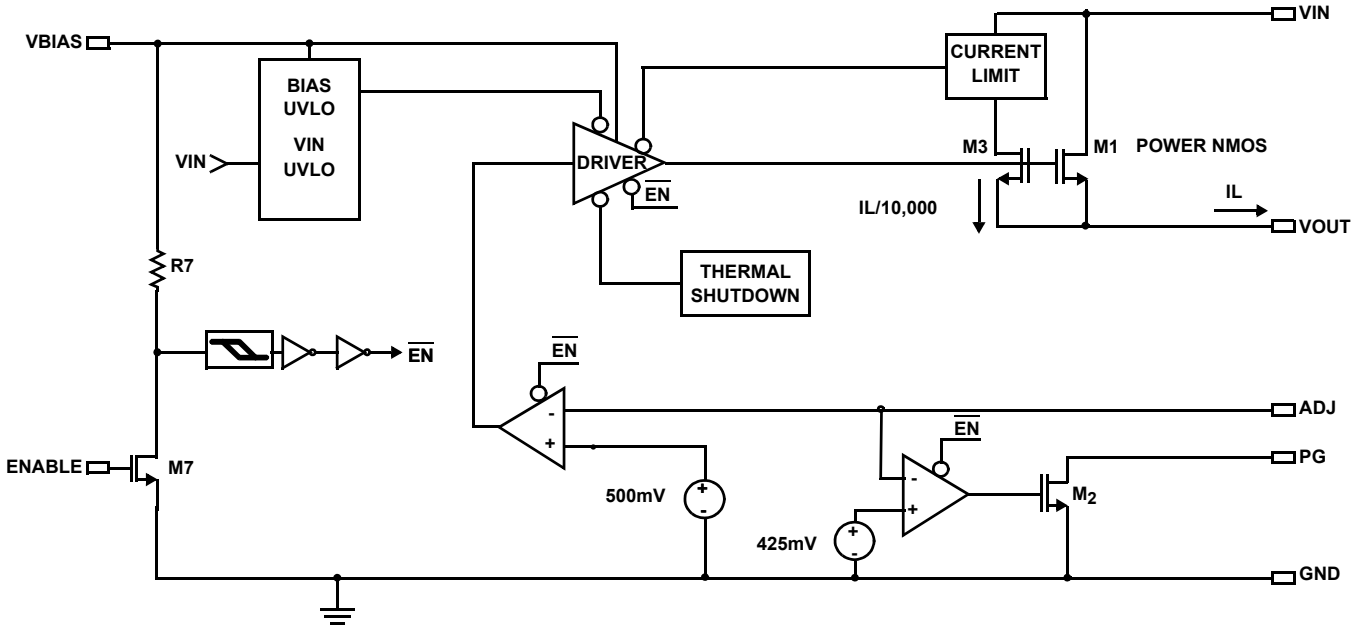
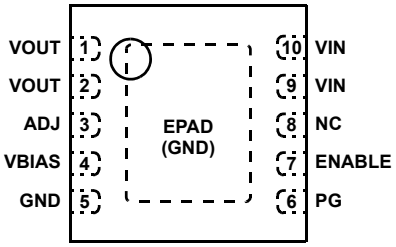


FIGURE 5. BLOCK DIAGRAM

Pin Configuration

ISL80111, ISL80112, ISL80113
(10 LD 3X3 DFN)
TOP VIEW



PIN NUMBER	PIN NAME	DESCRIPTION
1, 2	VOUT	Output voltage pin. Range 0.5V to 3.3V
3	ADJ	ADJ pin for externally setting V_{OUT}.
4	VBIAS	Bias voltage pin for internal control circuits. Range 2.9V to 5.5V
5	GND	Ground pin
6	PG	V_{OUT} in regulation signal. Logic low defines when V_{OUT} is not in regulation. Range 0V to BIAS
7	ENABLE	V_{IN} independent chip enable. TTL and CMOS compatible. Range 0V to V_{BIAS}. V_{EN} must always be less than or equal to the voltage applied to VBIAS. When this pin is not used, it must be tied to VBIAS.
8	NC	No Connect
9, 10	VIN	Input supply pins. Range 0.7V to 3.6V
-	EPAD	EPAD at ground potential. It is recommended to solder the EPAD to the ground plane.

Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	V_{OUT} (V)	TEMP RANGE (°C)	TAPE AND REEL (Units) (Note 1)	PACKAGE (RoHS COMPLIANT)	PKG DWG. #
ISL80111IRAJZ	1ADJ	ADJ	-40 to +125	-	10 Ld 3x3 DFN	L10.3x3
ISL80111IRAJZ-T	1ADJ	ADJ	-40 to +125	6k	10 Ld 3x3 DFN	L10.3x3
ISL80111IRAJZ-T7A	1ADJ	ADJ	-40 to +125	250	10 Ld 3x3 DFN	L10.3x3
ISL80112IRAJZ	2ADJ	ADJ	-40 to +125	-	10 Ld 3x3 DFN	L10.3x3
ISL80112IRAJZ-T	2ADJ	ADJ	-40 to +125	6k	10 Ld 3x3 DFN	L10.3x3
ISL80112IRAJZ-T7A	2ADJ	ADJ	-40 to +125	250	10 Ld 3x3 DFN	L10.3x3
ISL80113IRAJZ	3ADJ	ADJ	-40 to +125	-	10 Ld 3x3 DFN	L10.3x3
ISL80113IRAJZ-T	3ADJ	ADJ	-40 to +125	6k	10 Ld 3x3 DFN	L10.3x3
ISL80113IRAJZ-T7A	3ADJ	ADJ	-40 to +125	250	10 Ld 3x3 DFN	L10.3x3
ISL80111EVAL1Z	ISL80111 Evaluation Board					
ISL80112EVAL1Z	ISL80112 Evaluation Board					
ISL80113EVAL1Z	ISL80113 Evaluation Board					

NOTES:

1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL80111, ISL80112, and ISL80113 device pages for. For more information about MSL, see TB363.

TABLE 1. KEY DIFFERENCE BETWEEN FAMILY OF PARTS

PART NUMBER	I_{OUT} MAXIMUM
ISL80111	1A
ISL80112	2A
ISL80113	3A

Absolute Maximum Ratings

(Note 4)

VIN Relative to GND . . . . . -0.3 to +6V
VOUT Relative to GND . . . . . -0.3 to +4V
PG, ENABLE, ADJ, Relative to GND (Note 5) . . . . . -0.3 to +6V
VBIAS Relative to GND . . . . . -0.3V to +6V
PG Rated Current 10mA
ESD Rating
Human Body Model (Tested per JESD22-A114E) 4000V
Machine Model (Tested per JESD22-115-A) 300V
Charged Device Model 2000V
Latch-up 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld 3x3 DFN Package (Notes 6, 7)	48	4

θ_{JB} at Pin 3 (Note 8) . . . . . 14.7°C/W
θ_{JB} at Pin 5 (Note 8) . . . . . 8.9°C/W
Storage Temperature Range . . . . . -65°C to +150°C
Pb-free Reflow Profile . . . . . see TB493

Recommended Operating Conditions (Notes 4)

Junction Temperature Range . . . . . -40°C to +125°C
VIN Relative to GND (ISL80113) . . . . . V_{OUT} + 0.30V to 3.6V
VIN Relative to GND (ISL80112) . . . . . V_{OUT} + 0.25V to 3.6V
VIN Relative to GND (ISL80111) . . . . . V_{OUT} + 0.20V to 3.6V
Nominal V_{OUT} Range . . . . . 500mV to 3.3V
PG, ENABLE, ADJ, SS Relative to GND . . . . . 0V to 5.5V
VBIAS Relative to GND . . . . . 0V to 5.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. Absolute maximum ratings define limits of safe operation. Extended operation at these conditions may compromise reliability. Exceeding these limits will result in damage. Recommended operating conditions define limits where specifications are guaranteed.
5. Absolute maximum voltage rating is defined as the voltage applied for a lifetime average duty cycle above 6V of 1%.
6. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with direct attach features. See TB379.
7. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.
8. For θ_{JB}, the board temperature is taken on the board near the edge of the package, on a copper trace at either lead #3 or lead #5, as applicable. See TB379.

Electrical Specifications

Unless otherwise specified, V_{IN} = 3V, V_{BIAS} = 5.5V, V_{OUT} = 0.5V, T_J = +25°C, I_L = 0mA. Applications must follow thermal guidelines of the package to determine worst-case junction temperature. See the "Power Dissipation" on page 13 and TB379. **Boldface limits apply across junction temperature (T_J) range, -40°C to +125°C.** Pulse load techniques used by ATE to ensure T_J = T_A where datasheet limits are defined.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
DC CHARACTERISTICS						
V_{BIAS} UVLO	UVLO_BIAS_r	V_{BIAS} Rising		2.3	**2.9**	V
	UVLO_BIAS_f	V_{BIAS} Falling	**1.55**	2.1	**2.8**	V
V_{BIAS} UVLO Hysteresis	$UVLO_{B\_HYS}$			0.2		V
DC ADJ Pin Voltage Accuracy	V_{ADJ}	0.7V ≤ V_{IN} ≤ 3.6V, I_{LOAD} = 0A, 2.9V ≤ V_{BIAS} ≤ 5.5V, V_{OUT} = V_{ADJ}	**494**	502	**510**	mV
DC Input Line Regulation	(V_{OUT} low line-V_{OUT} high line)/V_{OUT} low line	2.9V < V_{IN} < 3.6V, V_{OUT} = 2.5V	**-0.18**	0.02	**0.18**	%
DC Bias Line Regulation	(V_{OUT} low line-V_{OUT} high line)/V_{OUT} low line	4.5V<V_{BIAS}<5.5V, V_{OUT} = 2.5V	**-0.28**	0.06	**0.28**	%
DC Output Load Regulation	(V_{OUT} no load-V_{OUT} high load)/V_{OUT} no load	0A < I_{LOAD} < Full Load, V_{OUT} = 2.5V	**-0.40**	-0.04	**0.40**	%
Feedback Input Current		V_{ADJ} = 0.5V		10	**80**	nA
V_{IN} Quiescent Current	I_Q (V_{IN})	V_{OUT} = 2.5V		8	**10**	mA
V_{IN} Quiescent Current	I_Q (V_{IN})	V_{OUT} = 3.3V, V_{IN} = 3.6V, V_{BIAS} = 5V		10.6		mA

Electrical Specifications Unless otherwise specified, V_{IN} = 3V, V_{BIAS} = 5.5V, V_{OUT} = 0.5V, T_J = +25°C, I_L = 0mA. Applications must follow thermal guidelines of the package to determine worst-case junction temperature. See the "Power Dissipation" on page 13 and TB379. **Boldface limits apply across junction temperature (T_J) range, -40°C to +125°C.** Pulse load techniques used by ATE to ensure T_J = T_A where datasheet limits are defined.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
V_{IN} Quiescent Current	I_Q (V_{IN})	V_{OUT} = 1.0V, V_{IN} = 1.4V, V_{BIAS} = 3.3V		3.5		mA
V_{BIAS} Quiescent Current	I_Q (V_{BIAS})	0 ≤ I_L ≤ 3A, 4.5V < V_{BIAS} < 5.5V (ISL80113)		2.9	**4.6**	mA
Ground Pin Current in Shutdown	I_{SHDN}	ENABLE Pin = 0.2V, TJ = +125°C		3	**20**	µA
V_{IN} Dropout Voltage (Note 10)	$V_{DO(VIN)}$	I_{LOAD} = 1A, V_{OUT} = 2.5V, V_{BIAS} = 4.5V (ISL80111)		27	**90**	mV
		I_{LOAD} = 2A, V_{OUT} = 2.5V, V_{BIAS} = 4.5V (ISL80112)		53	**115**	mV
		I_{LOAD} = 3A, V_{OUT} = 2.5V, V_{BIAS} = 4.5V (ISL80113)		75	**140**	mV
V_{BIAS} Dropout Voltage (Note 10)	$V_{DO(BIAS)}$	I_{LOAD} = 1A, V_{OUT} = 2.5V (ISL80111)		1.1	**1.3**	V
		I_{LOAD} = 2A, V_{OUT} = 2.5V (ISL80112)		1.2	**1.4**	V
		I_{LOAD} = 3A, V_{OUT} = 2.5V (ISL80113)		1.3	**1.5**	V
OVERCURRENT PROTECTION						
Output Short Circuit Current (3A Version)	ISC	V_{OUT} = 0.2V (ISL80113)		5.2		A
Output Short Circuit Current (2A Version)		V_{OUT} = 0.2V (ISL80112)		3.2		A
Output Short Circuit Current (1A Version)		V_{OUT} = 0.2V (ISL80111)		2.2		A
OVER-TEMPERATURE PROTECTION						
Thermal Shutdown Temperature	TSD			160		°C
Thermal Shutdown Hysteresis	TSDn			20		°C
AC CHARACTERISTICS						
Input Supply Ripple Rejection	PSRR(V_{IN})	f = 120Hz, I_{LOAD} = 1A		80		dB
	PSRR(V_{BIAS})	f = 120Hz, I_{LOAD} = 1A		60		dB
Output Noise Voltage	$e_{N(RMS)}$	BW = 100Hz ≤ f ≤ 100kHz, V_{BIAS} = 2.9V, V_{IN} = 1.6V, V_{OUT} = 1.2V, I_{LOAD} = 3A		38		μV_{RMS}
Spectral Noise Density	e_N	I_{LOAD} = 3A, f = 10Hz, V_{BIAS} = 2.9V, V_{IN} = 1.6V, V_{OUT} = 1.2V		3		$\mu V/\sqrt{Hz}$
		I_{LOAD} = 3A, f = 100Hz, V_{BIAS} = 2.9V, V_{IN} = 1.6V, V_{OUT} = 1.2V		1		$\mu V/\sqrt{Hz}$
DEVICE START-UP CHARACTERISTICS						
EN Start-up Time	t_{EN}	C_{OUT} = 10µF, I_{LOAD} = 1A		50		µs
BIAS Start-up Time	t_{BIAS}	C_{OUT} = 10µF, EN = BIAS		100		µs
ENABLE PIN CHARACTERISTICS						
Turn-on Threshold (Rising)		V_{IN} = 3.6V, V_{BIAS} = 5.5V	**400**	680	**850**	mV
Hysteresis		V_{IN} = 3.6V, V_{BIAS} = 5.5V	**60**	260	**330**	mV
PG PIN CHARACTERISTICS						
PG Flag Falling Threshold	PG_{TH}	V_{BIAS} = 5.5V	**71**	82	**93**	$\%V_{OUT}$
PG Flag Hysteresis	PGHYS	V_{BIAS} = 5.5V		9.3		$\%V_{OUT}$
PG Flag Low Voltage		I_{SINK} = 500µA		90	**130**	mV
PG Flag Leakage Current		PG = 5V, V_{BIAS} = 5.5V		11	**300**	nA

Electrical Specifications Unless otherwise specified, V_{IN} = 3V, V_{BIAS} = 5.5V, V_{OUT} = 0.5V, T_J = +25°C, I_L = 0mA. Applications must follow thermal guidelines of the package to determine worst-case junction temperature. See the "Power Dissipation" on page 13 and TB379. **Boldface limits apply across junction temperature (T_J) range, -40°C to +125°C.** Pulse load techniques used by ATE to ensure T_J = T_A where datasheet limits are defined.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
PG Flag Sink Current			7	10		mA

NOTES:

9. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
10. Dropout is defined by the difference in supply (V_{IN}, V_{BIAS}) and V_{OUT} when the supply produces a 2% drop in V_{OUT} from its nominal value, output voltage set to 2.5V.
11. For normal operation, V_{IN} must always be less than or equal to the voltage applied to V_{BIAS} and not greater than 3.6V. Part is protected against fault conditions where V_{IN} can be greater than V_{BIAS}.

Typical Operating Performance

Unless otherwise noted, V_{IN} = 1.8V, V_{BIAS} = 3.3V, V_{OUT} = 1.2V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_{LOAD} = 0A.

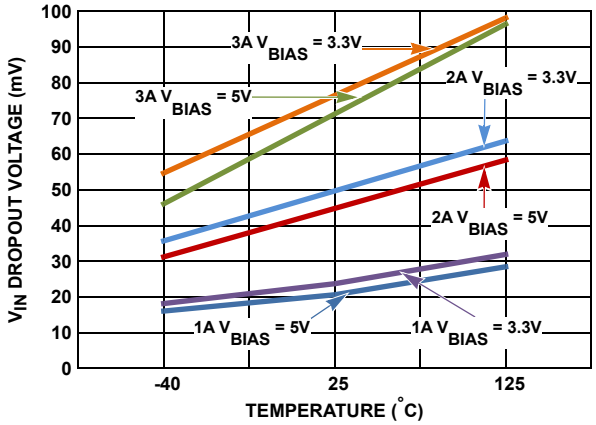


FIGURE 6. DROPOUT vs TEMPERATURE

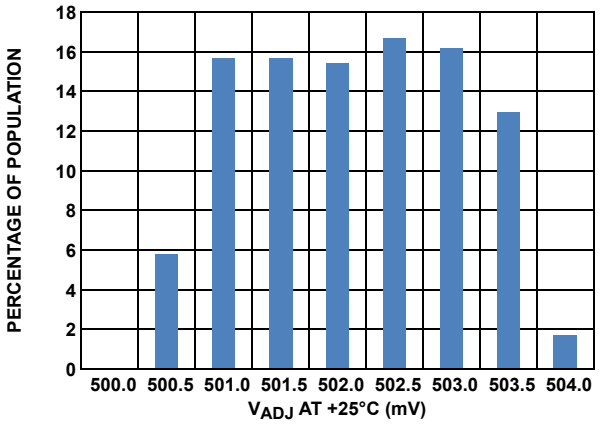


FIGURE 7. V_{ADJ} DISTRIBUTION

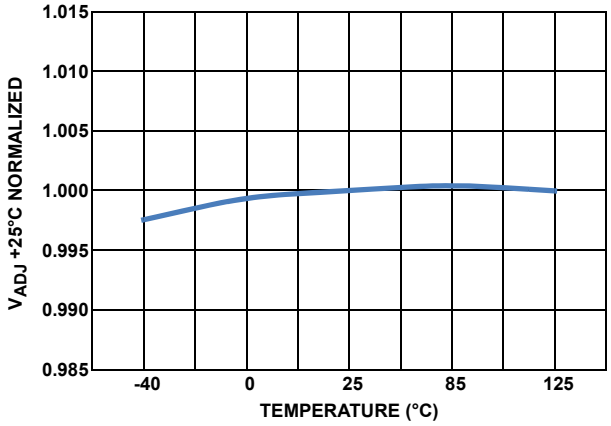


FIGURE 8. V_{ADJ} vs TEMPERATURE

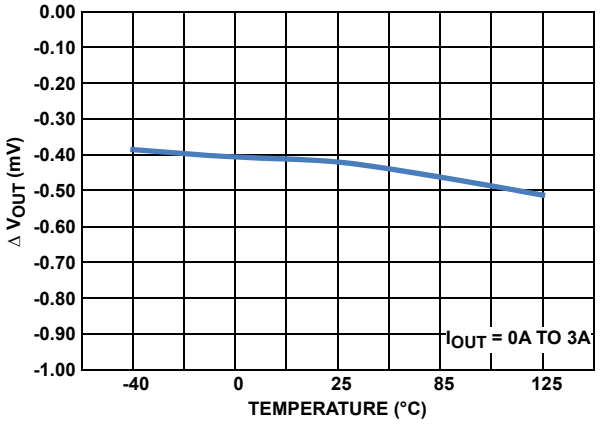


FIGURE 9. LOAD REGULATION vs TEMPERATURE

Typical Operating Performance

Unless otherwise noted, V_{IN} = 1.8V, V_{BIAS} = 3.3V, V_{OUT} = 1.2V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_{LOAD} = 0A. **(Continued)**

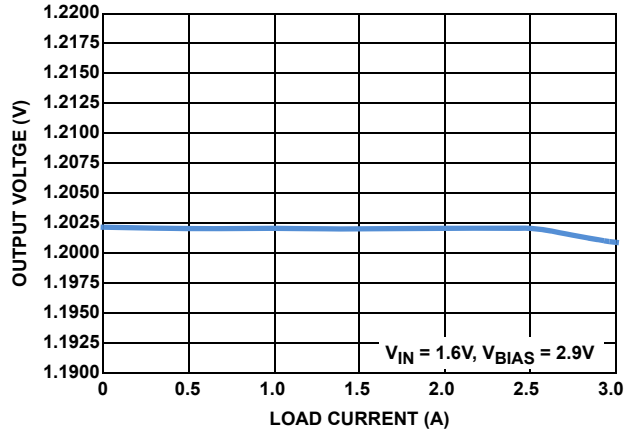


FIGURE 10. LOAD REGULATION, V_{OUT} vs I_{OUT}

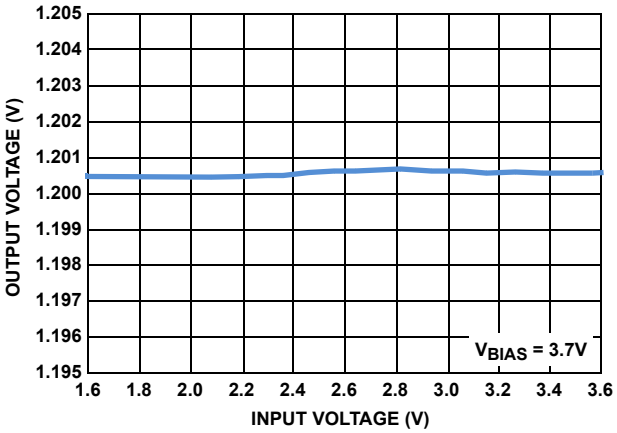


FIGURE 11. V_{IN} LINE REGULATION

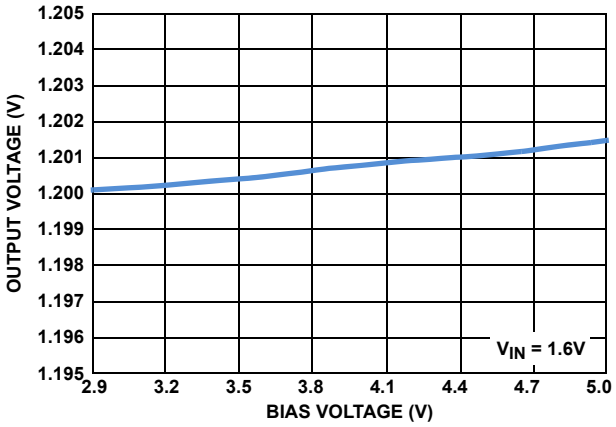


FIGURE 12. V_{BIAS} LINE REGULATION

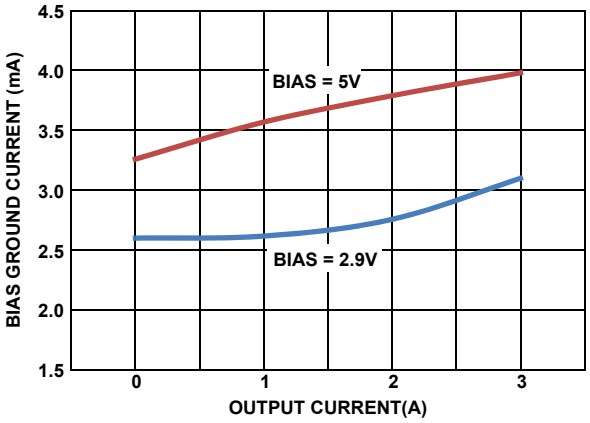


FIGURE 13. BIAS GROUND CURRENT vs LOAD CURRENT

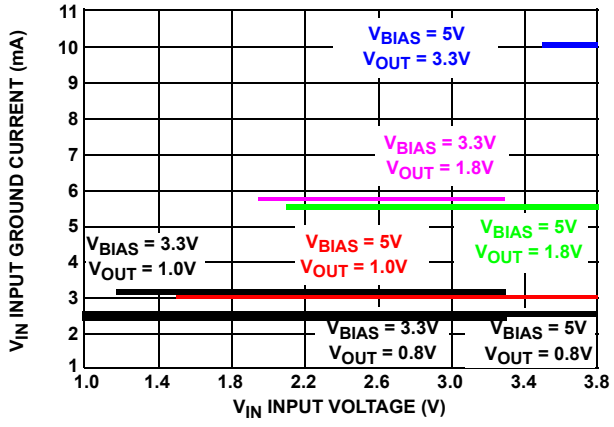


FIGURE 14. INPUT GROUND CURRENT vs V_{IN} and V_{OUT}

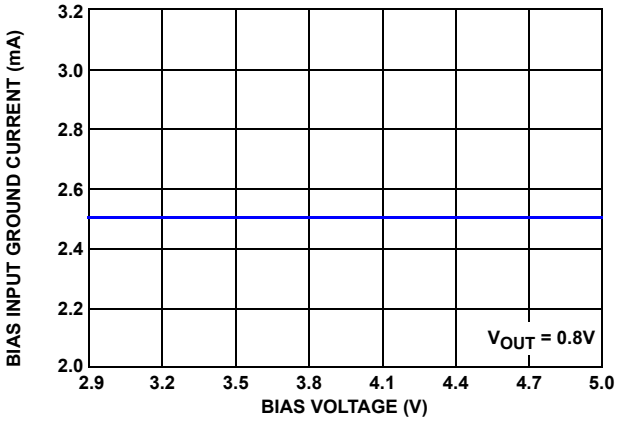


FIGURE 15. INPUT GROUND CURRENT vs V_{BIAS}

Typical Operating Performance

Unless otherwise noted, V_{IN} = 1.8V, V_{BIAS} = 3.3V, V_{OUT} = 1.2V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_{LOAD} = 0A. **(Continued)**

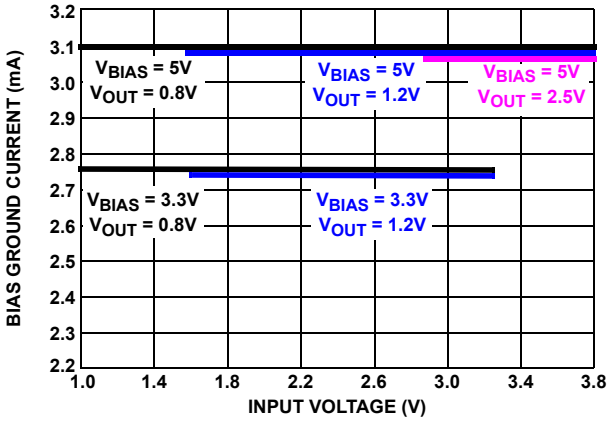


FIGURE 16. BIAS GROUND CURRENT vs V_{IN} and V_{OUT}

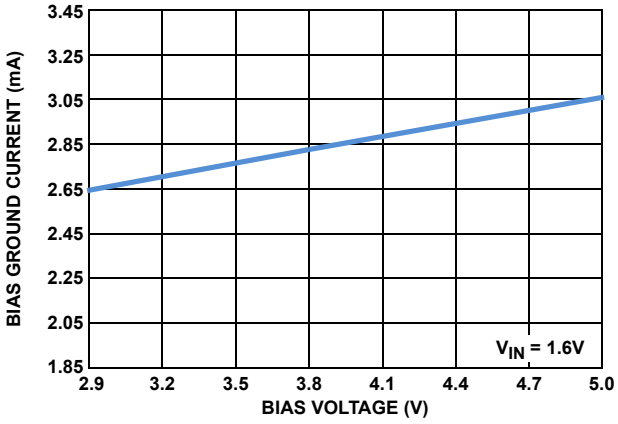


FIGURE 17. BIAS GROUND CURRENT vs V_{BIAS}

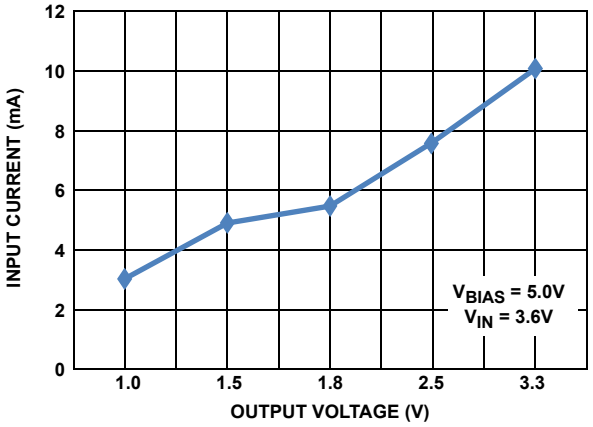


FIGURE 18. V_{IN} I_Q vs VOUT VOLTAGE

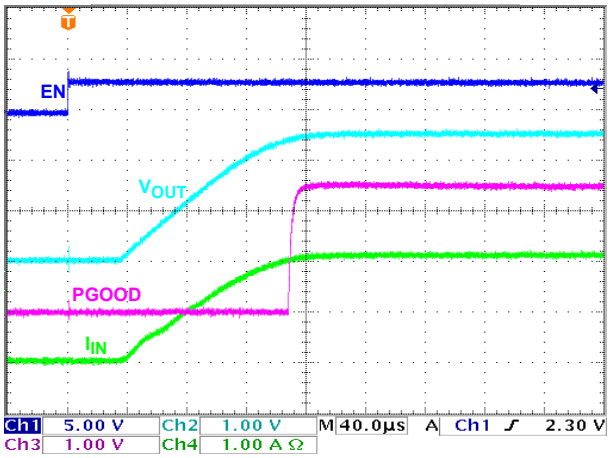


FIGURE 19. ENABLE START-UP WITH PGOOD

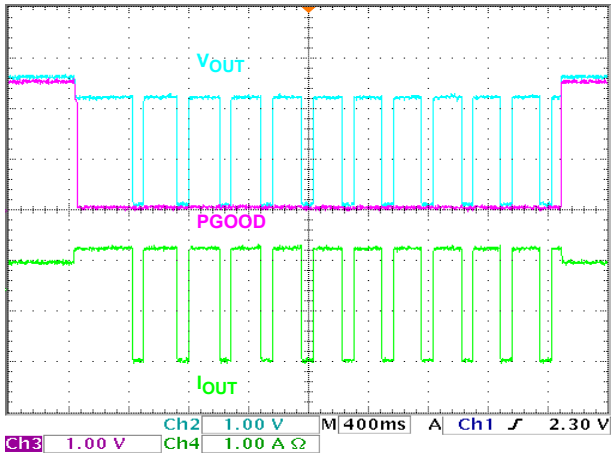


FIGURE 20. ISL8011X INTO AND OUT OF THERMAL SHUTDOWN

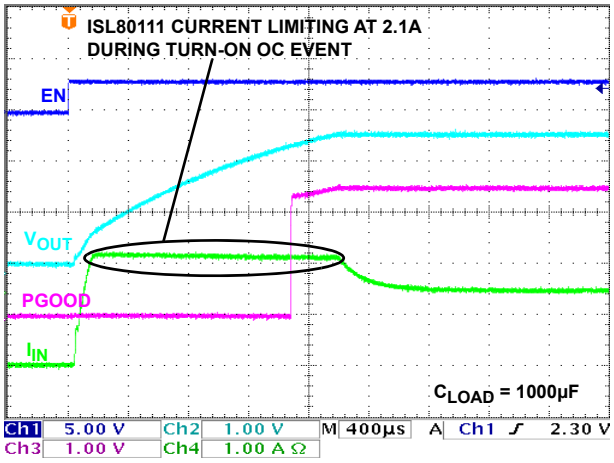


FIGURE 21. ISL80111 ENABLED INTO OVERCURRENT

Typical Operating Performance

Unless otherwise noted, V_{IN} = 1.8V, V_{BIAS} = 3.3V, V_{OUT} = 1.2V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_{LOAD} = 0A. **(Continued)**

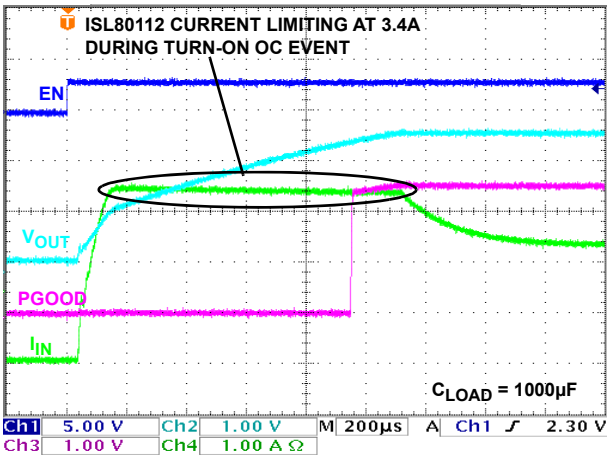


FIGURE 22. ISL80112 ENABLED INTO OVERCURRENT

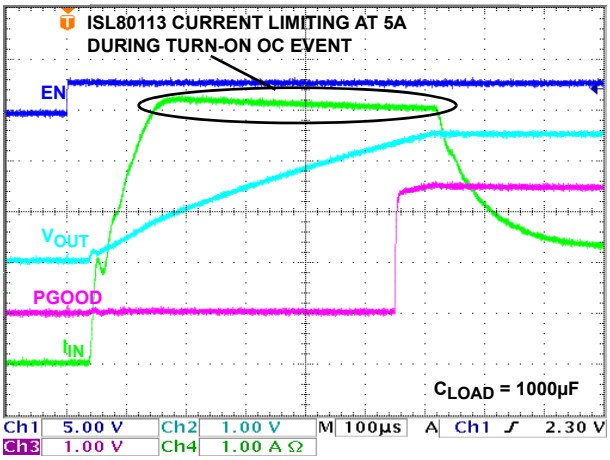


FIGURE 23. ISL80113 ENABLED INTO OVERCURRENT

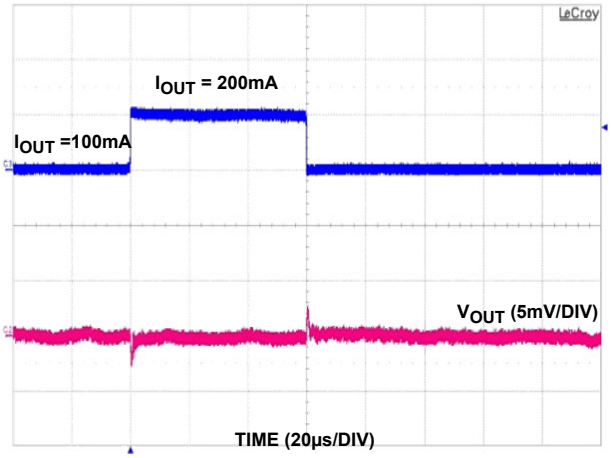


FIGURE 24. 100mA LOAD TRANSIENT RESPONSE

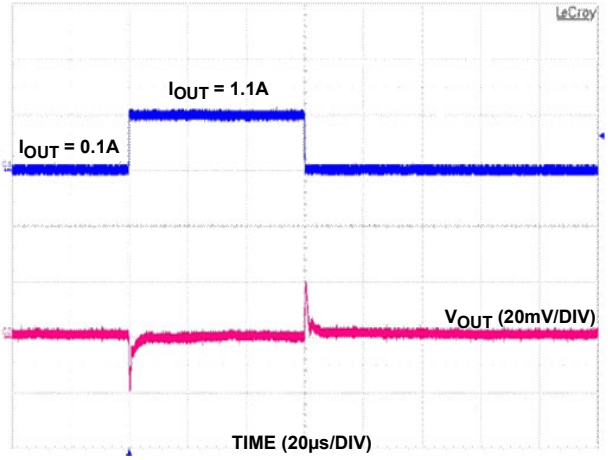


FIGURE 25. 1A LOAD TRANSIENT RESPONSE

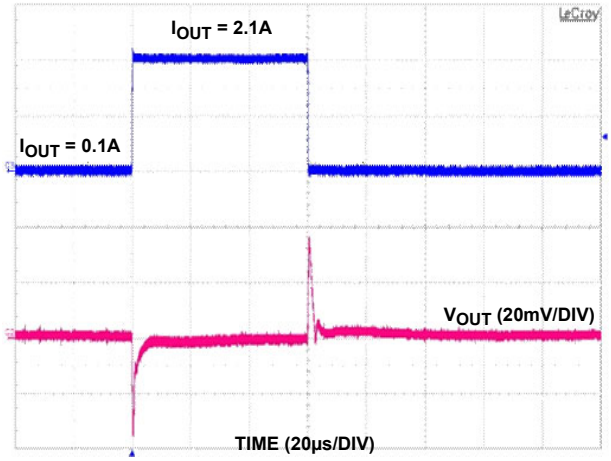


FIGURE 26. 2A LOAD TRANSIENT RESPONSE

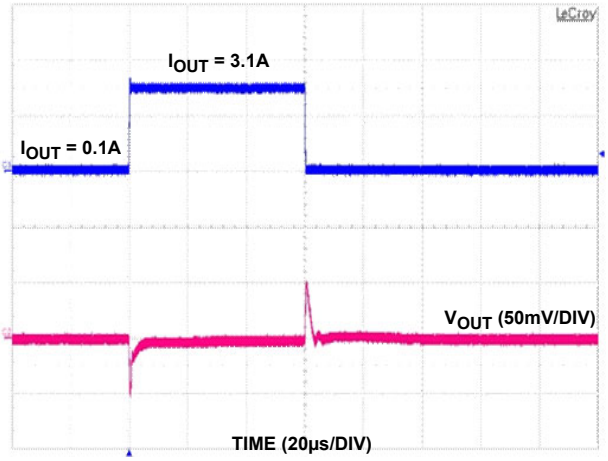


FIGURE 27. 3A LOAD TRANSIENT RESPONSE

Typical Operating Performance

Unless otherwise noted, V_{IN} = 1.8V, V_{BIAS} = 3.3V, V_{OUT} = 1.2V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_{LOAD} = 0A. **(Continued)**

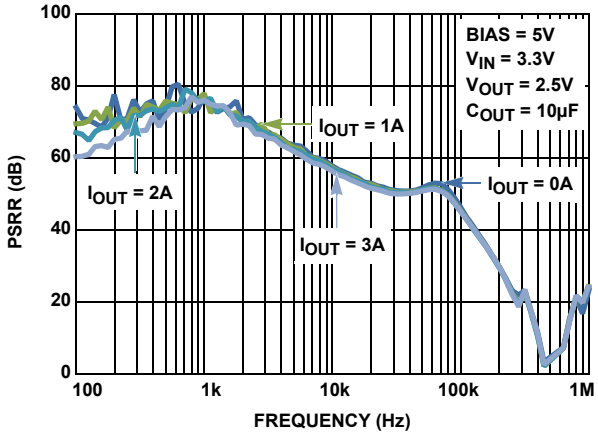


FIGURE 28. V_{IN} PSRR vs FREQUENCY FOR VARIOUS LOAD CURRENTS

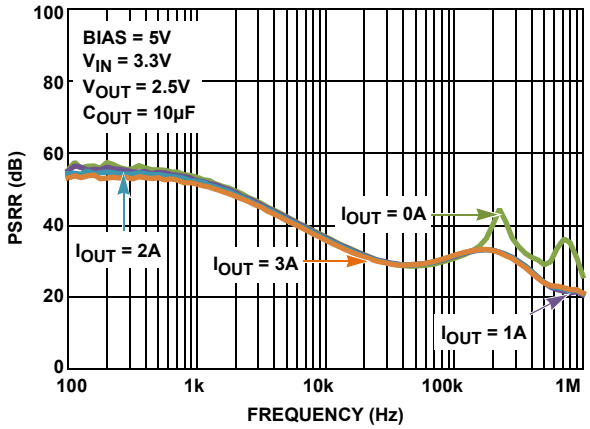


FIGURE 29. BIAS PSRR vs FREQUENCY FOR VARIOUS LOAD CURRENTS

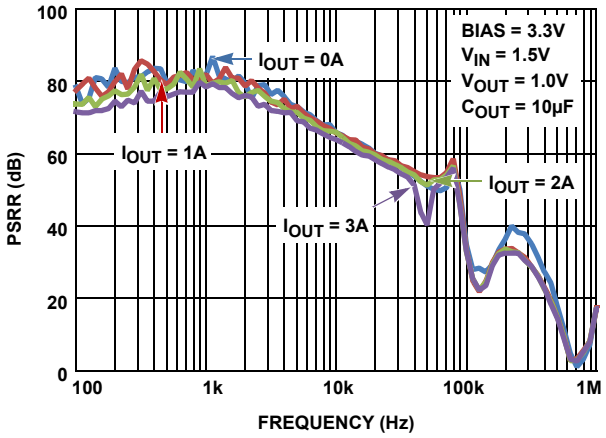


FIGURE 30. V_{IN} PSRR vs FREQUENCY FOR VARIOUS LOAD CURRENTS

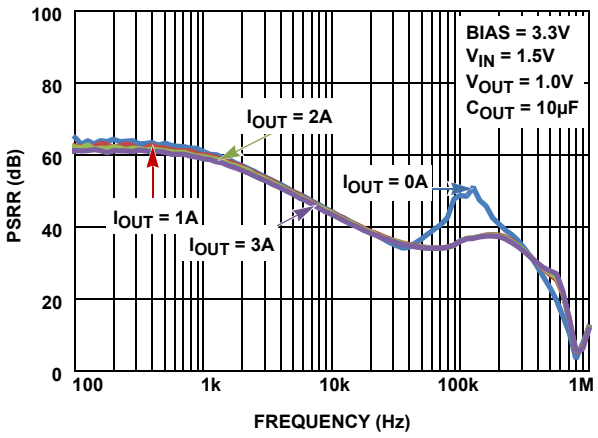


FIGURE 31. V_{BIAS} PSRR vs FREQUENCY FOR VARIOUS LOAD CURRENTS

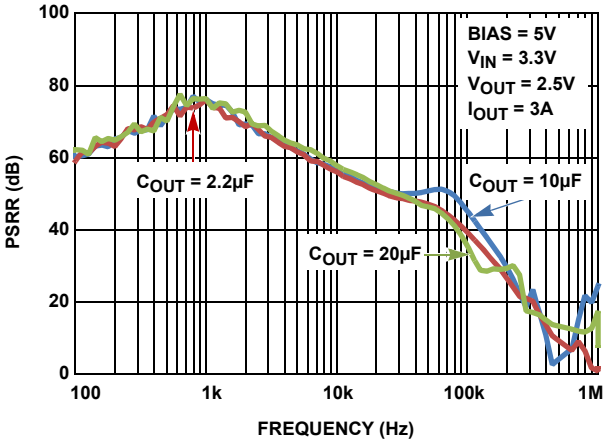


FIGURE 32. V_{IN} PSRR vs FREQUENCY FOR VARIOUS C_{OUT}

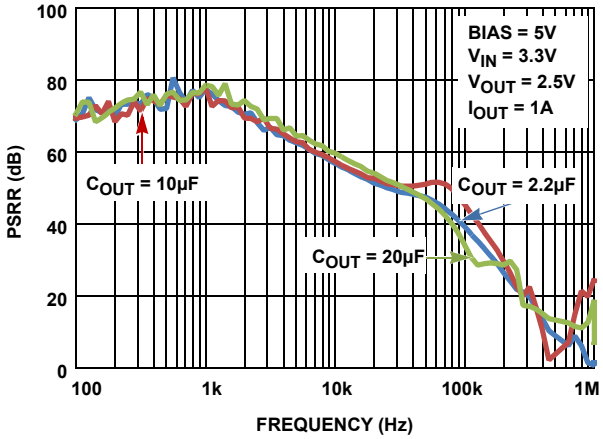


FIGURE 33. V_{IN} PSRR vs FREQUENCY FOR VARIOUS C_{OUT}

Typical Operating Performance

Unless otherwise noted, V_{IN} = 1.8V, V_{BIAS} = 3.3V, V_{OUT} = 1.2V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_{LOAD} = 0A. **(Continued)**

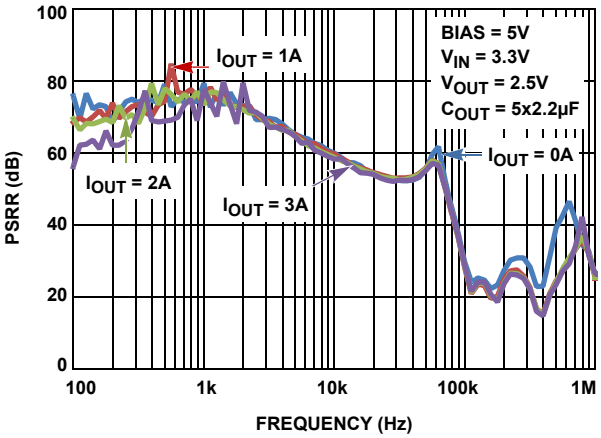


FIGURE 34. V_{IN} PSRR vs FREQUENCY FOR VARIOUS LOAD CURRENTS

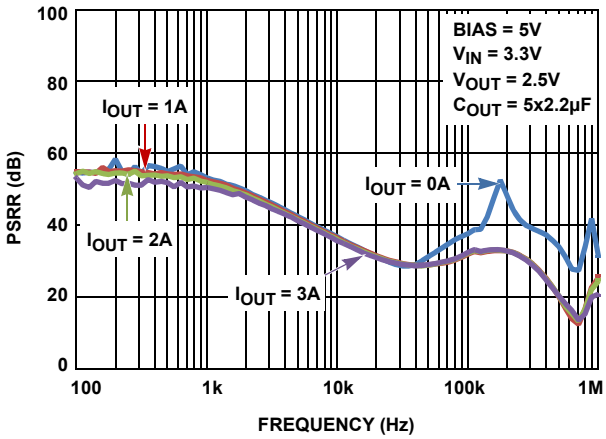


FIGURE 35. V_{BIAS} PSRR vs FREQUENCY FOR VARIOUS LOAD CURRENTS

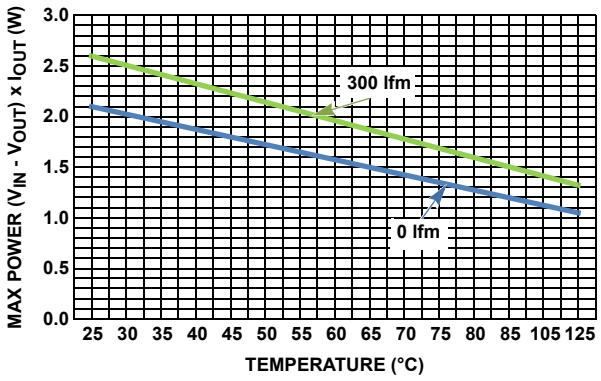


FIGURE 36. CONTINUOUS POWER LIMIT vs AIR TEMP AND FLOW

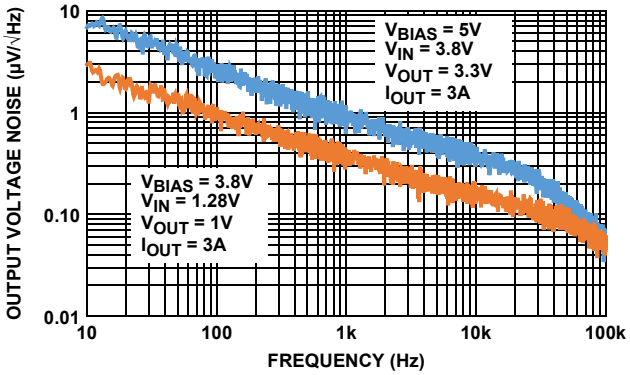


FIGURE 37. OUTPUT NOISE SPECTRAL DENSITY

Functional Description

The ISL80111, ISL80112 and ISL80113 are high-performance, low-dropout regulators featuring an NMOS pass device. Benefits of using an NMOS as a pass device include low input voltage, stability over a wide range of output capacitors and ultra low dropout voltage. The ISL80111, ISL80112 and ISL80113 are ideal for post regulation of switch mode power supplies.

The ISL80111, ISL80112 and ISL80113 also integrate enable, power-good indicator, current limit protection and thermal shutdown functions into a space-saving 3x3 DFN package.

Input Voltage Requirements

The VIN pin provides the high current to the drain of the NMOS pass transistor. The specified minimum input voltage is 0.7V and dropout voltage for this family of LDOs has been conservatively specified.

Bias Voltage Requirements

The V_{BIAS} input powers the internal control circuits, reference voltage, and LDO gate driver. The difference between the V_{BIAS} voltage and the output voltage must be greater than the V_{BIAS} dropout voltage specified in the “Electrical Specifications” table on page 5. The minimum V_{BIAS} input is 2.9V.

Enable Operation

The ENABLE turn-on threshold is typically 680mV with a hysteresis of 260mV. This pin must not be left floating. When this pin is not used, it must be tied to V_{BIAS}. A 1kΩ to 10kΩ pull-up resistor is required for applications that use open collector or open drain outputs to control the ENABLE pin.

Soft-start Operation

The ISL8011x has an internal 100µs typical soft-start function to prevent excessive in-rush current during start-up.

Power-good Operation

The PGOOD flag is an open-drain NMOS that can sink up to 10mA during a fault condition. Applications not using this feature must connect this pin to ground. The PGOOD pin requires an external pull-up resistor, which is typically connected to the V_{OUT} pin. The PGOOD pin should not be pulled up to a voltage source greater than V_{BIAS}. A PGOOD fault can be caused by the output voltage going below 84% of the nominal output voltage. PGOOD does not function during thermal shutdown as the V_{OUT} is less than the minimum regulation voltage during that time.

Output Voltage Selection

An external resistor divider is used to scale the output voltage relative to the internal reference voltage. This voltage is then fed back to the error amplifier. The output voltage can be programmed to any level between 0.5V and 3.3V. Referring to Figure 1 the external resistor divider, R_3 and R_4, is used to set the output voltage as shown in Equation 1. The recommended value for R_4 is 500Ω to 1kΩ. R_3 is then chosen according to Equation 2. See Table 2 for the recommended output capacitance at different output voltages.

$$V_{OUT} = 0.5V \times \left(\frac{R_3}{R_4} + 1\right) \quad \text{(EQ. 1)}$$

$$R_3 = R_4 \times \left(\frac{V_{OUT}}{0.5V} - 1\right) \quad \text{(EQ. 2)}$$

TABLE 2. RECOMMENDED OUTPUT CAPACITANCE AT DIFFERENT OUTPUT VOLTAGES

OUTPUT VOLTAGE	OUTPUT CAPACITANCE
<0.8V	47µF
≥0.8V	10µF

Current Limit Protection

The ISL80111, ISL80112, and ISL80113 incorporate protection against overcurrent due to a short, overload condition applied to the output and the in-rush current that occurs at start-up. The LDO performs as a constant current source when the output current exceeds the current limit threshold noted in “Electrical Specifications” on page 4. If the short or overload condition is removed from V_{OUT}, then the output returns to normal voltage mode regulation. In the event of an overload condition, the LDO might begin to cycle on and off due to the die temperature exceeding the thermal fault condition.

Thermal Fault Protection

If the die temperature exceeds (typically) +160°C, the LDO output shuts down until the die temperature cools to (typically) +140°C. The level of power, combined with the thermal impedance of the package (+48°C/W), determines whether the junction temperature exceeds the thermal shutdown temperature.

See Figure 36 for maximum continuous power dissipation guidance for ambient temperature and linear air flow rate. This graph ignores the insignificant power dissipation contribution of the BIAS pin.

External Capacitor Requirements

External capacitors are required for proper operation. To ensure optimal performance, careful attention must be paid to the layout guidelines and selection of capacitor type and value.

Input Capacitor

The minimum input capacitor required for proper operation is 10µF with a ceramic dielectric. This minimum capacitor must be connected to the V_{IN} and ground pins of the LDO no further than 0.5cm away.

Output Capacitor

The ISL8011x applies state-of-the-art internal compensation to simplify selection of the output capacitor. Stable operation over the full temperature range, V_{IN} range, V_{OUT} range, and load extremes is guaranteed for all capacitor types and values, assuming a 1µF X5R/X7R is used for local bypass on V_{OUT}. This minimum capacitor must be connected to the V_{OUT} and ground pins of the LDO no further than 0.5cm away.

Lower-cost Y5V and Z5U type ceramic capacitors are acceptable, if the size of the capacitor is larger, to compensate for the significantly lower tolerance over X5R/X7R types. Additional capacitors of any value, in ceramic, POSCAP, or alum/tantalum electrolytic types, can be placed in parallel to improve PSRR at higher frequencies or load-transient AC output voltage tolerances.

Bias Capacitor

The minimum input capacitor required for proper operation is 1µF with a ceramic dielectric. This minimum capacitor must be connected to the V_{BIAS} and ground pins of the LDO no further than 0.5cm away. When the VBIAS pin is connected to the V_{IN} pin, a total of 10µF of X5R/X7R connected to the V_{IN} pin and ground is sufficient.

Power Dissipation and Thermals

Power Dissipation

Junction temperature must not exceed the range specified in the "Recommended Operating Conditions" section on page 4. Power dissipation can be calculated with Equation 3.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{BIAS} \times IQ(BIAS) + V_{IN} \times IQ(V_{IN}) \quad \text{(EQ. 3)}$$

The maximum allowable junction temperature, $T_{J(MAX)}$, and the maximum expected ambient temperature, $T_{A(MAX)}$, determine the maximum allowable power dissipation, as shown in Equation 4, where θ_{JA} is the junction-to-ambient thermal resistance.

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA} \quad \text{(EQ. 4)}$$

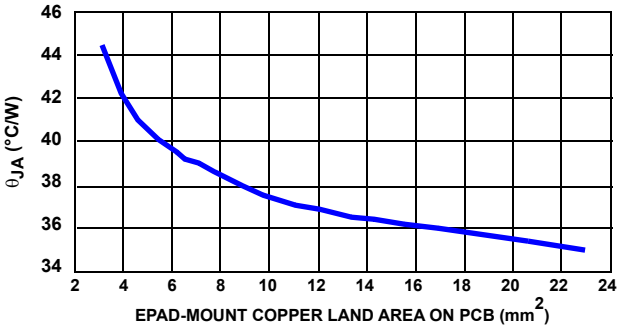


FIGURE 38. 3mmx3mm-10 PIN DFN ON 4-LAYER PCB WITH THERMAL VIAS θ_{JA} vs EPAD-MOUNT COPPER LAND AREA ON PCB

For safe operation, ensure that power dissipation calculated in Equation 3 (P_D) is less than the maximum allowable power dissipation, $P_{D(MAX)}$.

The DFN package uses the copper area on the PCB as a heat sink. For heat sinking, the EPAD of this package must be soldered to the copper plane (GND plane). Figure 38 shows a curve for the θ_{JA} of the DFN package for different copper area sizes.

General PowerPAD Design Considerations

The following is an example of how to use vias to remove heat from the IC.

Filling the thermal pad area with vias is recommended. A typical via array is to fill the thermal pad footprint with vias spaced such that they are center on center 3x the radius apart from each other. Keep the vias small but not so small that their inside diameter prevents solder from wicking through the holes during reflow.

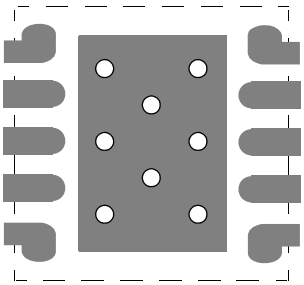


FIGURE 39. PCB VIA PATTERN

Connect all vias to the round plane. For efficient heat transfer, it is important that the vias have low thermal resistance. Do not use "thermal relief" patterns to connect the vias. It is important to have a complete connection of the plated through-hole to each plane.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
Jun 12, 2020	4.01	Added Theta JB information.
Mar 6, 2020	4.00	Updated the V_{IN} (minimum value changed from 1V to 0.7V) and V_{OUT} (minimum value changed from 0.8V to 0.5V) ranges throughout. Updated links throughout. Updated Related Literature section. Updated Ordering information table and notes. Removed Note 8 on page 4. Updated Output Voltage Selection section. Removed About Intersil section. Updated disclaimer.
Aug 30, 2016	3.00	-Updated text in Description Section page 1 from “3.3V to 5V” to “2.9V to 5.5V”. -Added Related Literature section on page 1. -Updated Figures 4 and 8. -Updated the Bock Diagram on page 2. -Updated the ADJ and Enable “Pin Descriptions” on page 2. -Updated Ordering Information table on page 3. -Added Table 1 on page 3. **On page 4:** -Updated VIN Relative to GND in the “Absolute Maximum Ratings” section. -Updated VIN Relative to GND in the “Recommended Operating Conditions” section. -Updated Note 9. -Removed Note 6 “Electromigration note”. **Electrical Specifications:** -Updated Heading -Updated the test conditions, min/max, and typical specifications for “DC Input Line Regulation”, “DC Bias –Line Regulation” and “DC Output Load Regulation” -Added “VIN = 3.6V, VBIAS = 5V” to the VIN quiescent current test conditions. **On Page 5** -Added “VIN = 1.4V, VBIAS = 3.3V” to the VIN quiescent current test conditions. -Updated test conditions for “VBIAS Quiescent Current”, “VIN Dropout Voltage”, “VBIAS Dropout Voltage”, “Turn-on Threshold (Rising)”, “PG Flag Falling Threshold”, “PG Flag Hysteresis”, and “PG Flag Leakage Current” -Updated test conditions and typical specs for “Output Noise Voltage”, “Spectral Noise Density. **Other Edits** -Updated Note 12 on page 6. -Updated Titles for Figures 5 and 27 through 34. -Updated Figure 18. -Corrected labels on Figure 17. -Replaced Figures 16 and 36. -Updated “Enable Operation” on page 12. -Updated “Output Voltage Selection” on page 12. -Removed the Evaluation Board User Guide section from datasheet. -Updated the About Intersil Verbiage. -Updated “Package Outline Drawing” on page 16 to the latest revision: -Added missing dimension 0.415 in Typical Recommended land pattern. -Shortened the e-pad rectangle on both the recommended land pattern and the package bottom view to line up with the centers of the corner pins. -Tiebar Note 4 updated From: Tiebar shown (if present) is a non-functional feature. To: Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends). **Note: Detailed changes available upon request.**

Revision History

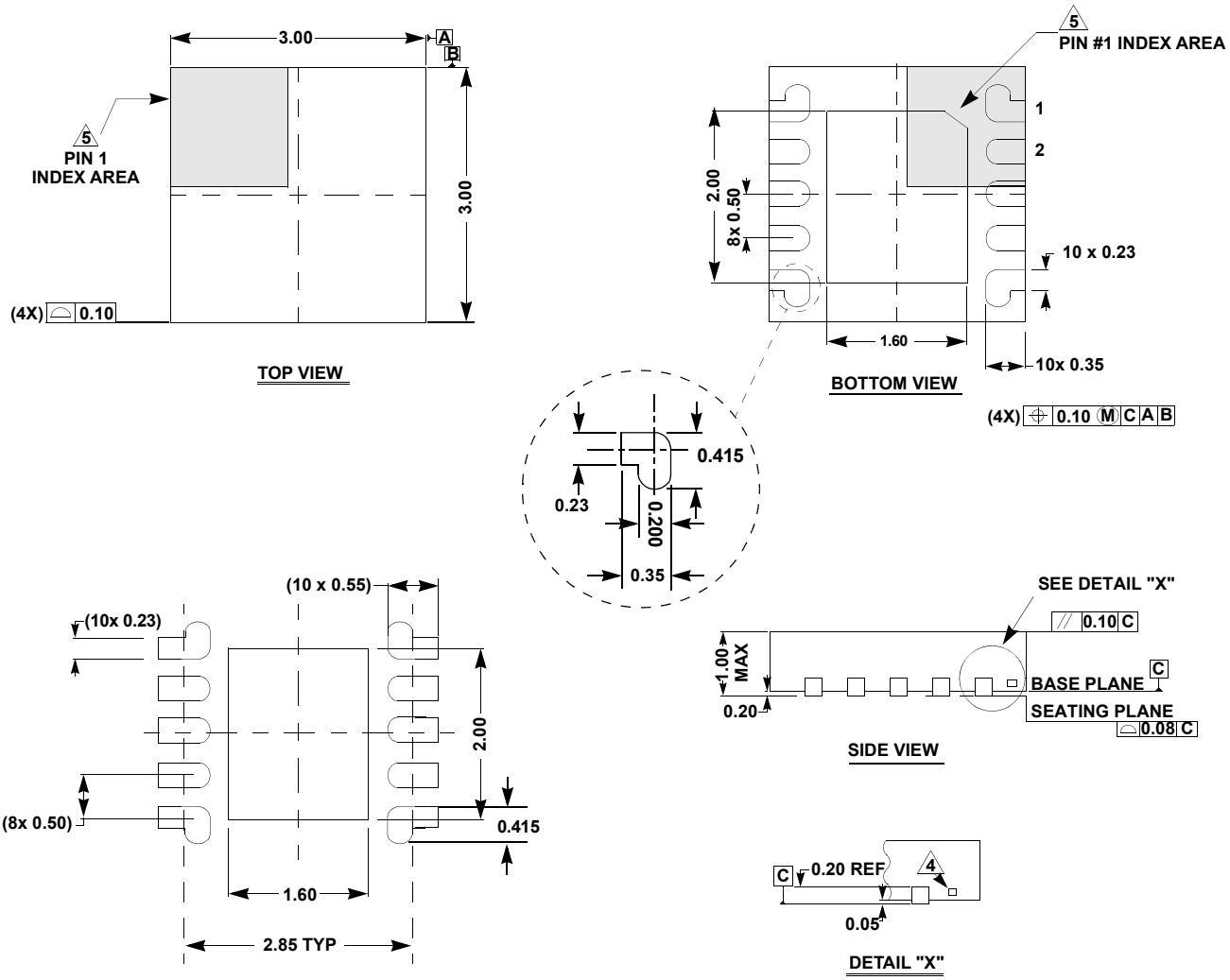
The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev. **(Continued)**

DATE	REVISION	CHANGE
Nov 1, 2013	2.00	Electrical Spec table: Bold the Min and Max values. page 4- Electrical Spec table title area: Removed “Unless otherwise noted, all parameters are guaranteed over the conditions specified as follows” and replaced by “Unless otherwise specified”. Updated POD to latest revision from rev 7 to rev 8. The changes as follow: Corrected L-shaped leads in Bottom view and land pattern so that they align with the rest of the leads (L shaped leads were shorter)
Jun 5, 2012	1.00	Ordering Information table on page 3: Changed evaluation board names from: ISL80111IRAJEVALZ, ISL80112IRAJEVALZ and ISL80113IRAJEVALZ to ISL80111EVAL1Z, ISL80112EVAL1Z and ISL80113VAL1Z. Changed POD L10.3x3 on page 17 to latest revision from Rev 6 to Rev 7. Change to POD is as follows: Removed package outline and included center to center distance between lands on recommended land pattern. Removed Note 4 “Dimension b applies to the metallized terminal and is measured between 0.18mm and 0.30mm from the terminal tip.” since it is not applicable to this package. Renumbered notes accordingly. Figure 7 VADJ Distribution, corrected “Y” scale units from (0.18, 0.16, 0.14, 0.12, 0.10, 0.08, 0.06, 0.04, 0.02, and 0.00) to (18, 16,14,12,10, 8, 6, 4, 2, and 0). Electrical Specifications table on page 4 “Added UVLO rising spec to show max of 2.9V so implementation at 3.3V is not a math problem”.
Mar 30 2012	0.00	Initial Release and Added “UVLO _BIAS _r” spec on pg 4. Modified Figures 14 - 18.

Package Outline Drawing

For the most recent package outline drawing, see L10.3x3.

L10.3x3
10 Lead Dual Flat Package (DFN)
Rev 11, 3/15



NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.