XO_DPLL Monitoring for ClockMatrix FW5.2

This application note explains how to configure the XO_DPLL input to have a pseudo input monitor.

1. Introduction

The XO_DPLL input does not have any input monitors, specifically, a short-term or LOS monitor for loss of signal. This could be problematic if there is any signal integrity issue with the XO_DPLL. The ClockMatrix FW5.2, however, can detect a poor XO_DPLL signal and disqualify the input to any of the DPLLs, including the SYSDPLL.

2. GUI and Register Settings

If the XO_DPLL monitoring feature is enabled for a DPLL, then the device will monitor the phase offset between the XO_DPLL input and the feedback. While in LOCKED state, the XO_DPLL input is declared valid if the phase offset is less than the phase lock threshold (lock criteria). If the lock criteria is violated, then the DPLL will go into HOLDOVER or switch to another reference if the DPLL is configured to do so.

In the example in Figure 1, the manual reference mode is selected and the TCXO/OCXO (XO_DPLL) is selected as the input to DPLL0. The XO_DPLL reference monitoring bit must be enabled as well.
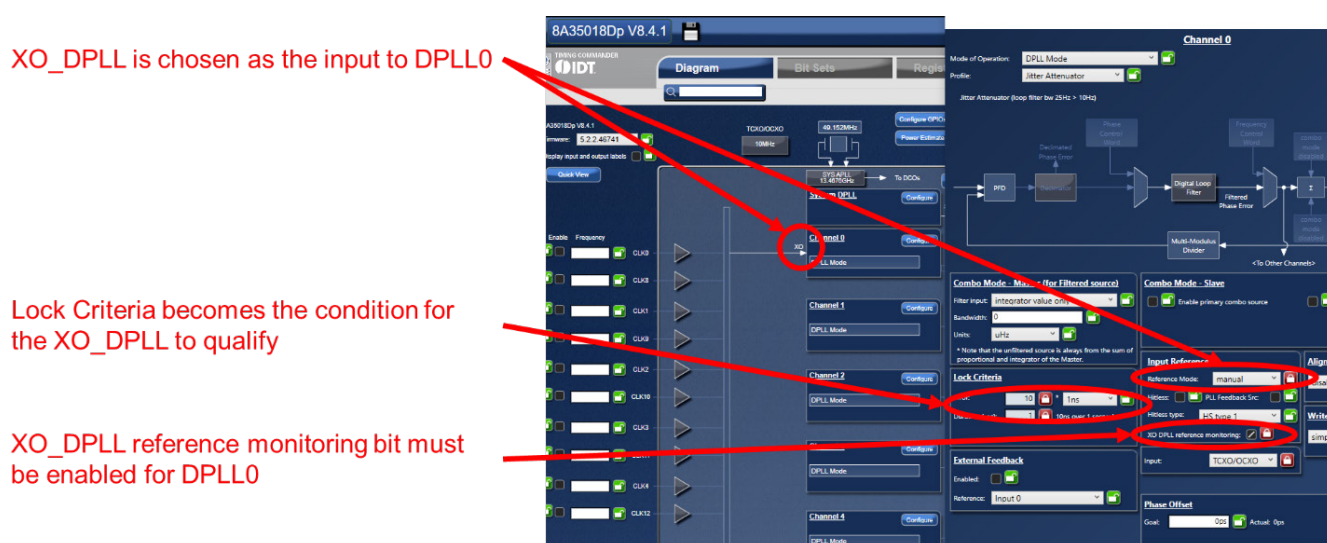

Figure 1. Configuring the GUI to Use XO_DPLL Monitoring

Each DPLL can independently enable the XO_DPLL reference monitoring bit as displayed in Figure 2. That allows any DPLL to use the XO_DPLL monitoring feature, when the XO_DPLL input is fed to a particular DPLL. The SCSR registers are named SCSR_DPLL_REF_MODE_XO_DPLL_MONITOR_ENx, where x = 0, 1, 2, 3, 4, 5, 6, or 7. Also, there is SCSR_SYS_DPLL_REF_MODE_XO_DPLL_MONITOR_EN. For more information about these bits, see the *8A3xxxx Family Programming Guide v5.2*.
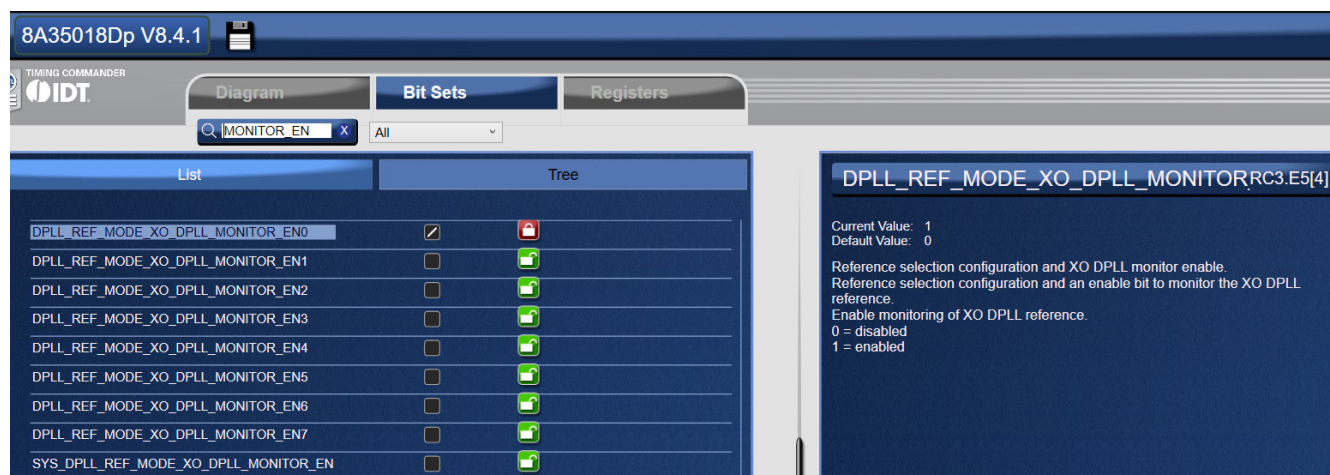
Figure 2. XO_DPLL Monitoring Registers for Each DPLL

3.   Revision History

Revision	Date	Description
1.00	Aug 20, 2021	Initial release.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.