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# **Preliminary Application Note**

# V850E/IF3, V850E/IG3

32-bit Single-Chip Microcontrollers

**Sample Programs for Timer T** 

V850E/IF3:  $\mu$ PD70F3451  $\mu$ PD70F3452 V850E/IG3:  $\mu$ PD70F3453  $\mu$ PD70F3454

Document No. U18732EJ1V0AN00 (1st edition)
Date Published August 2007 N

# [MEMO]

#### NOTES FOR CMOS DEVICES —

# 1 VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{\rm IL}$  (MAX) and  $V_{\rm IH}$  (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{\rm IL}$  (MAX) and  $V_{\rm IH}$  (MIN).

# (2) HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

#### ③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

#### (4) STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

#### ⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

# **6** INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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#### INTRODUCTION

- Cautions 1. This Application Note explains a case where the V850E/IG3 is used as a representative microcontroller. Use this Application Note for your reference when using the V850E/IF3.
  - 2. Download the program used in this manual from the page of Programming Examples (http://www.necel.com/micro/en/designsupports/sampleprogram/index.html) in the NEC Electronics Website (http://www.necel.com/).
  - 3. This sample program is provided for reference purposes only and operations are therefore not subject to guarantee by NEC Electronics Corporation. When using sample programs, customers are advised to sufficiently evaluate this product based on their systems, before use.
  - 4. When using sample programs, reference the following startup routine and link directive file and adjust them if necessary.

Startup routine: ig3\_start.sLink directive file: ig3\_link.dir

# Target Readers This Application Note is intended for users who understand the functions of the

V850E/IF3 ( $\mu$ PD70F3451, 70F3452), and V850E/IG3 ( $\mu$ PD70F3453, 70F3454), and

who design application systems that use these microcontrollers.

# Purpose This manual is intended to give users an understanding of the basic functions of the

V850E/IF3 and V850E/IG3, using the application programs.

# How to Use This Manual It is assumed that the reader of this Application Note has general knowledge in the

fields of electrical engineering, logic circuits, and microcontrollers.

For details of hardware functions (especially register functions, setting methods, etc.) and electrical specifications

→ See the V850E/IF3, V850E/IG3 Hardware User's Manual.

For details of instruction functions

→ See the **V850E1 Architecture User's Manual**.

**Conventions** Data significance: Higher digits on the left and lower digits on the right

Active low representation:  $\overline{xxx}$  (overscore over pin or signal name)

Memory map address: Higher addresses on the top and lower addresses on

the bottom

**Note:** Footnote for item marked with **Note** in the text

Caution: Information requiring particular attention

**Remark:** Supplementary information Numeric representation: Binary ... xxxx or xxxxB

Decimal ... xxxx

Hexadecimal ... xxxxH

Prefix indicating the power

of 2 (address space,

memory capacity): K (kilo):  $2^{10} = 1,024$ 

M (mega):  $2^{20} = 1,024^2$ 

G (giga):  $2^{30} = 1,024^3$ 

The function lists are structured as follows.

# Hardware name (symbol)

[Function] Function description [Function name] Name of sample function

[Argument(s)] Type and overview of argument(s)
[Processing content] Processing content of sample function
[SFR(s) used] Register name and setting content
[call function(s)] Name and function of call function(s)

[Variable(s)] Type, name, and overview of variable(s) used in sample function

[Interrupt(s)] Name of function

[Interrupt source(s)] Name

[File name] Name of corresponding sample program file

[Caution(s)] Caution(s) upon function usage

# Interrupt function

[Function name] Name of interrupt function

[Overview] Servicing content

[Source(s)] Name of interrupt and conditions for occurrence

[call function(s)] None

[Variable(s)] Name of variable, function

[File name] Name of corresponding sample program file

# **Product Differences**

The differences between the V850E/IG3 and the V850E/IF3 related to the 16-bit timer/event counter T (TMT) are shown below.

	Item	V850E/IG3	V850E/IF3
TIT00, TIT01, TOT00, TOT01, TENC00, TENC01, EVTT0, TECR0 pins		Provided	None
TMT0	External event count mode	Provided	None
	External trigger pulse output mode	Provided	None
	One-shot pulse output mode	Provided	None
	PWM output mode	Provided	None
	Free-running timer mode	Provided	Provided (compare function only)
	Triangular-wave PWM output mode	Provided	None
	Encoder compare mode	Provided	None

# **Related Documents**

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

# Documents related to V850E/IF3 and V850E/IG3

Document Name	Document No.
V850E1 Architecture User's Manual	U14559E
V850E/IF3, V850E/IG3 Hardware User's Manual	U18279E
V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (UARTA) Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (UARTB) Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (CSIB) Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (I <sup>2</sup> C) Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for DMA Function Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Timer M Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Watchdog Timer Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Timer AA Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Timer AB Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Timer T Application Note	This manual
V850E/IF3, V850E/IG3 Sample Programs for Port Function Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Clock Generator Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Standby Function Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Interrupt Function Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for A/D Converters 0 and 1 Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for A/D Converter 2 Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Low-Voltage Detector (LVI) Function Application Note	To be prepared
V850E/IF3, V850E/IG3 6-Phase PWM Output Control by Timer AB, Timer Q Option, Timer AA, A/D Converters 0 and 1 Application Note	U18717E

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# **CHAPTER 1 INTERVAL TIMER MODE**

[Function] Starts 16-bit counter operation by setting the TT0CTL0.TT0CE bit to 1.

Outputs an interrupt request signal (INTTTEQC00) at an interval set by the TT0CCR0

register.

Inverts the TOT00 pin output when the value set by the CCR0 buffer register and the

count value of the 16-bit counter match.

Can be implemented with TMT0 and TMT1.

[Function name] main

[Argument] None

[Processing content] Performs count operation of an fxx/64 count clock, generates an interrupt upon the count

(1 ms) subsequent to the count whose value matches the value of the TT0CCR0 register

(499), and clears 16-bit counter.

[SFR used] None

[call function] timermt\_interval\_ini, timermt\_interval\_st

[Variable] None

[Interrupt] timermt\_TT0CCR0\_int

[Interrupt source] INTTTEQC00

[File name] timermt\_interval\MAIN.C

[Caution] None

The interval time can be calculated by the following formula.

Interval = (Set value of TT0CCR0 register + 1) × Count clock cycle

#### **CHAPTER 1 INTERVAL TIMER MODE**

[Function name] timermt\_interval\_ini

[Argument] None

[Processing content] Sets the TMT0 operation and interrupts .

[SFRs used] TT0CTL0.TT0CE: 0 (Disables TMT0 operation.)

IMR2.TT0CCMK0: 0 (Enables INTTTEQC00 interrupt.)IMR2.TT0CCMK1: 1 (Disables INTTTEQC01 interrupt.)

[call function] timermt\_interval

[Variable] None

[File name] timermt\_interval\timermt\_1.c

[Caution] None

[Function name] timermt\_interval

[Argument] None

[Processing content] Sets TMT0 control register.

[SFRs used] TT0CTL0: 0x04 (Sets count clock to fxx/64.)

TT0CTL1: 0x00 (Sets interval timer mode.)

TT0CCR0: 499 (Compare register of 16-bit counter)
TT0CCR1: 0xFFFF (Compare register of 16-bit counter)

[call function] None
[Variable] None

[File name] timermt\_interval\timermt\_1.c

[Caution] When the TT0CCR1 register is not used, it is recommended to set the TT0CCR1 register to

FFFFH. Mask with the interrupt mask flag (IMR2.TT0CCMK1).

[Function name] timermt\_interval\_st

[Argument] None

[Processing content] Starting function of timermt\_interval.

[Starting method] Call this function after the timermt\_interval function.

[SFR used] TT0CTL0.TT0CE: 1 (Enables TMT0 operation.)

[call function] None
[Variable] None

[File name] timermt\_interval\timermt\_1.c

[Caution] None

# Interrupt function

[Function name] timermt\_TT0CCR0\_int

[Overview] Defined by the user.

[Source] INTTTEQC00 Match between the count value of the 16-bit counter and the value

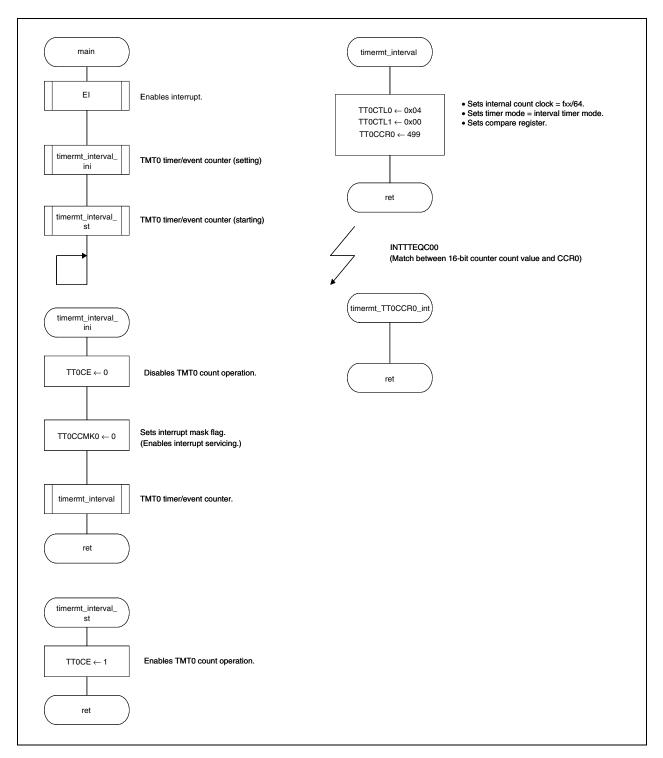
of the CCR0 buffer register

[call function] None

[Variable] None

[File name] timermt\_interval\timermt\_1.c

Figure 1-1. Interval Timer Mode



# **CHAPTER 2 EXTERNAL EVENT COUNT MODE**

[Function] Counts the valid edge of the external event count input (EVTT0 pin) and generates an

interrupt request signal (INTTTEQC00) each time the count value set by the TT0CCR0

register is counted. (Clears the 16-bit counter simultaneously.)

Can be implemented with TMT0 and TMT1.

[Function name] main

[Argument] None

[Processing content] Counts the valid edge of the external event count input, generates an interrupt upon the

count subsequent to the count whose value matches the value of the CCR0 buffer register,

and clears the 16-bit counter.

[SFR used] None

[call function] timermt\_event\_count\_ini, timermt\_event\_count\_st

[Variable] None

[Interrupt] timermt\_TT0CCR0\_int

timermt\_TT0CCR1\_int

[Interrupt source] INTTTEQC00

INTTTEQC01

[File name] timermt\_event\_count\MAIN.C

#### **CHAPTER 2 EXTERNAL EVENT COUNT MODE**

[Function name] timermt\_event\_count\_ini

[Argument] None

[Processing content] Sets the TMT0 operation and interrupts, and sets the alternate function of the P05 pin to

the EVTT0 input pin.

[SFRs used] TT0CTL0.TT0CE: 0 (Disables TMT0 operation.)

PFC0: 0x20 (Sets EVTT0 input pin.)
PFCE0: 0x00 (Sets EVTT0 input pin.)
PMC0: 0x20 (Sets EVTT0 input pin.)
IMR2.TT0CCMK0: 0 (Enables INTTTEQC00 interrupt.)
IMR2.TT0CCMK1: 1 (Disables INTTTEQC01 interrupt.)

[call function] timermt\_event\_count

[Variable] None

[File name] timermt\_event\_count\timermt\_2.c

[Caution] None

[Function name] timermt\_event\_count

[Argument] None

[Processing content] Sets TMT0 control register.

[SFRs used] TT0CTL0.TT0CE: 0 (Disables TMT0 operation.)

TT0CTL1: 0x21 (Sets external event count mode.)

TT0IOC2: 0x08 (Sets valid edge of the external event count input signal (EVTT0

pin) to falling edge detection.)

TT0CCR0: 40 (Compare register of 16-bit counter)
TT0CCR1: 0xFFFF (Compare register of 16-bit counter)

[call function] None

[Variable] None

[File name] timermt\_event\_count\timermt\_2.c

[Caution] When the TT0CCR1 register is not used, it is recommended to set the TT0CCR1 register

to FFFFH. Mask with the interrupt mask flag (IMR2.TT0CCMK1).

[Function name] timermt\_event\_count\_st

[Argument] None

[Processing content] Starting function of timermt\_event\_count.

[Starting method] Call this function after calling the timermt\_event\_count function.

[SFR used] TT0CTL0.TT0CE: 1 (Enables TMT0 operation.)

[call function] None
[Variable] None

[File name] timermt\_event\_count\timermt\_2.c

[Caution] None

# Interrupt function

[Function name] timermt\_TT0CCR0\_int

[Overview] Defined by the user.

[Source] INTTTEQC00 Match between the count value of the 16-bit counter and the value of the

CCR0 buffer register

[call function] None

[Variable] None

[File name] timermt\_event\_count\timermt\_2.c

[Caution] None

[Function name] timermt\_TT0CCR1\_int

[Overview] Defined by the user.

[Source] INTTTEQC01 Match between the count value of the 16-bit counter and the value of the

CCR1 buffer register

[call function] None

[Variable] None

[File name] timermt\_event\_count\timermt\_2.c

timermt\_event\_count main ΕI Enables interrupt. Disables TMT0 operation.  $\begin{array}{l} \mathsf{TT0CTL0} \leftarrow \mathsf{0x00} \\ \mathsf{TT0CTL1} \leftarrow \mathsf{0x21} \\ \mathsf{TT0IOC2} \leftarrow \mathsf{0x08} \\ \mathsf{TT0CCR0} \leftarrow \mathsf{40} \\ \mathsf{TT0CCR0} \leftarrow \mathsf{0xFFFF} \end{array}$ • Enables external event count input.  $\bullet$  Sets timer mode = external event count mode. • External event count input falling edge detection Sets compare register. timermt\_event TMT0 timer/event counter (setting) \_count\_ini timermt event TMT0 timer/event counter (starting) \_count\_st INTTTEQC00 (Match between 16-bit counter count value and CCR0) timermt\_TT0CCR0\_int timermt\_event \_count\_ini  $\mathsf{TT0CE} \leftarrow \mathsf{0}$ Disables TMT0 count operation. ret PFC0 ← 0x20 PFCE0 ← 0x00 Sets alternate-function pins. INTTTEQC01 PMC0 ← 0x20 (Match between 16-bit counter count value and CCR1) timermt\_TT0CCR1\_int  $\begin{array}{l} TT0CCMK0 \leftarrow 0 \\ TT0CCMK1 \leftarrow 1 \end{array}$ Sets interrupt mask flag. timermt\_event ret TMT0 timer/event counter \_count ret timermt\_event count st TT0CE ← 1 Enables TMT0 count operation. ret

Figure 2-1. External Event Count Mode

# **CHAPTER 3 EXTERNAL TRIGGER PULSE OUTPUT MODE**

[Function] Starts operation of the 16-bit counter when the valid edge of the external trigger input

(EVTT0 pin) is detected.

Clears the 16-bit counter upon a match between the CCR0 buffer register value and the 16-

bit counter value.

Inverts the TOT01 pin output upon a match between the CCR1 buffer register value and

the 16-bit counter value.

Inverts the TOT01 pin when the 16-bit counter is cleared.

Can be implemented with TMT0 and TMT1.

[Function name] main

[Argument] None

[Processing content] Starts count operation of an fxx/16 count clock when the valid edge of the external trigger

input is detected, generates an interrupt upon the count subsequent to the count whose

value matches the value of the CCR0 buffer register, and clears the 16-bit counter.

Generates an interrupt by inverting the TOT01 pin output upon a match between the CCR1

buffer register value and the 16-bit counter value.

TOT01 pin starts output at high level.

[SFR used] None

[call function] timermt\_trigger\_pulse\_ini, timermt\_trigger\_pulse\_st

[Variable] None

[Interrupt] timermt\_TT0CCR0\_int

timermt\_TT0CCR1\_int

[Interrupt source] INTTTEQC00

INTTTEQC01

[File name] timermt\_trigger\_pulse\MAIN.C

[Caution] None

The active level width, cycle and duty factor of the PWM waveform can be calculated by the following formula.

Active level width = (Set value of TT0CCR1 register)  $\times$  Count clock cycle

Cycle = (Set value of TT0CCR0 register + 1)  $\times$  Count clock cycle

Duty factor = (Set value of TT0CCR1 register)/(Set value of TT0CCR0 register + 1)

#### CHAPTER 3 EXTERNAL TRIGGER PULSE OUTPUT MODE

[Function name] timermt\_trigger\_pulse\_ini

[Argument] None

[Processing content] Sets the TMT0 operation and interrupts, sets the alternate function of the P05 pin to

EVTT0 input pin, and sets alternate function of the P06 pin to TOT01 output.

[SFRs used] TT0CTL0.TT0CE: 0 (Disables TMT0 operation.)

PFC0: 0x60 (Sets EVTT0 input pin, TOT01 output pin.)
PFCE0: 0x00 (Sets EVTT0 input pin, TOT01 output pin.)
PMC0: 0x60 (Sets EVTT0 input pin, TOT01 output pin.)

IMR2.TT0CCMK0: 0 (Enables INTTTEQC00 interrupt.)
IMR2.TT0CCMK1: 0 (Enables INTTTEQC01 interrupt.)

[call function] timermt\_trigger\_pulse

[Variable] None

[File name] timermt\_trigger\_pulse\timermt\_3.c

[Caution] None

[Function name] timermt\_trigger\_pulse

[Argument] None

[Processing content] Sets TMT0 control register.

[SFRs used] TT0CTL0: 0x03 (Sets count clock to fxx/16.)

TT0CTL1: 0x02 (Sets external trigger pulse output mode.)

TT0IOC0: 0x04 (Sets TOT00 pin output to high-level start, disables timer output,

sets TOT01 pin output to high-level start, enables timer output.)

TT0IOC2: 0x02 (Sets valid edge of the external trigger input signal (EVTT0 pin) to

falling edge detection.)

TT0CCR0: 2499 (Compare register of 16-bit counter)
TT0CCR1: 1249 (Compare register of 16-bit counter)

[call function] None
[Variable] None

[File name] timermt\_trigger\_pulse\timermt\_3.c

[Caution] The compare registers are rewritten in the batch write mode.

To rewrite the compare register during timer operation, rewrite the TT0CCR1 register last.

[Function name] timermt\_trigger\_pulse\_st

[Argument] None

[Processing content] Starting function of timermt\_trigger\_pulse

[Starting method] Call this function after calling the timermt\_trigger\_pulse function.

[SFR used] TT0CTL0.TT0CE: 1 (Enables TMT0 operation.)

[call function] None
[Variable] None

[File name] timermt\_trigger\_pulse\timermt\_3.c

[Caution] None

# Interrupt function

[Function name] timermt\_TT0CCR0\_int

[Overview] Defined by the user.

[Source] INTTTEQC00 Match between the count value of the 16-bit counter and CCR0 buffer

register

[call function] None

[Variable] None

[File name] timermt\_trigger\_pulse\timermt\_3.c

[Caution] None

[Function name] timermt\_TT0CCR1\_int

[Overview] Defined by the user.

[Source] INTTTEQC01 Match between the count value of the 16-bit counter and CCR1 buffer

register

[call function] None

[Variable] None

[File name] timermt\_trigger\_pulse\timermt\_3.c

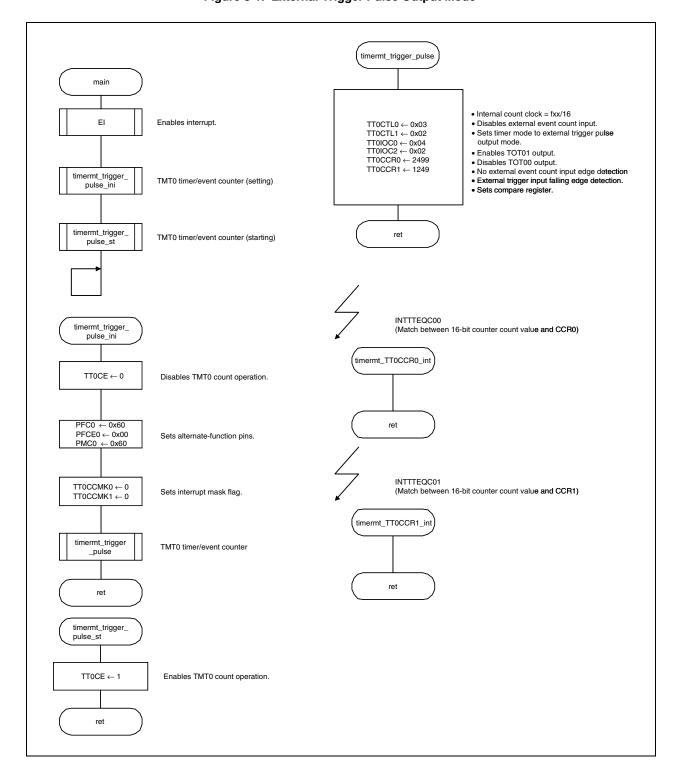


Figure 3-1. External Trigger Pulse Output Mode

# CHAPTER 4 ONE-SHOT PULSE OUTPUT MODE

[Function] Starts operation of the 16-bit counter when the valid edge of the external trigger input

(EVTT0 pin) is detected.

Clears the 16-bit counter upon a match between the CCR0 buffer register value and the

16-bit counter value, and stops count operation.

Inverts the TOT01 pin upon a match between the CCR1 buffer register value and the 16-bit

counter value.

Inverts the TOT01 pin when the 16-bit counter is cleared.

Can be implemented with TMT0 and TMT1.

[Function name] main

[Argument] None

[Processing content] Starts count operation of an fxx/16 count clock when the valid edge of the external trigger

input is detected, generates an interrupt upon the count subsequent to the count whose value matches the value of the CCR0 buffer register by inverting the TOT00 pin output, and

clears the 16-bit counter to stop the count operation.

Generates an interrupt by inverting the TOT01 pin output upon a match between the CCR1

buffer register value and the 16-bit counter value.

TOT01 pin starts output at high level.

[SFR used] None

[call function] timermt\_1shot\_pulse\_ini, timermt\_1shot\_pulse\_st

[Variable] None

[Interrupts] timermt\_TT0CCR0\_int

timermt\_TT0CCR1\_int

[Interrupt sources] INTTTEQC00

INTTTEQC01

[File name] timermt\_1shot\_pulse\MAIN.C

[Caution] None

The output delay time and active level width of one-shot pulse can be calculated by the following formula.

Output delay time = (Set value of TT0CCR1 register) × Count clock cycle

Active level width = (Set value of TT0CCR0 register - Set value of TT0CCR1 register + 1) × Count clock cycle

#### CHAPTER 4 ONE-SHOT PULSE OUTPUT MODE

[Function name] timermt\_1shot\_pulse\_ini

[Argument] None

[Processing content] Sets the TMT0 operation and interrupts, set the alternate function of the P05 pin to EVTT0

input pin, and sets alternate function of the P06 pin to TOT01 output.

[SFRs used] TT0CTL0.TT0CE: 0 (Disables TMT0 operation.)

PFC0: 0x60 (Sets EVTT0 input pin, TOT01 output pin.)
PFCE0: 0x00 (Sets EVTT0 input pin, TOT01 output pin.)
PMC0: 0x60 (Sets EVTT0 input pin, TOT01 output pin.)

IMR2.TT0CCMK0: 0 (Enables INTTTEQC00 interrupt.)
IMR2.TT0CCMK1: 0 (Enables INTTTEQC01 interrupt.)

[call function] timermt\_1shot\_pulse

[Variable] None

[File name] timermt\_1shot\_pulse\timermt\_4.c

[Caution] None

[Function name] timermt\_1shot\_pulse

[Argument] None

[Processing content] Sets TMT0 control register.

[SFRs used] TT0CTL0: 0x03 (Sets count clock to fxx/16.)

TT0CTL1: 0x03 (Sets one-shot pulse output mode.)

TT0IOC0: 0x04 (Sets TOT00 pin output to high-level start, disables timer output,

sets TOT01 pin output to high-level start, enables timer output.)

TT0IOC2: 0x02 (Sets valid edge of the external trigger input signal (EVTT0 pin)

to falling edge detection.)

TT0CCR0: 2499 (Compare register of 16-bit counter)
TT0CCR1: 1249 (Compare register of 16-bit counter)

[call function] None

[Variable] None

[File name] timermt\_1shot\_pulse\timermt\_4.c

[Function name] timermt\_1shot\_pulse\_st

[Argument] None

[Processing content] Starting function of timermt\_1shot\_pulse

[Starting method] Call this function after calling the timermt\_1shot\_pulse function.

[SFR used] TT0CTL0.TT0CE: 1 (Enables TMT0 operation.)

[call function] None
[Variable] None

[File name] timermt\_1shot\_pulse\timermt\_4.c

[Caution] None

# Interrupt function

[Function name] timermt\_TT0CCR0\_int

[Overview] Defined by the user.

[Source] INTTTEQC00 Match between the count value of the 16-bit counter and the value of

the CCR0 buffer register

[call function] None

[Variable] None

[File name] timermt\_1shot\_pulse\timermt\_4.c

[Caution] None

[Function name] timermt\_TT0CCR1\_int

[Overview] Defined by the user.

[Source] INTTTEQC01 Match between the count value of the 16-bit counter and the value of

the CCR1 buffer register

[call function] None

[Variable] None

[File name] timermt\_1shot\_pulse\timermt\_4.c

timermt\_1shot\_pulse main • Internal count clock = fxx/16 TT0CTL0 ← 0x03 TT0CTL1 ← 0x03 ΕI • Disables external event count input. Enables interrupt. • Sets timer mode to one-shot pulse output mode. TT0IOC0 ← 0x04 TT0IOC2 ← 0x02 TT0CCR0 ← 2499 TT0CCR1 ← 1249 • Enables TOT01 output. • Disables TOT00 output. No external event count input edge detection
External trigger input falling edge detection. timermt\_1shot\_ pulse\_ini TMT0 timer/event counter (setting) Sets compare register. timermt\_1shot\_ pulse\_st TMT0 timer/event counter (starting) INTTTEQC00 (Match between 16-bit counter count value and CCR0) timermt\_1shot\_pulse\_ini timermt\_TT0CCR0\_int TT0CE ← 0 Disables TMT0 count operation. PFC0 ← 0x60 PFCE0 ← 0x00 Sets alternate-function pins. PMC0  $\leftarrow$  0x60 INTTTEQC01 (Match between 16-bit counter count value and CCR1)  $\begin{array}{l} \text{TT0CCMK0} \leftarrow 0 \\ \text{TT0CCMK1} \leftarrow 0 \end{array}$ Sets interrupt mask flag. timermt\_TT0CCR1\_int timermt\_1shot\_pulse TMT0 timer/event counter ret timermt\_1shot\_pulse\_st Enables TMT0 count operation. TT0CE ← 1 ret

Figure 4-1. One-Shot Pulse Output Mode

# **CHAPTER 5 PWM OUTPUT MODE**

[Function] Starts operation of the 16-bit counter by setting the TT0CTL0.TT0CE bit to 1.

Clears the 16-bit counter upon a match with the CCR0 buffer register value, inverts the TOT00 pin output, and outputs a PWM waveform with a 50% duty factor whose half cycle

is equal to the set value of the TT0CCR0 register + 1.

Inverts the TOT01 pin upon a match between the CCR1 buffer register value and the 16-bit

counter value.

Inverts the TOT01 pin when the 16-bit counter is cleared.

Can be implemented with TMT0 and TMT1.

[Function name] main

[Argument] None

[Processing content] Performs count operation of an fxx/16 count clock, generates an interrupt by inverting the

TOT00 pin output upon the count subsequent to the count whose value matches the value

of the CCR0 buffer register, and clears the 16-bit counter.

Generates an interrupt by inverting the TOT01 pin output upon a match between the CCR1

buffer register value and the 16-bit counter value.

Both TOT00 pin and TOT01 pin start output at high level.

[SFR used] None

[call function] timermt\_pwm\_output\_ini, timermt\_pwm\_output\_st

[Variable] None

[Interrupts] timermt\_TT0CCR0\_int

timermt\_TT0CCR1\_int

[Interrupt sources] INTTTEQC00

INTTTEQC01

[File name] timermt\_pwm\_output\MAIN.C

[Caution] None

The active level width, cycle, and duty factor of the PWM waveform output from the TOT01 pin can be calculated by the following formula.

Active level width = (Set value of TT0CCR1 register) × Count clock cycle

Cycle = (Set value of TT0CCR0 register + 1) × Count clock cycle

Duty factor = (Set value of TT0CCR1 register) / (Set value of TT0CCR0 register + 1)

#### **CHAPTER 5 PWM OUTPUT MODE**

[Function name] timermt\_pwm\_output\_ini

[Argument] None

[Processing content] Sets the TMT0 operation and interrupts, sets the alternate function of the P04 pin to TOT00

output pin, and sets alternate function of the P06 pin to TOT01 output.

[SFRs used] TT0CTL0.TT0CE: 0 (Disables TMT0 operation.)

PFC0: 0x50 (Sets TOT00 output pin, TOT01 output pin.)
PFCE0: 0x00 (Sets TOT00 output pin, TOT01 output pin.)
PMC0: 0x50 (Sets TOT00 output pin, TOT01 output pin.)

IMR2.TT0CCMK0: 0 (Enables INTTTEQC00 interrupt.)
IMR2.TT0CCMK1: 0 (Enables INTTTEQC01 interrupt.)

[call function] timermt\_pwm\_output

[Variable] None

[File name] timermt\_pwm\_output\timermt\_5.c

[Caution] None

[Function name] timermt\_pwm\_output

[Argument] None

[Processing content] Sets TMT0 control register.

[SFRs used] TT0CTL0: 0x03 (Sets count clock to fxx/16.)

TT0CTL1: 0x04 (Sets PWM output mode.)

TT0IOC0: 0x05 (Sets TOT00 pin output to high-level start, enables timer output,

sets TOT01 pin output to high-level start, enables timer output.)

TT0IOC2: 0x00 (Sets valid edge of the external event count input signal (EVTT0

pin) to no edge detection.)

TT0CCR0: 2499 (Compare register of 16-bit counter)
TT0CCR1: 1999 (Compare register of 16-bit counter)

[call function] None

[Variable] None

[File name] timermt\_pwm\_output\timermt\_5.c

[Caution] The compare registers are rewritten in the batch write mode.

To rewrite the compare register during timer operation, rewrite the TT0CCR1 register last.

[Function name] timermt\_pwm\_output\_st

[Argument] None

[Processing content] Starting function of timermt\_pwm\_output

[Starting method] Call this function after calling the timermt\_pwm\_output function.

[SFR used] TT0CTL0.TT0CE: 1 (Enables TMT0 operation.)

[call function] None
[Variable] None

[File name] timermt\_pwm\_output\timermt\_5.c

[Caution] None

# Interrupt function

[Function name] timermt\_TT0CCR0\_int

[Overview] Defined by the user.

[Source] INTTTEQC00 Match between the count value of the 16-bit counter and CCR0 buffer

register

[call function] None

[Variable] None

[File name] timermt\_pwm\_output\timermt\_5.c

[Caution] None

[Function name] timermt\_TT0CCR1\_int

[Overview] Defined by the user.

[Source] INTTTEQC01 Match between the count value of the 16-bit counter and CCR1 buffer

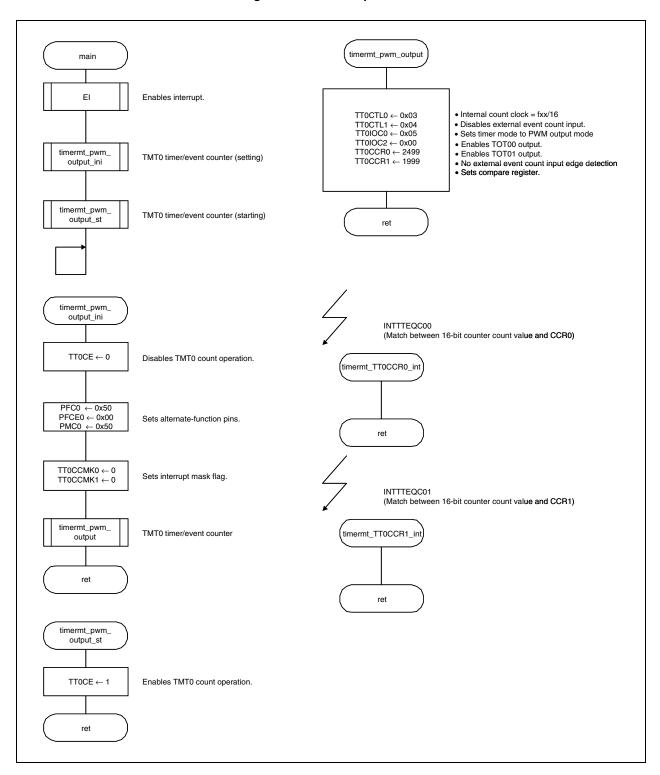
register

[call function] None

[Variable] None

[File name] timermt\_pwm\_output\timermt\_5.c

Figure 5-1. PWM Output Mode



# CHAPTER 6 FREE-RUNNING TIMER MODE

[Function] Starts operation of the 16-bit counter by setting the TT0CTL0.TT0CE bit to 1.

Inverts the TOT00 pin output upon a match between the CCR0 buffer register and the

count value of the 16-bit counter (compare function).

Stores the count value of the 16-bit counter in the TT0CCR1 register when the valid edge

of the capture trigger input (TIT01 pin) is detected (capture function).

After counting up to FFFFH, generates an overflow interrupt request signal (INTTTIOV0) at

the next clock and clears to 0000H to continue counting.

The compare function and capture function can be implemented with TMT0 and TMT1.

[Function name] main

[Argument] None

[Processing content] Performs count operation of an fxx/16 count clock, generates an interrupt by inverting the

TOT00 pin output upon the count subsequent to the count whose value matches the value

of the CCR0 buffer register, and clears the 16-bit counter.

Generates an interrupt by capturing the 16-bit counter value to the TT0CCR1 register when

a valid edge is detected from the TIP01 pin.

Generates an INTTTIOV0 interrupt when a 16-bit counter overflow is detected.

The TOT00 pin starts output at high level.

[SFR used] None

[call function] timermt\_free\_running\_ini, timermt\_free\_running\_st

[Variable] None

[Interrupts] timermt\_TT0CCR0\_int

timermt\_TT0CCR1\_int timermt\_TTTIOV0\_int

[Interrupt sources] INTTTEQC00

INTTTEQC01 INTTTIOV0

[File name] timermt\_free\_running \MAIN.C

#### CHAPTER 6 FREE-RUNNING TIMER MODE

[Function name] timermt\_free\_running\_ini

[Argument] None

[Processing content] Sets the TMT0 operation and interrupts, sets the alternate function of the P04 pin to TOT00

output pin, and sets alternate function of the P06 pin to TIT01 input.

[SFRs used] TT0CTL0.TT0CE: 0 (Disables TMT0 operation.)

PFC0: 0x10 (Sets TOT00 output pin, TIT01 input pin.)
PFCE0: 0x00 (Sets TOT00 output pin, TIT01 input pin.)
PMC0: 0x50 (Sets TOT00 output pin, TIT01 input pin.)

IMR2.TT0CCMK0: 0 (Enables INTTTEQC00 interrupt.)IMR2.TT0CCMK1: 0 (Enables INTTTEQC01 interrupt.)IMR2.TT0OVMK: 0 (Enables INTTTIOV0 interrupt.)

[call function] timermt\_free\_running

[Variable] None

[File name] timermt\_free\_running\timermt\_6.c

[Caution] None

[Function name] timermt\_free\_running

[Argument] None

[Processing content] Sets TMT0 control register.

[SFRs used] TT0CTL0: 0x03 (Sets count clock to fxx/16.)

TT0CTL1: 0x05 (Sets free-running timer mode.)

TT0IOC0: 0x01 (Sets TOT00 pin output to high-level start, enables timer output.)

TT0IOC1: 0x08 (Sets valid edge of the capture trigger input signal (TIT01 pin) to

falling edge detection.)

TT0IOC2: 0x00 (Sets valid edge of the external event count input signal (EVTT0

pin) to no edge detection.)

TT0OPT0: 0x20 (Sets TT0CCR0 as compare register, and TT0CCR1 as capture

register.)

TT0CCR0: 2499 (Compare register of 16-bit counter)

[call function] None

[Variable] None

[File name] timermt\_free\_running\timermt\_6.c

[Function name] timermt\_free\_running\_st

[Argument] None

[Processing content] Starting function of timermt\_free\_running

[Starting method] Call this function after calling the timermt\_free\_running function.

[SFR used] TT0CTL0.TT0CE: 1 (Enables TMT0 operation.)

[call function] None
[Variable] None

[File name] timermt\_free\_running\timermt\_6.c

[Caution] None

# Interrupt function

[Function name] timermt\_TT0CCR0\_int

[Overview] Defined by the user.

[Source] INTTTEQC00 Match between the count value of the 16-bit counter and the value of the

CCR0 buffer register

[call function] None

[Variable] None

[File name] timermt\_free\_running\timermt\_6.c

[Caution] None

[Function name] timermt\_TT0CCR1\_int

[Overview] Defined by the user.

[Source] INTTTEQC01 Detects valid edge of the TIT01 pin input.

[call function] None
[Variable] None

[File name] timermt\_free\_running\timermt\_6.c

# CHAPTER 6 FREE-RUNNING TIMER MODE

[Function name] timermt\_TTTIOV0\_int

[Overview] Defined by the user.

[Source] INTTTIOV0 16-bit counter overflow occurrence

[call function] None
[Variable] None

[File name] timermt\_free\_running\timermt\_6.c

main ΕI Enables interrupt. timermt\_free\_running Internal count clock = fxx/16 • Disables external event count input. timermt\_free\_ TMT0 timer/event counter (setting) Sets timer mode to free-running timer mode running\_ini  $\begin{aligned} & \mathsf{TTOCTL0} \leftarrow \mathsf{0x03} \\ & \mathsf{TTOCTL1} \leftarrow \mathsf{0x05} \\ & \mathsf{TT0IOC0} \leftarrow \mathsf{0x01} \\ & \mathsf{TT0IOC1} \leftarrow \mathsf{0x08} \\ & \mathsf{TT0IOC2} \leftarrow \mathsf{0x00} \\ & \mathsf{TT0OPT0} \leftarrow \mathsf{0x20} \\ & \mathsf{TT0CCR0} \leftarrow \mathsf{2499} \end{aligned}$  Enables TOT00 output.
 Capture trigger input (TIT01) falling edge detection • No capture trigger input (TIT00) edge detection timermt\_free\_ No external event count input edge detection TMT0 timer/event counter (starting) running\_st TT0CCR1 = capture register • TT0CCR0 = compare register • Sets compare register. TT0OVF is 1? Yes ret Clears overflow flag of 16-bit TT0OVF  $\leftarrow$  0 INTTTEQC00 (Match between 16-bit counter count value and CCR0) timermt\_free\_ running\_ini timermt\_TT0CCR0\_ TT0CE ← 0 Disables TMT0 count operation.  $\begin{array}{c} \mathsf{PFC0} \leftarrow \mathsf{0x10} \\ \mathsf{PFCE0} \leftarrow \mathsf{0x00} \\ \mathsf{PMC0} \leftarrow \mathsf{0x50} \end{array}$ ret Sets alternate-function pins.  $\begin{array}{c} \mathsf{TT0CCMK0} \leftarrow 0 \\ \mathsf{TT0CCMK1} \leftarrow 0 \\ \mathsf{TT0OVMK} \leftarrow 0 \end{array}$ INTTTEQC01 (TIT01 pin falling edge detection) Sets interrupt mask flag. timermt\_TT0CCR1\_in timermt\_free\_ TMT0 timer/event counter running ret INTTTIOV0 timermt\_free\_ (16-bit counter overflow occurrence) running\_st timermt\_TTTIOV0\_int  $\mathsf{TT0CE} \leftarrow \mathsf{1}$ Enables TMT0 count operation. ret ret

Figure 6-1. Free-Running Timer Mode

## CHAPTER 7 PULSE WIDTH MEASUREMENT MODE

[Function] Starts operation of the 16-bit counter by setting the TT0CTL0.TT0CE bit to 1.

Stores the count value of the 16-bit counter to the TT0CCR0 register when the valid edge

of the capture trigger input (TIT00 pin) is detected, and clears the 16-bit counter.

Measures the valid edge interval of the TIT00 pin by generating an interrupt when the valid

edge of the TIT00 pin input is detected and reading the TT0CCR0 register value.

Can be implemented with TMT0 and TMT1.

[Function name] main
[Argument] None

[Processing content] Performs count operation of an fxx/16 count clock, generates an interrupt by storing the

count value of the 16-bit counter to the TT0CCR0 register when the valid edge of the TIT00

pin input is detected, and clears the 16-bit counter.

Generates an INTTTIOV0 interrupt when a 16-bit counter overflow is detected.

[SFR used] None

[call function] timermt\_pulse\_measure\_ini, timermt\_pulse\_measure\_st

[Variable] None

[Interrupt] timermt\_TT0CCR0\_int

timermt\_TTTIOV0\_int

[Interrupt source] INTTTEQC00

**INTTTIOV0** 

[File name] timermt\_pulse\_measure\MAIN.C

[Caution] None

The pulse width can be calculated by the following formula.

Pulse width = Captured value × Count clock cycle

The pulse width when the 16-bit counter overflow is detected can be calculated by the following formula.

Pulse width = (10000H × number of times the TT00VF bit is set + Captured value) × Count clock cycle

[Function name] timermt\_pulse\_measure\_ini

[Argument] None

[Processing content] Sets the TMT0 operation and interrupts, and sets the alternate function of the P04 pin to

TIT00 input pin.

[SFRs used] TT0CTL0.TT0CE: 0 (Disables TMT0 operation.)

PFC0: 0x00 (Sets TIT00 input pin.)
PFCE0: 0x00 (Sets TIT00 input pin.)
PMC0: 0x10 (Sets TIT00 input pin.)

IMR2.TT0CCMK0: 0 (Enables INTTTEQC00 interrupt.)IMR2.TT0CCMK1: 1 (Disables INTTTEQC01 interrupt.)IMR2.TT0OVMK: 0 (Enables INTTTIOV0 interrupt.)

[call function] timermt\_pulse\_measure

[Variable] None

[File name] timermt\_pulse\_measure\timermt\_7.c

[Caution] None

[Function name] timermt\_pulse\_measure

[Argument] None

[Processing content] Sets TMT0 control register.

[SFRs used] TT0CTL0: 0x03 (Sets count clock to fxx/16.)

TT0CTL1: 0x06 (Sets pulse width measurement mode.)

TT0IOC1: 0x02 (Sets valid edge of the capture trigger input signal (TIT00 pin) to

falling edge detection.)

TT0IOC2: 0x00 (Sets valid edge of the external event count input signal (EVTT0

pin) to no edge detection.)

[call function] None

[Variable] None

[File name] timermt\_pulse\_measure\timermt\_7.c

#### CHAPTER 7 PULSE WIDTH MEASUREMENT MODE

[Function name] timermt\_pulse\_measure\_st

[Argument] None

[Processing content] Starting function of timermt\_pulse\_measure

[Starting method] Call this function after calling the timermt\_pulse\_measure function.

[SFR used] TT0CTL0.TT0CE: 1 (Enables TMT0 operation.)

[call function] None
[Variable] None

[File name] timermt\_pulse\_measure\timermt\_7.c

[Caution] None

# Interrupt function

[Function name] timermt\_TT0CCR0\_int

[Overview] Defined by the user.

[Source] INTTTEQC00 TIT00 pin input valid edge detection

[call function] None
[Variable] None

[File name] timermt\_pulse\_measure\timermt\_7.c

[Caution] None

[Function name] timermt\_TTTIOV0\_int

[Overview] Defined by the user.

[Source] INTTTIOV0 16-bit counter overflow occurrence

[call function] None

[Variable] None

[File name] timermt\_pulse\_measure\timermt\_7.c

FΙ Enables interrupt. timermt\_pulse\_measure Internal count clock = fxx/16
Disables external event count input. timermt\_pulse\_ measure\_ini TMT0 timer/event counter (setting) Sets timer mode to pulse width measure TT0CTL0 ← 0x03 mode. No capture trigger input (TIT01) edge detection  $\begin{array}{l} \text{TTOCTL0} \leftarrow 0x03 \\ \text{TTOCTL1} \leftarrow 0x06 \\ \text{TTOIOC1} \leftarrow 0x02 \\ \text{TTOIOC2} \leftarrow 0x00 \end{array}$  Capture trigger input (TIT00) falling edge detection. timermt\_pulse\_ TMT0 timer/event counter (starting) measure\_st No external event count input edge detection TT0OVF is 1? ΪΥes ret Clears overflow flag of 16-bit counter INTTTEQC00 timermt\_pulse\_ (Match between 16-bit counter count value and CCR0) measure ini timermt\_TT0CCR0\_int  $\mathsf{TT0CE} \leftarrow \mathsf{0}$ Disables TMT0 count operation.  $\begin{array}{c} \mathsf{PFC0} \leftarrow \mathsf{0x00} \\ \mathsf{PFCE0} \leftarrow \mathsf{0x00} \\ \mathsf{PMC0} \leftarrow \mathsf{0x10} \end{array}$ ret Sets alternate-function pins.  $\begin{array}{c} \mathsf{TT0CCMK0} \leftarrow 0 \\ \mathsf{TT0CCMK1} \leftarrow 1 \\ \mathsf{TT0OVMK} \leftarrow 0 \end{array}$ Sets interrupt mask flag. (Enables interrupt servicing.) INTTTIOV0 (16-bit counter overflow occurrence) timermt\_TTTIOV0\_int timermt\_pulse\_ TMT0 timer/event counter measure ret ret timermt\_pulse\_  $\mathsf{TT0CE} \leftarrow \mathsf{1}$ Enables TMT0 count operation. ret

Figure 7-1. Pulse Width Measurement Mode

## CHAPTER 8 TRIANGULAR-WAVE PWM OUTPUT MODE

[Function] Starts operation of the 16-bit counter by setting the TT0CTL0.TT0CE bit to 1.

Performs 16-bit counter count up/down, and generates an overflow interrupt request signal (INTTTIOV0) when the 16-bit counter count value reaches 0000H during counting down. Generates a compare match interrupt request signal (INTTTEQC00) when the 16-bit

counter count value and CCR0 buffer register value match during counting up.

Inverts the TOT01 pin output upon a match (INTTTEQC01) between the 16-bit counter count value and CCR1 buffer register value, and outputs the triangular-wave PWM

waveform.

Also, inverts the TOT00 pin output upon a match (INTTTEQC01) between the overflow interrupt request signal (INTTTIOV0), 16-bit counter count value, and the CCR1 buffer

register value, and outputs the PWM waveform. Can be implemented with TMT0 and TMT1.

[Function name] main

[Argument] None

[Processing content] Performs 16-bit counter-count up operation of an fxx/16 count clock, generates a compare

match interrupt request signal (INTTTEQC00) upon a match between the 16-bit counter count value and CCR0 buffer register value, and 16-bit counter switches to the count-down

operation.

Generates an overflow interrupt request signal (INTTTIOV0) when the 16-bit counter count value reaches 0000H during counting down, and 16-bit counter switches to count-up

operation.

[SFR used] None

[call function] timermt\_chopping\_wave\_ini, timermt\_chopping\_wave\_st

[Variable] None

[Interrupts] timermt\_TT0CCR0\_int

timermt\_TT0CCR1\_int timermt\_TTTIOV0\_int

[Interrupt sources] INTTTEQC00

INTTTEQC01 INTTTIOV0

[File name] timermt\_chopping\_wave\MAIN.C

[Function name] timermt\_chopping\_wave\_ini

[Argument] None

[Processing content] Sets the TMT0 operation and interrupts, and sets the alternate-function of the P06 pin to

TOT01 output pin.

[SFRs used] TT0CTL0.TT0CE: 0 (Disables TMT0 operation.)

PFC0: 0x40 (Sets TOT01 output pin.)
PFCE0: 0x00 (Sets TOT01 output pin.)
PMC0: 0x40 (Sets TOT01 output pin.)
IMR2.TT0CCMK0: 0 (Enables INTTTEQC00 interrupt.)
IMR2.TT0CCMK1: 0 (Enables INTTTEQC01 interrupt.)
IMR2.TT0OVMK: 0 (Enables INTTTIOV0 interrupt.)

[call function] timermt\_chopping\_wave

[Variable] None

[File name] timermt\_chopping\_wave\timemt\_8.c

[Caution] None

[Function name] timermt\_chopping\_wave

[Argument] None

[Processing content] Sets TMT0 control register.

[SFRs used] TT0CTL0: 0x03 (Sets count clock to fxx/16.)

TT0CTL1: 0x07 (Sets triangular-wave PWM output mode.)

TT0IOC0: 0x04 (Sets TOT01 pin output to high-level start, and enables timer

output.)

TT0IOC2: 0x00 (Sets valid edge of the external event count input signal (EVTT0

pin) to no edge detection.)

TT0OPT0: 0x00 (Sets the TT0CCR0 and TT0CCR1 as compare registers.)

TT0CCR0: 2499 (Compare register of 16-bit counter)
TT0CCR1: 1499 (Compare register of 16-bit counter)

[call function] None

[Variable] None

[File name] timermt\_chopping\_wave\timemt\_8.c

[Caution] The compare registers are rewritten in the batch write mode.

To rewrite the compare register during timer operation, rewrite the TT0CCR1 register last.

#### CHAPTER 8 TRIANGULAR-WAVE PWM OUTPUT MODE

[Function name] timermt\_chopping\_wave\_st

[Argument] None

[Processing content] Starting function of timermt\_chopping\_wave

[Starting method] Call this function after calling the timermt\_chopping\_wave function.

[SFR used] TT0CTL0.TT0CE: 1 (Enables TMT0 operation.)

[call function] None
[Variable] None

[File name] timermt\_chopping\_wave\timemt\_8.c

[Caution] None

# Interrupt function

[Function name] timermt\_TT0CCR0\_int

[Overview] Defined by the user.

[Source] INTTTEQC00 Match between the count value of the 16-bit counter and the value of the

CCR0 buffer register

[call function] None

[Variable] None

[File name] timermt\_chopping\_wave\timemt\_8.c

[Caution] None

[Function name] timermt\_TT0CCR1\_int

[Overview] Defined by the user.

[Source] INTTTEQC01 Match between the count value of the 16-bit counter and the value of the

CCR1 buffer register

[call function] None

[Variable] None

[File name] timermt\_chopping\_wave\timemt\_8.c

## CHAPTER 8 TRIANGULAR-WAVE PWM OUTPUT MODE

[Function name] timermt\_TTTIOV0\_int

[Overview] Defined by the user.

[Source] INTTTIOV0 16-bit counter overflow occurrence

[call function] None
[Variable] None

[File name] timermt\_chopping\_wave\timemt\_8.c

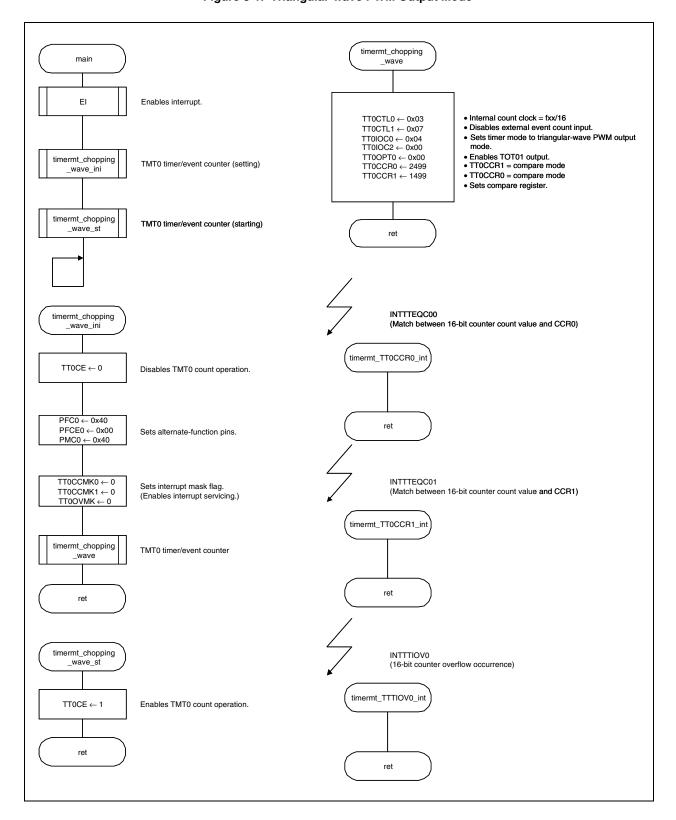


Figure 8-1. Triangular-wave PWM Output Mode

## **CHAPTER 9 ENCODER COMPARE MODE**

[Function] Starts the 16-bit counter operation by setting the TT0CTL0.TT0CE bit to 1 to transfer the

TT0TCW register set value to the 16-bit counter.

Generates a compare match interrupt request signal (INTTTEQC00) upon a match

between the 16-bit counter count value and the CCR0 buffer register value.

Generates a compare match interrupt request signal (INTTTEQC01) upon a match

between the 16-bit counter count value and CCR1 buffer register value.

Can be implemented with TMT0 and TMT1.

[Function name] main

[Argument] None

[Processing content] Performs 16-bit counter count-up operation of an fxx/16 count clock, and generates a

compare match interrupt request signal (INTTTEQC00) upon a match between the 16-bit

counter count value and CCR0 buffer register value.

Clears the 16-bit counter to 0000H if the next count operation is counting up.

Generates a compare match interrupt request signal (INTTTEQC01) upon a match

between the 16-bit counter count value and CCR1 buffer register value.

Clears the 16-bit counter to 0000H if the next count operation is counting down.

[SFR used] None

[call function] timermt\_encod\_compare\_ini, timermt\_encod\_compare\_st

[Variable] None

[Interrupts] timermt\_TT0CCR0\_int

timermt\_TT0CCR1\_int

[Interrupt sources] INTTTEQC00

INTTTEQC01

[File name] timermt\_encod\_compare\MAIN.C

#### **CHAPTER 9 ENCODER COMPARE MODE**

[Function name] timermt\_encod\_compare\_ini

[Argument] None

[Processing content] Sets the TMT0 operation and interrupts, and set the alternate function of the P05 pin to

TENC00 input pin and the P06 pin to TENC01 input pin.

[SFRs used] TT0CTL0.TT0CE: 0 (Disables TMT0 operation.)

PFC0: 0x00 (Sets TENC00 input pin, TENC01 input pin.)
PFCE0: 0x00 (Sets TENC00 input pin, TENC01 input pin.)
PMC0: 0x60 (Sets TENC00 input pin, TENC01 input pin.)

IMR2.TT0CCMK0: 0 (Enables INTTTEQC00 interrupt.)
IMR2.TT0CCMK1: 0 (Enables INTTTEQC01 interrupt.)

[call function] timermt\_encod\_compare

[Variable] None

[File name] timermt\_encod\_compare\timermt\_9.c

[Function name] timermt\_encod\_compare

[Argument] None

[Processing content] Sets TMT0 control register.

[SFRs used] TT0CTL0: 0x03 (Sets count clock to fxx/16.)

TT0CTL1: 0x08 (Sets encoder compare mode.)

TT0CTL2: Sets to clear the 16-bit counter to 0000H upon a match between the 16-

bit counter count value and CCR0 buffer register value, and to clear the 16-bit counter to 0000H upon a match between the 16-bit counter count

value and CCR1 buffer register value.

TT0IOC3: 0x00 (Sets encoder clear signal (TECR0 pin) edge detection clear.)

TT0TCW: 0x00 (Initializes the 16-bit counter.)

TT0CCR0: 2499 (Compare register of 16-bit counter)

TT0CCR1: 1499 (Compare register of 16-bit counter)

[call function] None
[Variable] None

[File name] timermt\_encod\_compare\timermt\_9.c

[Caution]

- If a value which is the same as that of the TT0TCW register is set to the TT0CCR0 or TT0CCR1 register and the counter operation is started when the TT0CTL2.TT0ECC bit = 0, and if the count value (TT0TCW) of the 16-bit counter matches the value of the CCRa buffer register immediately after the start of the operation, the match is masked and the compare match interrupt request signal (INTTTEQC0a) is not generated (a = 0, 1). In addition, the 16-bit counter is not cleared to 0000H by setting the TT0CTL2.TT0ECM1 and TT0CTL2.TT0ECM0 bits.
- If the count operation is resumed when the TT0CTL2.TT0ECC bit = 1, the 16-bit counter does not overflow if its count value that has been held is FFFFH and if the next count operation is counting up.

After the counter starts operating and counts up from a count value (value of TT0TCW register = FFFFH), the counter overflows from FFFFH to 0000H. However, detection of the overflow is masked, the overflow flag (TT0EOF) is not set, and the overflow interrupt request signal (INTTTIOV0) is not generated.

#### CHAPTER 9 ENCODER COMPARE MODE

[Function name] timermt\_encod\_compare\_st

[Argument] None

[Processing content] Starting function of timermt\_encod\_compare

[Starting method] Call this function after calling the timermt\_encod\_compare function.

[SFR used] TT0CTL0.TT0CE: 1 (Enables TMT0 operation.)

[call function] None
[Variable] None

[File name] timermt\_encod\_compare\timermt\_9.c

[Caution] None

# Interrupt function

[Function name] timermt\_TT0CCR0\_int

[Overview] Defined by the user.

[Source] INTTTEQC00 Match between the count value of the 16-bit counter and the value of the

CCR0 buffer register

[call function] None

[Variable] None

[File name] timermt\_encod\_compare\timermt\_9.c

[Caution] None

[Function name] timermt\_TT0CCR1\_int

[Overview] Defined by the user.

[Source] INTTTEQC01 Match between the count value of the 16-bit counter and the value of the

CCR1 buffer register

[call function] None

[Variable] None

[File name] timermt\_encod\_compare\timermt\_9.c

timermt\_encod \_compare ΕI Enables interrupt.  $\begin{array}{l} \mathsf{TT0CTL0} \leftarrow \mathsf{0x03} \\ \mathsf{TT0CTL1} \leftarrow \mathsf{0x08} \end{array}$ • Internal count clock = fxx/16 • Disables external event count input. TT0CTL2.3 ← 1 • Sets timer mode to encoder compare TT0CTL2.2 ← 1 mode • CCR1, CCR0 = encoder clear  $\mathsf{TT0IOC3} \leftarrow \mathsf{0x00}$ timermt\_encod • Sets edge detection clear of encoder  $\mathsf{TT0TCW} \leftarrow \mathsf{0x00}$ TMT0 timer/event counter (setting) \_compare\_ini clear signal (TECR0)  $\begin{array}{l} \mathsf{TT0CCR0} \leftarrow \mathsf{2499} \\ \mathsf{TT0CCR1} \leftarrow \mathsf{1499} \end{array}$ • Initializes 16-bit counter. • Sets compare register. timermt\_encod TMT0 timer/event counter (starting) \_compare\_st ret timermt\_encod INTTTEQC00 \_compare\_ini (Match between 16-bit counter count value and CCR0) timermt\_TT0CCR0\_int  $\mathsf{TT0CE} \leftarrow \mathsf{0}$ Disables TMT0 count operation.  $\begin{array}{c} \mathsf{PFC0} \leftarrow \mathsf{0x00} \\ \mathsf{PFCE0} \leftarrow \mathsf{0x00} \end{array}$ ret Sets alternate-function pins.  $\mathsf{PMC0} \leftarrow \mathsf{0x60}$ INTTTEQC01  $\mathsf{TT0CCMK0} \leftarrow \mathsf{0}$ Sets interrupt mask flag. (Match between 16-bit counter count value and CCR1)  $\mathsf{TT0CCMK1} \leftarrow \mathsf{0}$ (Enables interrupt servicing.) timermt\_TT0CCR1\_int timermt encod TMT0 timer/event counter \_compare ret ret timermt encod TT0CE ← 1 Enables TMT0 count operation.

Figure 9-1. Encoder Compare Mode

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