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RENESAS

Preliminary Application Note

V850E/IF3, V850E/IG3

32-bit Single-Chip Microcontrollers

Sample Programs for Clock Generator

V850E/IF3:
- μPD70F3451
- μPD70F3452

V850E/IG3:
- μPD70F3453
- μPD70F3454

Document No. U18734EJ1V0AN00 (1st edition)
Date Published September 2007 N

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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M5 02. 11-1

INTRODUCTION

Cautions 1. This Application Note explains a case where the V850E/IG3 is used as a representative microcontroller. Use this Application Note for your reference when using the V850E/IF3.

2. Download the program used in this manual from the page of Programming Examples (http://www.necel.com/micro/en/designsupports/sampleprogram/index.html) in the NEC Electronics Website (http://www.necel.com/).

3. The sample programs are provided for reference purposes only and operations are therefore not subject to guarantee by NEC Electronics Corporation. When using sample programs, customers are advised to sufficiently evaluate this product based on their systems, before use.

4. When using sample programs, reference the following startup routine and link directive file and adjust them if necessary.

- **Startup routine: ig3_start.s**
- **Link directive file: ig3_link.dir**

Target Readers

This Application Note is intended for users who understand the functions of the V850E/IF3 (μPD70F3451, 70F3452), and V850E/IG3 (μPD70F3453, 70F3454), and who design application systems that use these microcontrollers.

Purpose

This manual is intended to give users an understanding of the basic functions of the V850E/IF3 and V850E/IG3, using the application programs.

How to Use This Manual

It is assumed that the reader of this Application Note has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

For details of hardware functions (especially register functions, setting methods, etc.) and electrical specifications

→ See the **V850E/IF3, V850E/IG3 Hardware User's Manual**.

For details of instruction functions

→ See the **V850E1 Architecture User's Manual**.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Active low representation:	$\overline{xxx}$ (overscore over pin or signal name)
Memory map address:	Higher addresses on the top and lower addresses on the bottom
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeric representation:	Binary ... xxxx or xxxxB
	Decimal ... xxxx
	Hexadecimal ... xxxxH
Prefix indicating the power of 2 (address space, memory capacity):	K (kilo): $2^{10} = 1,024$
	M (mega): $2^{20} = 1,024^2$
	G (giga): $2^{30} = 1,024^3$

The function lists are structured as follows.

Theme

[Function]	Function description
[Function name]	Name of sample function
[Argument(s)]	Type and overview of argument(s)
[Processing content]	Processing content of sample function
[Starting method]	Conditions for calling a function
[SFR(s) used]	Register name and setting content
[call function(s)]	Name and function of call function(s)
[Variable(s)]	Type, name, and overview of variable(s) used in sample function
[Interrupt(s)]	Name of function
[Interrupt source(s)]	Name
[File name]	Name of corresponding sample program file
[Caution(s)]	Caution(s) upon function usage

Product Differences The differences between the V850E/IG3 and the V850E/IF3 related to the clock generator are shown below.

Item	V850E/IG3	V850E/IF3
CLKOUT pin	Provided (μPD70F3454GC-8EA-A only)	None

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents related to V850E/IF3 and V850E/IG3

Document Name	Document No.
V850E1 Architecture User's Manual	U14559E
V850E/IF3, V850E/IG3 Hardware User's Manual	U18279E
V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (UARTA) Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (UARTB) Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (CSIB) Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (I^2C) Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for DMA Function Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Timer M Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Watchdog Timer Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Timer AA Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Timer AB Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Timer T Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Port Function Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Clock Generator Application Note	This manual
V850E/IF3, V850E/IG3 Sample Programs for Standby Function Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Interrupt Function Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for A/D Converters 0 and 1 Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for A/D Converter 2 Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Low-Voltage Detector (LVI) Function Application Note	To be prepared
V850E/IF3, V850E/IG3 6-Phase PWM Output Control by Timer AB, Timer Q Option, Timer AA, A/D Converters 0 and 1 Application Note	U18717E

CONTENTS

[Function]	Sets the clock frequency by setting the CPU operation clock (PLL mode) and the PCC register which is a special register.
[Function name]	pll_main
[Argument]	None
[Processing content]	Calls the PLL setting function by terminating all DMAs in use. When DMA is not used, the terminate processing of DMA is not needed.
[Starting method]	None
[SFR used]	None
[call functions]	clock_pll_mode, clock_pcc_mode
[Variable]	None
[Interrupt]	None
[Interrupt source]	None
[File name]	clock_generator1.c
[Caution]	Note that if the pll_main function is called the maskable interrupt request will not be enabled (EI).

[Function name]	clock_pll_mode
[Processing content]	Sets to PLL mode by the PLLCTL register.
[SFR used]	PLLCTL: 0x03 (Sets to PLL mode.)
[call functions]	None
[Variable]	None
[File name]	clock_generator1.c
[Caution]	None

[Function name]	clock_pcc_mode	
[Processing content]	Sets the PCC register by forcibly terminating DMA transfer.	
[SFRs used]	DCHC0.TC0:	DMA0 transfer status bit
	DCHC0.E00:	1 (Enables DMA0 transfer.)
	DCHC0.INIT0:	1 (Forcibly terminates DMA0 transfer.)
	DCHC1.TC1	DMA1 transfer status bit
	DCHC1.E11:	1 (Enables DMA1 transfer.)
	DCHC1.INIT1:	1 (Forcibly terminates DMA1 transfer.)
	DCHC2.TC2	DMA2 transfer status bit
	DCHC2.E22:	1 (Enables DMA2 transfer.)
	DCHC2.INIT2:	1 (Forcibly terminates DMA2 transfer.)
	DCHC3.TC3	DMA3 transfer status bit
	DCHC3.E33:	1 (Enables DMA3 transfer.)
	DCHC3.INIT3:	1 (Forcibly terminates DMA3 transfer.)
	PRCMD:	0x00 (Writes to command register (used when writing to a special register).)
	PCC:	0x00 (Selects clock as f_{XX}.)
[call functions]	None	
[Variable]	None	
[File name]	clock_generator1.c	
[Cautions]	• DMA transfer is forcibly terminated in this sample program, because all DMA transfers must be terminated before performing data setting to the special register. When DMA is not used, the terminate processing of DMA is not needed. • Set the PCC register after switching to the PLL mode. The PCC register is a special register and can therefore only be written in a combination of specific sequences.	

Figure 1-1. PLL mode (1/2)

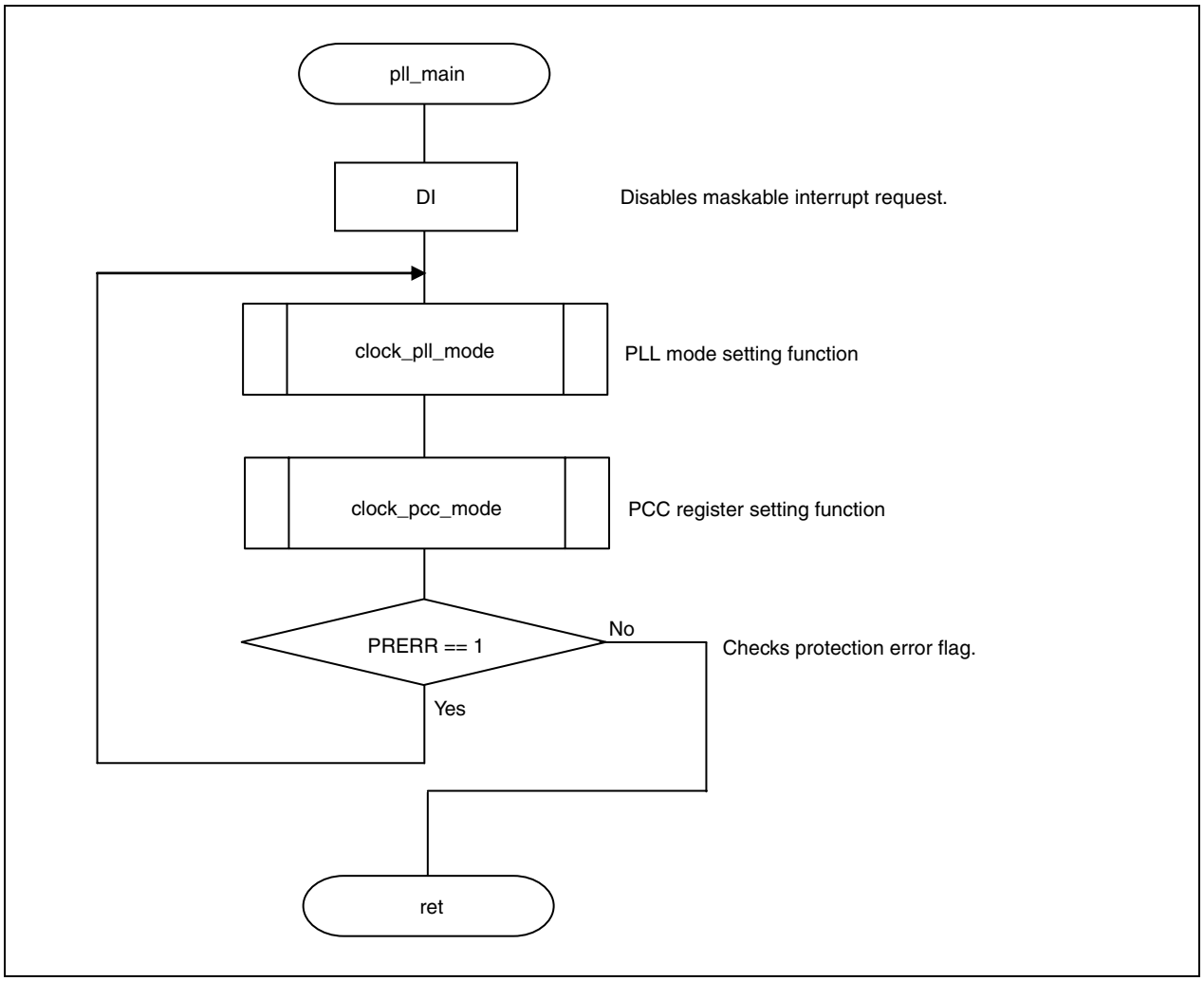
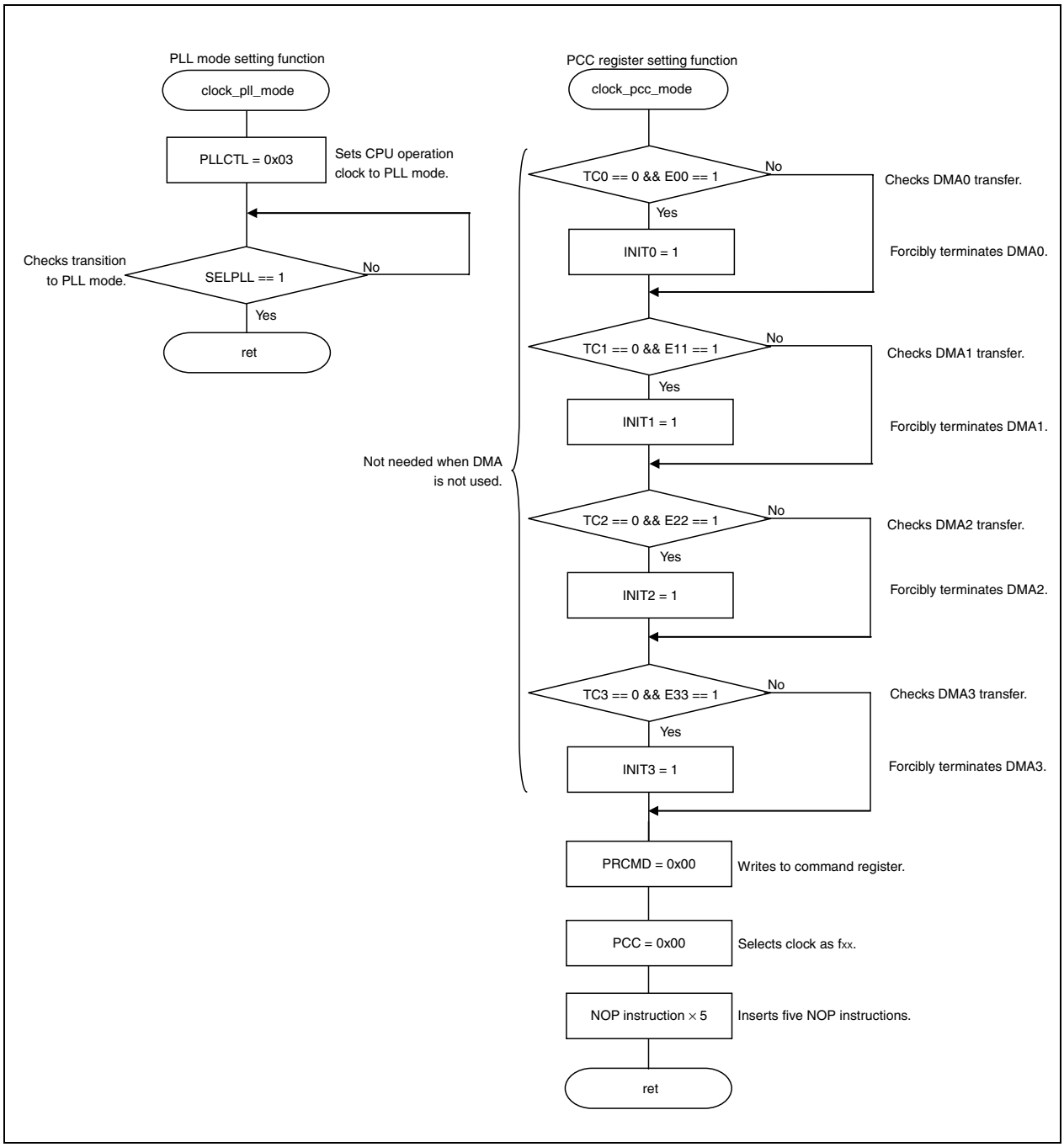


Figure 1-1. PLL mode (2/2)



CHAPTER 2 CLOCK MONITOR MODE

[Function]	Performs clock monitor operation.
[Function name]	clock_monitor_main
[Argument]	None
[Processing content]	Enables operation of the clock monitor mode by calling the clock monitor mode function.
[Starting method]	None
[SFR used]	None
[call functions]	clock_monitor_mode
[Variable]	None
[Interrupt]	None
[Interrupt source]	None
[File name]	clock_generator2.c
[Caution]	Note that if the clock_monitor_main function is called the maskable interrupt request will not be enabled (EI).

[Function name]	clock_monitor_mode	
[Processing content]	Sets the operation mode of the clock monitor via the CLM register, by forcibly terminating DMA transfer.	
[SFRs used]	DCHC0.TC0	DMA0 transfer status bit
	DCHC0.E00:	1 (Enables DMA0 transfer.)
	DCHC0.INIT0:	1 (Forcibly terminates DMA0 transfer.)
	DCHC1.TC1	DMA1 transfer status bit
	DCHC1.E11:	1 (Enables DMA1 transfer.)
	DCHC1.INIT1:	1 (Forcibly terminates DMA1 transfer.)
	DCHC2.TC2	DMA2 transfer status bit
	DCHC2.E22:	1 (Enables DMA2 transfer.)
	DCHC2.INIT2:	1 (Forcibly terminates DMA2 transfer.)
	DCHC3.TC3	DMA3 transfer status bit
	DCHC3.E33:	1 (Enables DMA3 transfer.)
	DCHC3.INIT3:	1 (Forcibly terminates DMA3 transfer.)
	PRCMD:	0x01 (Writes to command register (used when writing to a special register).)
	CLM:	0x01 (Enables operation of clock monitor.)
[call functions]	None	
[Variable]	None	
[File name]	clock_generator2.c	
[Cautions]	• DMA transfer is forcibly terminated in this sample program, because all DMA transfers must be terminated before performing data setting to the special register. When DMA is not used, the terminate processing of DMA is not needed. • The CLM register is a special register and can therefore only be written in a combination of specific sequences.	

Figure 2-1. Clock Monitor Mode (1/2)

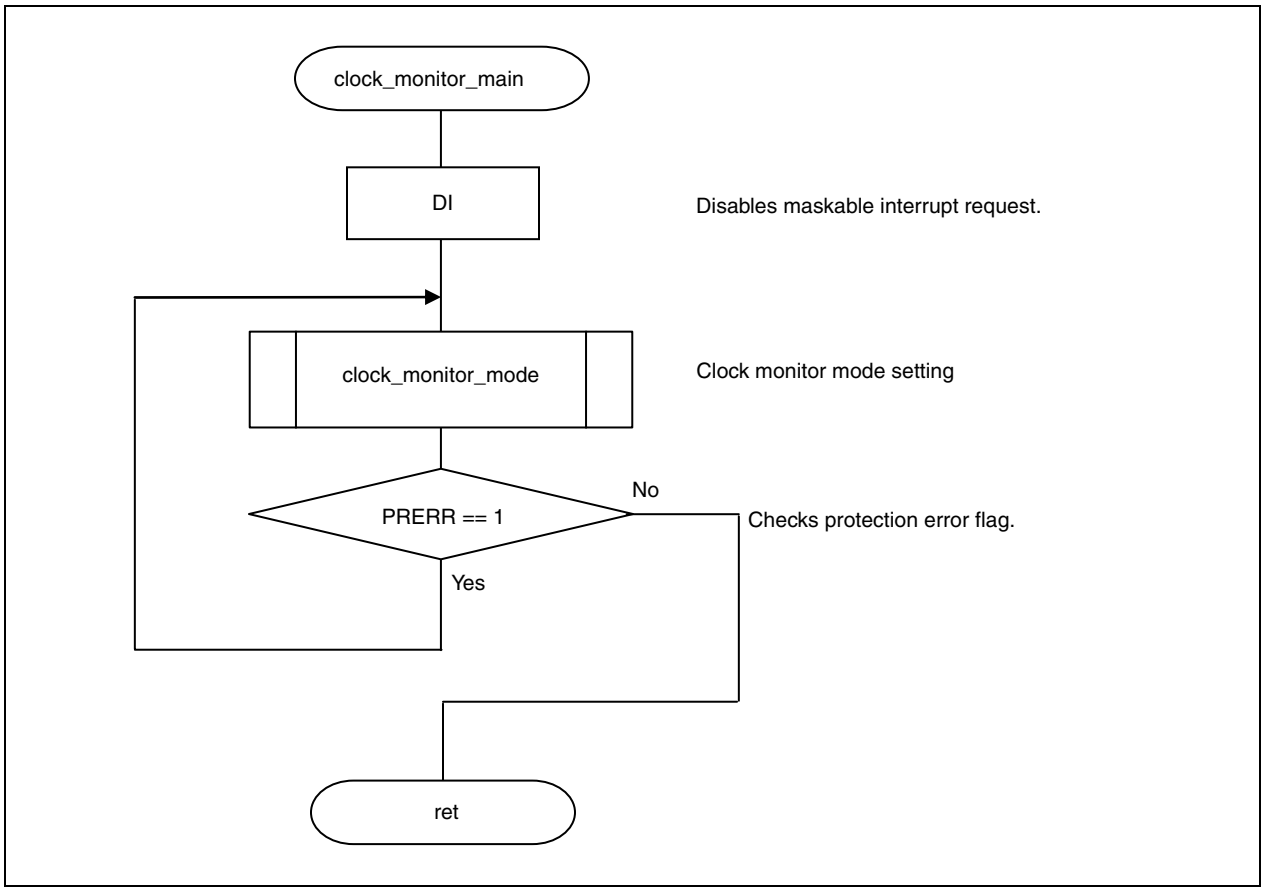
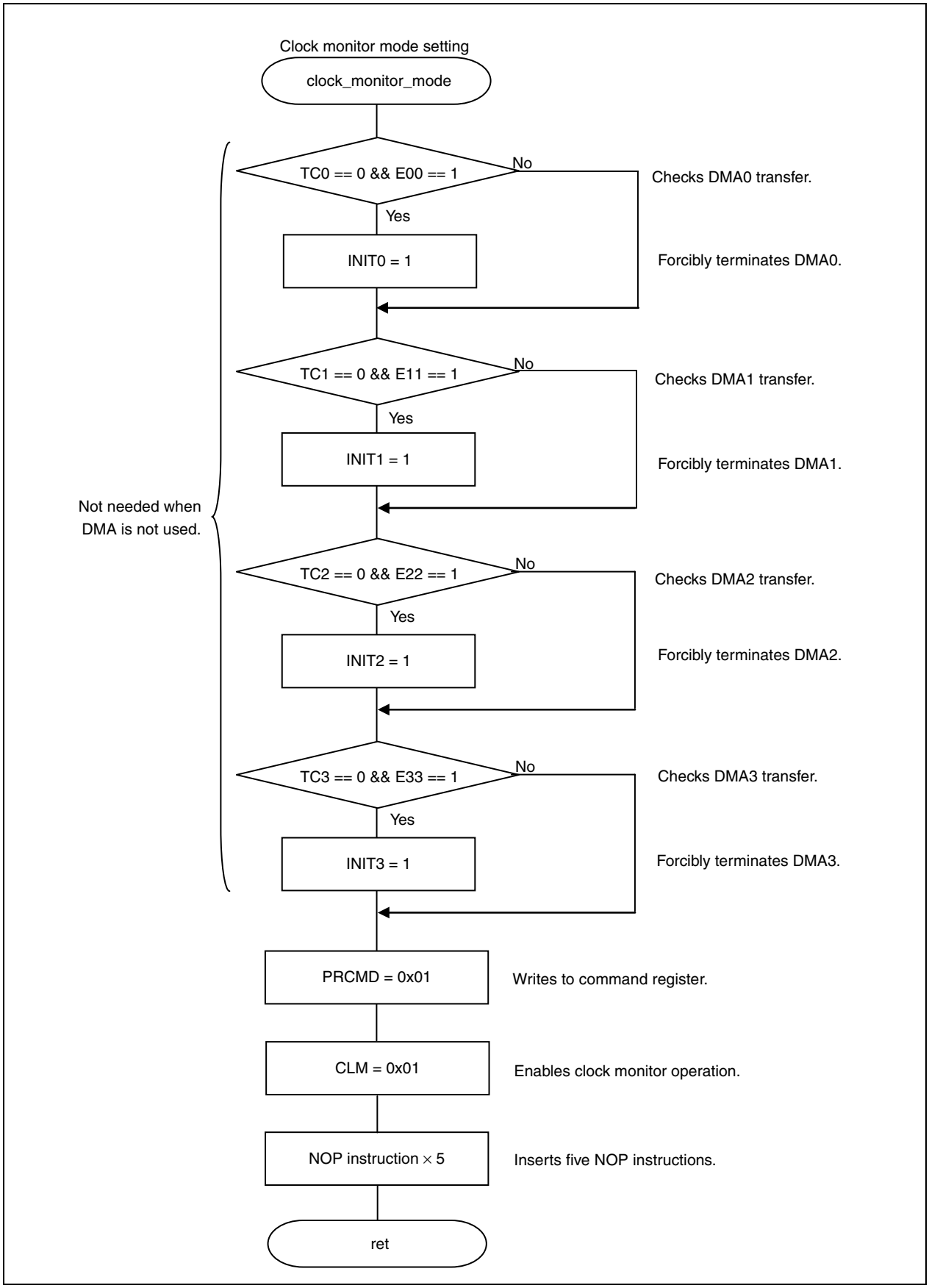


Figure 2-1. Clock Monitor Mode (2/2)



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