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RENESAS

Preliminary Application Note

V850E/IF3, V850E/IG3

32-bit Single-Chip Microcontrollers

6-Phase PWM Output Control by Timer AB, Timer Q Option, Timer AA, A/D Converters 0 and 1

V850E/IF3:
- μPD70F3451
- μPD70F3452

V850E/IG3:
- μPD70F3453
- μPD70F3454

Document No. U18717EJ1V0AN00 (1st edition)
Date Published August 2007 N

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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M5 02. 11-1

INTRODUCTION

Cautions 1. This Application Note explains a case where the V850E/IG3 (μPD70F3454GC-8EA-A) is used as a representative microcontroller. Use this Application Note for your reference when using the V850E/IG3 (other than the μPD70F3454GC-8EA-A) and V850E/IF3.

2. Download the program used in this manual from the page of Programming Examples (http://www.necel.com/micro/en/designsupports/sampleprogram/index.html) in the NEC Electronics Website (http://www.necel.com/).

3. When using sample programs, reference the following startup routine and link directive file and adjust them if necessary.

- **Startup routine: ig3_start.s**
- **Link directive file: ig3_link.dir**

4. This sample program is provided for reference purposes only and operations are therefore not subject to guarantee by NEC Electronics Corporation. When using sample programs, customers are advised to sufficiently evaluate this product based on their systems, before use.

Target Readers

This Application Note is intended for users who understand the functions of the V850E/IF3 and V850E/IG3, and who design application systems that use these microcontrollers. The applicable products are shown below.

- V850E/IF3
  μPD70F3451, 70F3452
- V850E/IG3
  μPD70F3453, 70F3454

Purpose

This Application Note explains, for your reference, how to set a 6-phase PWM output mode and A/D conversion starting trigger timing using 16-bit timer/event counter AB0 (TAB0), timer Q0 option (TMQOP0), 16-bit timer/event counter AA0 (TAA0), and A/D converters 0 and 1 which are necessary for inverter control of a 3-phase motor by the V850E/IF3 or V850E/IG3.

Organization

This Application Note is divided into the following sections.

- Hardware configuration
- Control method
- Program configuration
- File configuration
- Flowchart
- Settings

How to Use This Manual

It is assumed that the reader of this Application Note has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

For details of hardware functions (especially register functions, setting methods, etc.) and electrical specifications

→ See the **V850E/IF3, V850E/IG3 Hardware User's Manual**.

For details of instruction functions

→ See the **V850E1 Architecture User's Manual**.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Active low representation:	$\overline{xxx}$ (overscore over pin or signal name)
Memory map address:	Higher addresses on the top and lower addresses on the bottom
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeric representation:	Binary ... xxxx or xxxxB
	Decimal ... xxxx
	Hexadecimal ... xxxxH
Prefix indicating the power of 2 (address space, memory capacity):	K (kilo): $2^{10} = 1,024$
	M (mega): $2^{20} = 1,024^2$
	G (giga): $2^{30} = 1,024^3$
Data type:	Word: 32 bits
	Halfword: 16 bits
	Byte: 8 bits

Product Differences

The differences between the V850E/IG3 and the V850E/IF3 related to the timer Q option (TMQOP) and 16-bit timer/event counter AA (TAA) are shown below.

Item		V850E/IG3	V850E/IF3
TMQOP	TOA3OFF	Available	None
TAA	TIA30 pin	Available	None
	TIA31 pin	Available	None
	TOA30 pin	Available	None
	TOA31 pin	Available	None

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents related to V850E/IF3 and V850E/IG3

Document Name	Document No.
V850E1 Architecture User's Manual	U14559E
V850E/IF3, V850E/IG3 Hardware User's Manual	U18279E
V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (UARTA) Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (UARTB) Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (CSIB) Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Serial Communication (I^2C) Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for DMA Function Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Timer M Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Watchdog Timer Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Timer AA Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Timer AB Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Timer T Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Port Function Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Clock Generator Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Standby Function Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Interrupt Function Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for A/D Converters 0 and 1 Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for A/D Converter 2 Application Note	To be prepared
V850E/IF3, V850E/IG3 Sample Programs for Low-Voltage Detector (LVI) Function Application Note	To be prepared
V850E/IF3, V850E/IG3 6-Phase PWM Output Control by Timer AB, Timer Q Option, Timer AA, A/D Converters 0 and 1 Application Note	This manual

Documents related to development tools (user's manuals)

Document Name		Document No.
QB-V850EIX3 In-Circuit Emulator		U18651E
QB-V850MINI On-Chip Debug Emulator		U17638E
QB-MINI2 On-Chip Debug Emulator with Programming Function		U18371E
CA850 Ver. 3.00 C Compiler Package	Operation	U17293E
	C Language	U17291E
	Assembly Language	U17292E
	Link Directives	U17294E
PM+ Ver. 6.30 Project Manager		U18416E
ID850QB Ver. 3.40 Integrated Debugger	Operation	U18604E
TW850 Ver. 2.00 Performance Analysis Tuning Tool		U17241E
SM+ System Simulator	Operation	U18601E
	User Open Interface	U18212E
RX850 Ver. 3.20 Real-Time OS	Basics	U13430E
	Installation	U17419E
	Technical	U13431E
	Task Debugger	U17420E
RX850 Pro Ver. 3.21 Real-Time OS	Basics	U18165E
	Installation	U17421E
	Technical	U13772E
	Task Debugger	U17422E
AZ850 Ver. 3.30 System Performance Analyzer		U17423E
PG-FP4 Flash Memory Programmer		U15260E

CONTENTS

CHAPTER 1 HARDWARE CONFIGURATION

This chapter describes the hardware configuration of the 3-phase PWM driver.

1.1 Operation

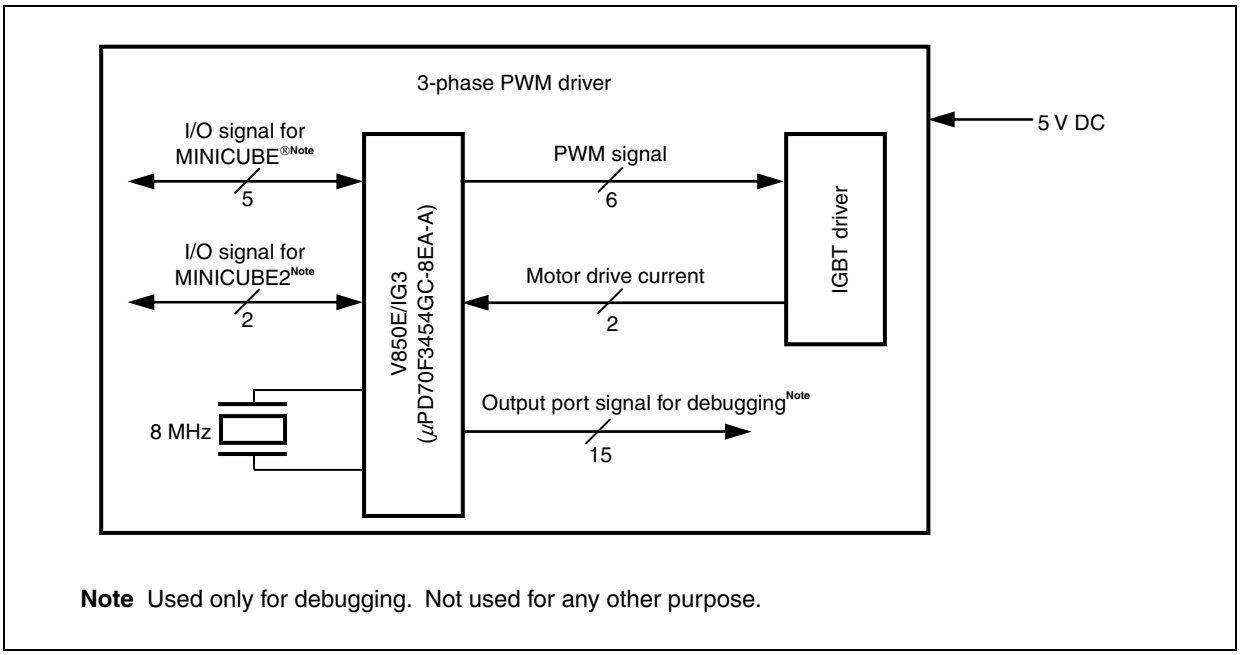
The following shows the main functions of the 3-phase PWM driver.

- Pulse duty for U, V, and W phases can be set freely by specifying the d axis, q axis, and rotational coordinates (θ).
- PWM pulse of the same duty can be continuously output in output lock mode.
- PWM output pins (TOB0T1 to TOB0T3, TOB0B1 to TOB0B3) can be set to high-impedance state by software.
- The start trigger for conversion of A/D converters 0 and 1 can be generated in synchronization with carrier cycles.

1.2 System Configuration

The system configuration is shown below.

Figure 1-1. System Configuration Diagram



Note Used only for debugging. Not used for any other purpose.

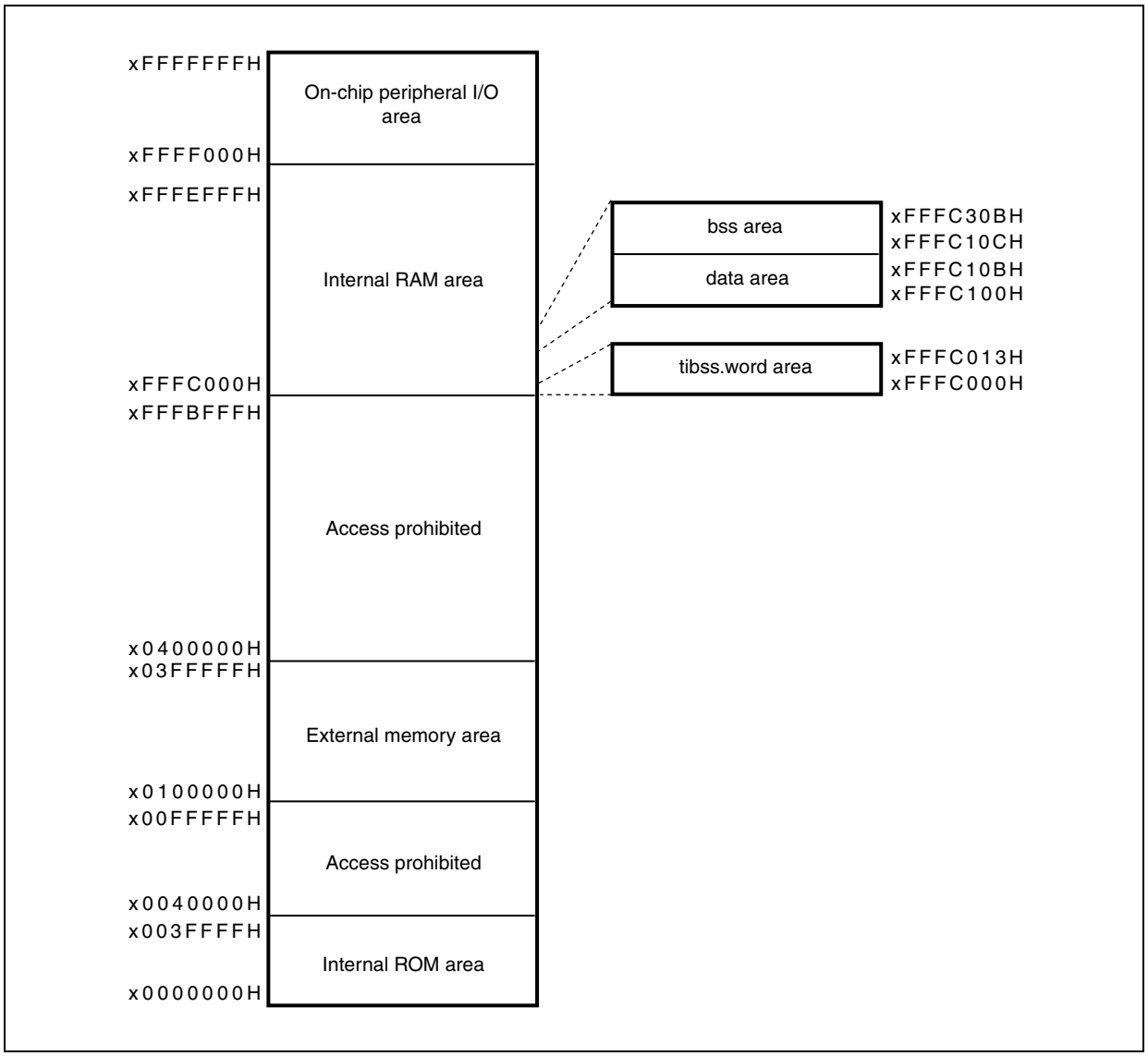
1.3 CPU Block

The 3-phase PWM driver inputs an 8 MHz clock to the V850E/IG3 (μPD70F3454GC-8EA-A) and operates at 64 MHz by multiplying the clock by eight. The internal RAM size of the V850E/IG3 (μPD70F3454GC-8EA-A) is 12 KB.

1.3.1 Memory map

The memory map is shown below.

Figure 1-2. Memory Map



1.3.2 Pin assignment

Pin assignments of the V850E/IG3 (μPD70F3454GC-8EA-A) are shown below.

Table 1-1. V850E/IG3 (μPD70F3454GC-8EA-A) Pin Assignment (1/3)

Pin No.	Pin Name	I/O Mode Setting	Signal Name	Active Level
1	EV_{SS1}	–	Ground potential for internal unit	GND
2	ANI00	Input	Motor drive current for A/D converter 0	0 to +5 V
3	ANI01	–	Unused	–
4	ANI02	–		–
5	AIN03	–		–
6	AIN04	–		–
7	AV_{SS0}	–	Ground potential for A/D converter 0	GND
8	AV_{REFP0}	–	Reference voltage input for A/D converter 0	+5 V
9	AV_{DD0}	–	Positive power supply for A/D converter 0	+5 V
10	AV_{DD1}	–	Positive power supply for A/D converter 1	+5 V
11	AV_{REFP1}	–	Reference voltage input for A/D converter 1	+5 V
12	AV_{SS1}	–	Ground potential for A/D converter 1	GND
13	ANI14	–	Unused	–
14	ANI13	–		–
15	ANI12	–		–
16	ANI11	–		–
17	ANI10	–	Motor drive current for A/D converter 1	0 to +5 V
18	P77	Input	Unused	–
19	P76	Input		–
20	P75	Input		–
21	P74	Input		–
22	P73	Input		–
23	P72	Input		–
24	P71	Input		–
25	P70	Input		–
26	AV_{DD2}	–	Positive power supply for A/D converter 2	+5 V
27	AV_{SS2}	–	Ground potential for A/D converter 2	+5 V
28	P20	Input	Unused	–
29	P21	Input		–
30	P22	Input		–
31	P23	Input		–
32	P24	Input		–
33	P25	Input		–
34	P26	Input		–
35	V_{DD0}	–	Positive power supply for internal unit	+5 V
36	REGC0	–	Regulator output stabilization capacitor connection	–
37	V_{SS0}	–	Ground potential for internal unit	GND
38	X1	Input	Unused	–
39	X2	–		–

Table 1-1. V850E/IG3 (μPD70F3454GC-8EA-A) Pin Assignment (2/3)

Pin No.	Pin Name	I/O Mode Setting	Signal Name	Active Level
40	$\overline{\text{RESET}}$	Input	System reset input	L
41	EV_{DD2}	–	Positive power supply for external pin	GND
42	EV_{SS2}	–	Ground potential for external pin	GND
43	$\overline{\text{DRST}}$	Input	Debug reset input for on-chip debug emulator (used only in debugging)	L
44	DDO	Output	Debug data output for on-chip debug emulator (used only in debugging)	L
45	P27	Input	Unused	–
46	FLMD0	Input	Flash memory programming mode setting pin	H
47	RXDA0	Input	Serial receive data input for UARTA0	L
48	TXDA0	Output	Serial transmit data output for UARTA0	L
49	P42	Input	Unused	–
50	P43	Input		–
51	P44	Input		–
52	P45	Input		–
53	P46	Input		–
54	P47	Input		–
55	P30	Input		–
56	P31	Input		–
57	P32	Input		–
58	P33	Input		–
59	P34	Input		–
60	P35	Input		–
61	P36	Input		–
62	P37	Input		–
63	P07	Input		–
64	EV_{SS0}	–	Ground potential for external pin	GND
65	EV_{DD0}	–	Positive power supply for external pin	+5 V
66	PDL15	Input (output in debugging)	Output ports for debugging	– (H in debugging)
67	PDL14	Input (output in debugging)		– (H in debugging)
68	PDL13	Input (output in debugging)		– (H in debugging)
69	PDL12	Input (output in debugging)		– (H in debugging)
70	PDL11	Input (output in debugging)		– (H in debugging)
71	PDL10	Input (output in debugging)		– (H in debugging)
72	PDL9	Input (output in debugging)		– (H in debugging)
73	PDL8	Input (output in debugging)		– (H in debugging)
74	PDL7	Input (output in debugging)		– (H in debugging)
75	PDL6	Input (output in debugging)		– (H in debugging)

Remark L: low level
H: high level

Table 1-1. V850E/IG3 (μPD70F3454GC-8EA-A) Pin Assignment (3/3)

Pin No.	Pin Name	I/O Mode Setting	Signal Name	Active Level
76	FLMD1	Input	Flash memory programming mode setting pin	H
77	PDL4	Input (output in debugging)	Output ports for debugging	– (H in debugging)
78	PDL3	Input (output in debugging)		– (H in debugging)
79	PDL2	Input (output in debugging)		– (H in debugging)
80	PDL1	Input (output in debugging)		– (H in debugging)
81	PDL0	Input (output in debugging)		– (H in debugging)
82	P06	Input	Unused	–
83	P05	Input		–
84	P04	Input		–
85	V_{SS1}	–	Ground potential for internal unit	GND
86	REGC1	–	Regulator output stabilization capacitor connection	–
87	V_{DD1}	–	Positive power supply for internal unit	+5 V
88	P03	Input	Unused	–
89	P02	Input		–
90	P01	Input		–
91	P00	Input		–
92	P17	Input		–
93	P16	Input		–
94	TOB0B3	Output	$\overline{W}$ phase output	–
95	TOB0T3	Output	W phase output	–
96	TOB0B2	Output	$\overline{V}$ phase output	–
97	TOB0T2	Output	V phase output	–
98	TOB0B1	Output	$\overline{U}$ phase output	–
99	TOB0T1	Output	U phase output	–
100	EV_{DD1}	–	Positive power supply for external pin	+5 V

Remark H: high level

1.3.3 On-chip peripheral I/O

The following peripheral I/Os are used in the 3-phase PWM driver.

Table 1-2. On-Chip Peripheral I/Os Used

On-Chip Peripheral I/O Function Name (V850E/IG3 (μPD70F3454GC-8EA-A))	Function
PDL0 to PDL4, PDL6 to PDL15	For debugging (used only for debugging, not used for any other purpose)
Timer AB0 (TAB0) + TMQ0 option (TMQOP0) + Timer AA0 (TAA0)	PWM output
ANI00	Motor drive current for A/D converter 0
ANI10	Motor drive current for A/D converter 1
On-chip debug function (MINICUBE, MINICUBE2)	Using DCU: MINICUBE used Without using DCU: MINICUBE2

(1) Description of on-chip peripheral I/O function

(a) Output ports for debugging

Ports used in program debugging. Do not input/output for any other purpose.

(b) PWM output

- TAB0: Sets the PWM timer count and duty ratio in 6-phase PWM output mode.
- TMQOP0: Appends a dead time to PWM, generated by TAB0.
- TAA0: Synchronizes TAA0 and TAB0, and generates the start trigger for conversion of A/D converters 0 and 1.

PWM settings by the 3-phase PWM driver are as follows.

Carrier frequency: 20 kHz
Dead time: 4 μs
Culling rate: 1/1

Table 1-3. PWM Output Pin Output Level

TOB0T1 to TOB0T3, TOB0B1 to TOB0B3	Output Level
Before execution of CALL instruction for 3-phase PWM	High impedance
While 3-phase PWM driver is operating	High impedance/high level/low level

(c) ANI00

In response to the trigger from TAA0, performs A/D conversion of the ANI00 value. After the A/D conversion completes, generates the A/D0 conversion completion interrupt (INTAD0) of the priority level 4.

ANI00: 0 to +5 V
INTTA0CC0 trigger timing: 1 μs after the TAB0 valley interrupt (INTTB0OV) of the carrier cycle
A/D conversion completion time: 2 μs

(d) ANI10

In response to the trigger from TAA0, performs A/D conversion of the ANI10 value. After the A/D conversion completes, generates the A/D1 conversion completion interrupt (INTAD1) of the priority level 4.

ANI10: 0 to +5 V
INTTA0CC1 trigger timing: 1 μs after the TAB0 valley interrupt (INTTB0OV) of the carrier cycle
A/D conversion completion time: 2 μs

(e) On-chip debug function

The on-chip debug function of the V850E/IG3 (μPD70F3454GC-8EA-A) can be realized in the following two ways.

- Debugging using DCU (debug control unit) (using MINICUBE)
  By using the $\overline{\text{DRST}}$, DCK, DMS, DDI, and DDO pins as debug interface pins, on-chip debugging is realized by the internal DCU of the V850E/IG3.

- Debugging without using DCU (using MINICUBE2)
  On-chip debugging is realized by MINICUBE2 without using the DCU but by using the user resources.

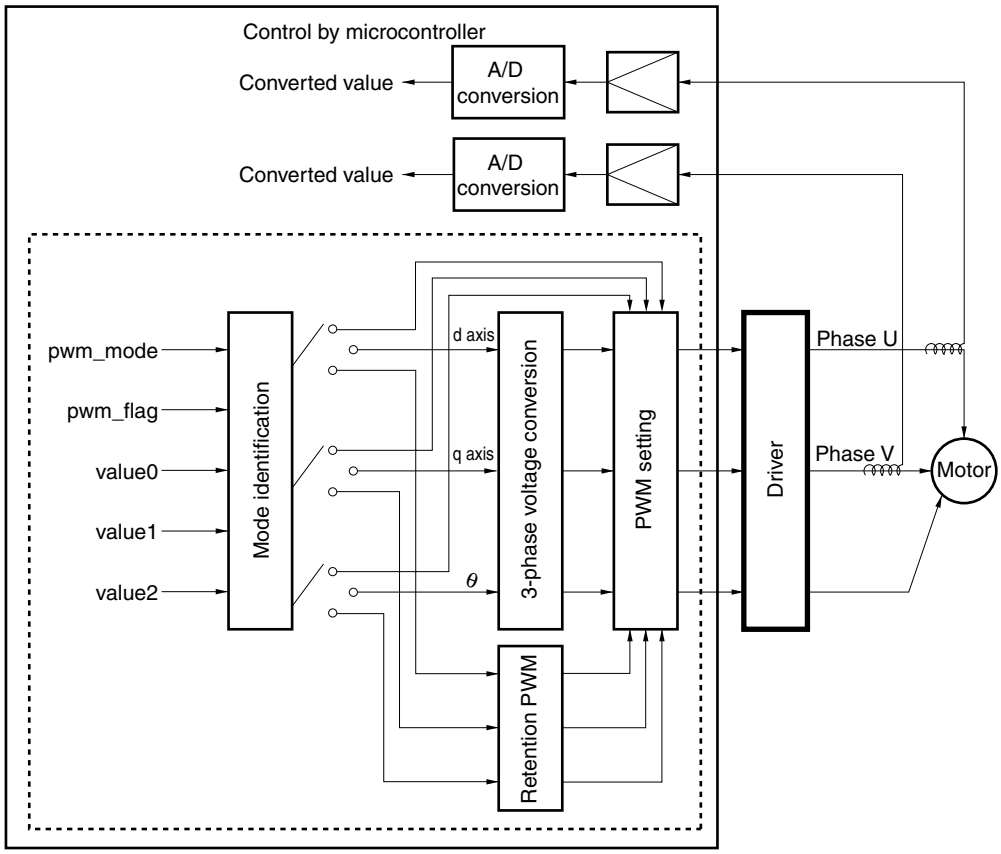
For how to connect to the on-chip debug emulator (MINICUBE, MINICUBE2), refer to the manual of the debugger used.

CHAPTER 2 CONTROL METHOD

2.1 Control Block

The control block diagram of the 3-phase PWM driver is shown below.

Figure 2-1. 3-Phase PWM Driver Control Block Diagram



Remark Processing enclosed by broken lines indicates the processing by software.
Processing of the driver, denoted by a heavy solid line, varies depending on the driving motor used, so the driver should be designed by users.

(1) Mode identification

Mode of the 3-phase PWM driver can be identified in accordance with the software state.

Modes of the 3-phase PWM driver are as follows.

- Direct mode: PWM duty ratio set by value0 to value2 is used as the PWM voltage.
- dq conversion mode: PWM voltage is determined by d axis voltage, q axis voltage, and rotation position (θ).
- Output lock mode: PWM voltage previously set by the 3-phase PWM driver is output.

(2) 3-phase voltage conversion

Coordinate transformation processing is performed in the dq conversion mode.

(3) Retention PWM

PWM voltage previously set by the 3-phase PWM driver is retained.

(4) PWM setting

PWM voltage is calculated and output to registers of the V850E/IG3 (μPD70F3454GC-8EA-A).

2.2 3-Phase Voltage Conversion

The following shows the formula to convert the dq axes voltage into the 3-phase coordinate.

Phase U voltage = (d axis voltage $\times$ sin(θ + 90°)) − (q axis voltage × sin(θ))
Phase V voltage = (d axis voltage × sin(θ + 330°)) − (q axis voltage × sin(θ + 240°))
Phase W voltage = −Phase U voltage − Phase V voltage

2.3 Register Settings

(1) System wait control register (VSWC)

The VSWC register is set as follows.

VSWC register = 13H

VSWC — Address: FFFFF06EH

	7	6	5	4	3	2	1	0
After reset	0	1	1	1	0	1	1	1
Bit name	–	–	–	–	–	–	–	–
Set value	0	0	0	1	0	0	1	1

Wait for bus access to the on-chip peripheral I/O register
4 waits in 64 MHz operation

Caution Set the VSWC register by using the startup routine (ig3_start.s).

(2) PLL control register (PLLCTL)

The PLLCTL register is set as follows.

PLLCTL register = 03H

PLLCTL — Address: FFFFF82CH

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	1
Bit name	0	0	0	0	0	0	SELPLL	1
Set value	0	0	0	0	0	0	1	1

SELPLL	CPU operation clock selection
1	PLL mode

Caution Be sure to set bits 7 to 2 to “0” and set bit 0 to “1”.

(3) Processor clock control register (PCC)

The PCC register is set as follows.

PCC register = 00H

PCC — Address: FFFFF828H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	1	1
Bit name	0	0	0	0	0	0	CK1	CK0
Set value	0	0	0	0	0	0	0	0

CK1	CK0	Clock selection (f_{CLK}/f_{CPU})
0	0	f_{XX}

Cautions 1. The PCC register is a special register. Data can be written to this register only in a combination of specific sequences. For details, refer to 3.4.8 Special registers in the V850E/IF3, V850E/IG3 Hardware User's Manual (U18279E).

2. Be sure to set bits 2 to 7 to "0".

3. Set the PCC register after the PLL mode is selected (PLLCTL.SELPLL bit = 1).

(4) Power save control register (PSC)

The PSC register is set as follows.

PSC register = 00H

PSC — Address: FFFFF1FEH

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	0	INTM	0	0	STB	0
Set value	0	0	0	0	0	0	0	0

INTM	Standby mode control by maskable interrupt request (INTxx[Note])
0	Standby mode release by INTxx request enabled

STB	Operation mode selection
0	Normal mode

Note For details, see **Table 20-1 Interrupt Source List** in the **V850E/IF3, V850E/IG3 Hardware User's Manual (U18279E)**.

Cautions 1. The PSC register is a special register. Data can be written to this register only in a combination of specific sequences. For details, refer to 3.4.8 Special registers in the V850E/IF3, V850E/IG3 Hardware User's Manual (U18279E).

2. Be sure to set bits 0, 2, 3, and 5 to 7 to "0".

(5) Power save mode register (PSMR)

The PSMR register is set as follows.

PSMR register = 00H

PSMR — Address: FFFFF820H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	0	0	0	0	0	PSM0
Set value	0	0	0	0	0	0	0	0

PSM0	Operation specification in software standby mode
0	IDLE mode

Cautions 1. Be sure to set bits 1 to 7 to "0".

2. The PSM0 bit is valid only when the PSC.STB bit is 1.

(6) Oscillation stabilization time select register (OSTS)

The OSTS register is set as follows.

OSTS register = 04H

OSTS — Address: FFFFF6C0H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	1	0	0
Bit name	0	0	0	0	OSTS3	OSTS2	OSTS1	OSTS0
Set value	0	0	0	0	0	1	0	0

OSTS3	OSTS2	OSTS1	OSTS0	Selection of oscillation stabilization time (f_X = 8 MHz)
0	1	0	0	$2^{14}/f_X$ (2.05 ms)

Caution Be sure to set bits 4 to 7 to "0".

(7) Clock monitor mode register (CLM)

The CLM register is set as follows.

CLM register = 00H

CLM — Address: FFFFF870H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	0	0	0	0	0	CLME
Set value	0	0	0	0	0	0	0	0

CLME	Clock monitor operation control
0	Clock monitor operation disabled

Caution The CLM register is a special register. Data can be written to this register only in a combination of specific sequences. For details, refer to 3.4.8 Special registers in the V850E/IF3, V850E/IG3 Hardware User's Manual (U18279E).

(8) Port 1 mode control register (PMC1)

The PMC1 register is set as follows.

PMC1 register = 3FH

PMC1 — Address: FFFFF442H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	PMC17	PMC16	PMC15	PMC14	PMC13	PMC12	PMC11	PMC10
Set value	0	0	1	1	1	1	1	1

PMC17	Specification of operating mode of P17 pin
0	I/O port

PMC16	Specification of operating mode of P16 pin
0	I/O port

PMC15	Specification of operating mode of P15 pin
1	TOB0B3 output/TRGB0 input/A5 output

PMC14	Specification of operating mode of P14 pin
1	TOB0T3 output/EVTB0 input/A4 output

PMC13	Specification of operating mode of P13 pin
1	TOB0B2 output/TIB00 input/A3 output

PMC12	Specification of operating mode of P12 pin
1	TOB0T2 output/TIB03 input/TOB03 output/A2 output

PMC11	Specification of operating mode of P11 pin
1	TOB0B1 output/TIB02 input/TOB02 output/A1 output

PMC10	Specification of operating mode of P10 pin
1	TOB0T1 output/TIB01 input/TOB01 output/A0 output

(9) Port 1 function control register (PFC1), port 1 function control expansion register (PFCE1)

The PFC1 and PFCE1 registers are set as follows.

PFC1 register = 00H

PFCE1 register = 00H

PFCE1 Address: FFFFF702H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	PFCE15	PFCE14	PFCE13	PFCE12	PFCE11	PFCE10
Set value	0	0	0	0	0	0	0	0

PFC1 Address: FFFFF462H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	PFC15	PFC14	PFC13	PFC12	PFC11	PFC10
Set value	0	0	0	0	0	0	0	0

PFCE15	PFC15	Specification of alternate function of P15 pin
0	0	TOB0B3 output

PFCE14	PFC14	Specification of alternate function of P14 pin
0	0	TOB0T3 output

PFCE13	PFC13	Specification of alternate function of P13 pin
0	0	TOB0B2 output

PFCE12	PFC12	Specification of alternate function of P12 pin
0	0	TOB0T2 output

PFCE11	PFC11	Specification of alternate function of P11 pin
0	0	TOB0B1 output

PFCE10	PFC10	Specification of alternate function of P10 pin
0	0	TOB0T1 output

(10) Pull-up resistor option register 1 (PU1)

The PU1 register is set as follows.

PU1 register = 00H

PU1 Address: FFFFFC42H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	PU17	PU16	PU15	PU14	PU13	PU12	PU11	PU10
Set value	0	0	0	0	0	0	0	0

PU1n	Control of on-chip pull-up resistor connection (n = 0 to 7)
0	No connection

(11) TAA0 control register 0 (TAA0CTL0)

The TAA0CTL0 register is set as follows.

TAA0CTL0 register = 01H/81H

TAA0CTL0 Address: FFFFF660H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	TAA0CE	0	0	0	0	TAA0CKS2	TAA0CKS1	TAA0CKS0
Set value	0/1	0	0	0	0	0	0	1

TAA0CE	TAA0 operation control
0	TAA0 operation disabled (TAA0 reset asynchronously[Note]).
1	TAA0 operation enabled. TAA0 operation started.

TAA0CKS2	TAA0CKS1	TAA0CKS0	Internal count clock selection
0	0	1	$f_{XX}/2$

Note The TAA0OPT0.TAA0OVF bit and 16-bit counter are reset simultaneously.

Caution Be sure to set bits 3 to 6 to "0".

(12) TAA0 control register 1 (TAA0CTL1)

The TAA0CTL1 register is set as follows.

TAA0CTL1 register = 85H

TAA0CTL1 Address: FFFFF661H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	TAA0SYE	0	0	0	0	TAA0MD2	TAA0MD1	TAA0MD0
Set value	1	0	0	0	0	1	0	1

TAA0SYE	Operation mode selection
1	Tuning operation mode

TAA0MD2	TAA0MD1	TAA0MD0	Timer mode selection
1	0	1	Free-running timer mode

Caution Be sure to set bits 3 and 6 to “0”.

(13) TAA2 I/O control register 0 (TAA2IOC0)

The TAA2IOC0 register is set as follows.

TAA2IOC0 register = 00H

TAA2IOC0 Address: FFFFF6A2H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	0	0	TAA2OL1	TAA2OE1	TAA2OL0	TAA2OE0
Set value	0	0	0	0	0	0	0	0

TAA2OL1	TOA21 pin output level setting
0	TOA21 pin starts output at high level.

TAA2OE1	TOA21 pin output setting
0	Timer output prohibited • Low level is output from the TOA21 pin.

TAA2OL0	TOA20 pin output level setting
0	TOA20 pin starts output at high level.

TAA2OE0	TOA20 pin output setting
0	Timer output prohibited • Low level is output from the TOA20 pin.

(14) TAA2 I/O control register 1 (TAA2IOC1)

The TAA2IOC1 register is set as follows.

TAA2IOC1 register = 00H

TAA2IOC1 Address: FFFFF6A3H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	0	0	TAA2IS3	TAA2IS2	TAA2IS1	TAA2IS0
Set value	0	0	0	0	0	0	0	0

TAA2IS3	TAA2IS2	Capture trigger input signal (TIA21 pin) valid edge setting
0	0	No edge detection (capture operation invalid)

TAA2IS1	TAA2IS0	Capture trigger input signal (TIA20 pin) valid edge setting
0	0	No edge detection (capture operation invalid)

(15) TAA2 I/O control register 2 (TAA2IOC2)

The TAA2IOC2 register is set as follows.

TAA2IOC2 register = 00H

TAA2IOC2 Address: FFFFF6A4H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	0	0	TAA2EES1	TAA2EES0	TAA2ETS1	TAA2ETS0
Set value	0	0	0	0	0	0	0	0

TAA2EES1	TAA2EES0	External event count input signal (TIA20 pin) valid edge setting
0	0	No edge detection (external event count invalid)

TAA2ETS1	TAA2ETS0	External trigger input signal (TIA20 pin) valid edge setting
0	0	No edge detection (external trigger invalid)

(16) TAA0 option register 0 (TAAOPT0)

The TAA0OPT0 register is set as follows.

TAA0OPT0 register = 00H

TAA0OPT0 Address: FFFFF665H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	0	0	0	0	0	TAA0OVF
Set value	0	0	0	0	0	0	0	0

TAA0OVF	TAA0 overflow detection flag
Reset (0)	0 written to TAA0OVF bit or TAA0CTL0.TAA0CE bit = 0

Caution Be sure to set bits 1 to 7 to “0”.

(17) TAA0 capture/compare register 0 (TAA0CCR0)

The TAA0CCR0 register is set as follows.

TAA0CCR0 register = 0020H

TAA0CCR0 Address: FFFFF666H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit name	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Set value	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Compare register value setting
TAA0 A/D converter 0 conversion start trigger value setting (compare match occurs 1 μs later)

(18) TAA0 capture/compare register 1 (TAA0CCR1)

The TAA0CCR1 register is set as follows.

TAA0CCR1 register = 0020H

TAA0CCR1 Address: FFFFF668H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit name	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Set value	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Compare register value setting
TAA0 A/D converter 1 conversion start trigger value setting (compare match occurs 1 μs later)

(19) TAB0 control register 0 (TAB0CTL0)

The TAB0CTL0 register is set as follows.

TAB0CTL0 register = 01H/81H

TAB0CTL0 Address: FFFFF5E0H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	TAB0CE	0	0	0	0	TAB0CKS2	TAB0CKS1	TAB0CKS0
Set value	0/1	0	0	0	0	0	0	1

TAB0CE	TAB0 operation control
0	TAB0 operation disabled (TAB0 reset asynchronously[Note]).
1	TAB0 operation enabled. TAB0 operation started.

TAB0CKS2	TAB0CKS1	TAB0CKS0	Internal count clock selection
0	0	1	$f_{XX}/2$

Note The TAB0OPT0.TAB0OVF bit and 16-bit counter are reset simultaneously. Moreover, timer outputs (TOB00 to TOB03 pins) are reset to the TAB0IOC0 register set status at the same time as the 16-bit counter.

Caution Be sure to set bits 3 to 6 to "0".

(20) TAB0 control register 1 (TAB0CTL1)

The TAB0CTL1 register is set as follows.

TAB0CTL1 register = 07H

TAB0CTL1 Address: FFFFF5E1H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	TAB0EST	TAB0EEE	0	0	TAB0MD2	TAB0MD1	TAB0MD0
Set value	0	0	0	0	0	1	1	1

TAB0EST	Software trigger control
0	No software trigger operation

TAB0EEE	Count clock selection
0	Disables operation with external event count input (EVTB0 pin). Perform counting with the count clock selected by the TAB0CTL0.TAB0CKS0 to TAB0CTL0.TAB0CKS2 bits.)

TAB0MD2	TAB0MD1	TAB0MD0	Timer mode selection
1	1	1	6-phase PWM output mode

Caution Be sure to set bits 3, 4, and 7 to "0".

(21) TAB0 I/O control register 0 (TAB0IOC0)

The TAB0IOC0 register is set as follows.

TAB0IOC0 register = 55H

TAB0IOC0 Address: FFFFF5E2H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	TAB0OL3	TAB0OE3	TAB0OL2	TAB0OE2	TAB0OL1	TAB0OE1	TAB0OL0	TAB0OE0
Set value	0	1	0	1	0	1	0	1

TAB0OLm	Output level setting of TOB0m and TOB0Tb pins (m = 0 to 3, b = 1 to 3)
0	TOB0m and TOB0Tb pins start output at high level.

TAB0OEm	Output setting of TOB0m and TOB0Tb pins (m = 0 to 3, b = 1 to 3)
1	Timer output enabled (A pulse is output from the TOB0m and TOB0Tb pins.)

(22) TAB0 I/O control register 1 (TAB0IOC1)

The TAB0IOC1 register is set as follows.

TAB0IOC1 register = 00H

TAB0IOC1 Address: FFFFF5E3H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	TAB0IS7	TAB0IS6	TAB0IS5	TAB0IS4	TAB0IS3	TAB0IS2	TAB0IS1	TAB0IS0
Set value	0	0	0	0	0	0	0	0

TAB0IS7	TAB0IS6	Capture trigger input signal (TIB03 pin) valid edge setting
0	0	No edge detection (capture operation invalid)

TAB0IS5	TAB0IS4	Capture trigger input signal (TIB02 pin) valid edge setting
0	0	No edge detection (capture operation invalid)

TAB0IS3	TAB0IS2	Capture trigger input signal (TIB01 pin) valid edge setting
0	0	No edge detection (capture operation invalid)

TAB0IS1	TAB0IS0	Capture trigger input signal (TIB00 pin) valid edge setting
0	0	No edge detection (capture operation invalid)

(23) TAB0 I/O control register 2 (TAB0IOC2)

The TAB0IOC2 register is set as follows.

TAB0IOC2 register = 00H

TAB0IOC2 Address: FFFFF5E4H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	0	0	TAB0EES1	TAB0EES0	TAB0ETS1	TAB0ETS0
Set value	0	0	0	0	0	0	0	0

TAB0EES1	TAB0EES0	External event count input signal (EVTB0 pin) valid edge setting
0	0	No edge detection (external event count invalid)

TAB0ETS1	TAB0ETS0	External trigger input signal (TRGB0 pin) valid edge setting
0	0	No edge detection (external trigger invalid)

(24) TAB0 option register 0 (TAB0OPT0)

The TAB0OPT0 register is set as follows.

TAB0OPT0 register = 00H

TAB0OPT0 Address: FFFFF5E5H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	TAB0CCS3	TAB0CCS2	TAB0CCS1	TAB0CCS0	0	TAB0CMS	TAB0CUF	TAB0OVF
Set value	0	0	0	0	0	0	0	0

TAB0CCSm	TAB0CCRm register capture/compare selection (m = 0 to 3)
0	Compare register selected

TAB0CMS	Compare register rewrite mode selection
0	Batch rewrite mode specified (transfer operation specified)

TAB0CUF	Timer AB0 count up/down flag
0	Timer AB0 is counting up.

TAB0OVF	TAB0 overflow flag
Reset (0)	0 written to TAB0OVF bit or TAB0CTL0.TAB0CE bit = 0

Caution Be sure to set bit 3 to “0”.

(25) TAB0 capture/compare register 0 (TAB0CCR0)

The TAB0CCR0 register is set as follows.

TAB0CCR0 register = 031FH

TAB0CCR0 Address: FFFFF5E6H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit name	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Set value	0	0	0	0	0	0	1	1	0	0	0	1	1	1	1	1

Compare register value setting
50 μs, 799 counts

(26) TAB0 capture/compare register 1 (TAB0CCR1)

The TAB0CCR1 register is set as follows.

TAB0CCR1 register = 0320H

TAB0CCR1 Address: FFFFF5E8H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit name	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Set value	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0

Compare register value setting
800 counts

(27) TAB0 capture/compare register 2 (TAB0CCR2)

The TAB0CCR2 register is set as follows.

TAB0CCR2 register = 0320H

TAB0CCR2 Address: FFFFF5EAH

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit name	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Set value	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0

Compare register value setting
800 counts

(28) TAB0 capture/compare register 3 (TAB0CCR3)

The TAB0CCR3 register is set as follows.

TAB0CCR3 register = 0320H

TAB0CCR3 Address: FFFFF5ECH

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit name	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Set value	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0

Compare register value setting
800 counts

(29) TAB0 option register 1 (TAB0OPT1)

The TAB0OPT1 register is set as follows.

TAB0OPT1 register = 40H

TAB0OPT1 Address: FFFFF600H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	TAB0ICE	TAB0IOE	0	TAB0ID4	TAB0ID3	TAB0ID2	TAB0ID1	TAB0ID0
Set value	0	1	0	0	0	0	0	0

TAB0ICE	Crest interrupt (INTTB0CC0 signal) enable
0	Do not use INTTB0CC0 signal (do not use it as count signal for interrupt culling).

TAB0IOE	Valley interrupt (INTTB0OV signal) enable
1	Use INTTB0OV signal (use it as count signal for interrupt culling).

TAB0ID4	TAB0ID3	TAB0ID2	TAB0ID1	TAB0ID0	Number of times of interrupt
0	0	0	0	0	Not culled (all interrupts are output)

(30) TAB0 option register 2 (TAB0OPT2)

The TAB0OPT2 register is set as follows.

TAB0OPT2 register = 85H

TAB0OPT2 Address: FFFFF601H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	TAB0RDE	TAB0DTM	TAB0ATM3	TAB0ATM2	TAB0AT3	TAB0AT2	TAB0AT1	TAB0AT0
Set value	1	0	0	0	0	1	0	1

TAB0RDE	Transfer culling enable
1	Culls transfer at the same interval as interrupt culling set by the TAB0OPT1 register.

TAB0DTM	Dead-time counter operation mode selection (m = 1 to 3)
0	Dead-time counter counts up normally and, if TOB0m output of TAB0 is at a narrow interval (TOB0m output width < dead-time width), the dead-time counter is cleared and counts up again.

TAB0ATM3	TAB0ATM3 mode selection
0	Outputs A/D trigger signal (TABTADT00) for INTTA0CC1 interrupt while dead-time counter is counting up.

TAB0ATM2	TAB0ATM2 mode selection
0	Outputs A/D trigger signal (TABTADT00) for INTTA0CC0 interrupt while dead-time counter is counting up.

TAB0AT3	A/D trigger output control 3
0	Disables output of A/D trigger signal (TABTADT00) for INTTA0CC1 interrupt.

TAB0AT2	A/D trigger output control 2
1	Enables output of A/D trigger signal (TABTADT00) for INTTA0CC0 interrupt.

TAB0AT1	A/D trigger output control 1
0	Disables output of A/D trigger signal (TABTADT00) for INTTB0CC0 (crest interrupt).

TAB0AT0	A/D trigger output control 0
1	Enables output of A/D trigger signal (TABTADT00) for INTTB0OV (valley interrupt).

(31) TAB0 option register 3 (TAB0OPT3)

The TAB0OPT3 register is set as follows.

TAB0OPT3 register = 05H

TAB0OPT3 Address: FFFFF603H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	TAB0ATM7	TAB0ATM6	TAB0AT7	TAB0AT6	TAB0AT5	TAB0AT4
Set value	0	0	0	0	0	1	0	1

TAB0ATM7	TAB0ATM7 mode selection
0	Outputs A/D trigger signal (TABTADT01) of INTTA0CC1 interrupt while dead-time counter is counting up.

TAB0ATM6	TAB0ATM6 mode selection
0	Outputs A/D trigger signal (TABTADT01) of INTTA0CC0 interrupt while dead-time counter is counting up.

TAB0AT7	A/D trigger output control 3
0	Disables output of A/D trigger signal (TABTADT01) for INTTA0CC1 interrupt.

TAB0AT6	A/D trigger output control 2
1	Enables output of A/D trigger signal (TABTADT01) for INTTA0CC0 interrupt.

TAB0AT5	A/D trigger output control 1
0	Disables output of A/D trigger signal (TABTADT01) for INTTB0CC0 interrupt (crest interrupt).

TAB0AT4	A/D trigger output control 0
1	Enables output of A/D trigger signal (TABTADT01) for INTTB0OV interrupt (valley interrupt).

(32) TAB0 I/O control register 3 (TAB0IOC3)

The TAB0IOC3 register is set as follows.

TAB0IOC3 register = FCH

TAB0IOC3 — Address: FFFFF602H

	7	6	5	4	3	2	1	0
After reset	1	0	1	0	1	0	0	0
Bit name	TAB0OLB3	TAB0OEB3	TAB0OLB2	TAB0OEB2	TAB0OLB1	TAB0OEB1	0	0
Set value	1	1	1	1	1	1	0	0

TAB0OLBm	Setting of TOB0Bm pin output level (m = 1 to 3)
1	Enables inversion of output of TOB0Bm pin.

TAB0OEBm	Setting of TOB0Bm pin output (m = 1 to 3)
1	Enables TOB0Bm pin output.

(33) TAB0 dead-time compare register (TAB0DTC)

The TAB0DTC register is set as follows.

TAB0DTC register = 0080H

TAB0DTC — Address: FFFFF604H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit name	0	0	0	0	0	0	TAB0 DTC9	TAB0 DTC8	TAB0 DTC7	TAB0 DTC6	TAB0 DTC5	TAB0 DTC4	TAB0 DTC3	TAB0 DTC2	TAB0 DTC1	TAB0 DTC0
Set value	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Dead-time value specification
4 μs

(34) High-impedance output control register 00 (HZA0CTL0)

The HZA0CTL0 register is set as follows.

HZA0CTL0 register = 80H/88H

HZA0CTL0 Address: FFFFF610H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	HZA0DCE0	HZA0DCM0	HZA0DCN0	HZA0DCP0	HZA0DCT0	HZA0DCC0	0	HZA0DCF0
Set value	1	0	0	0	0/1	0	0	0

HZA0DCE0	High-impedance output control
1	Enables high-impedance output control operation.

HZA0DCM0	Condition of clearing high-impedance state by HZA0DCC0 bit
0	Setting of the HZA0DCC0 bit is valid regardless of the TOB0OFF pin input.

HZA0DCN0	HZA0DCP0	TOB0OFF pin input edge specification
0	0	No valid edge (setting the HZA0DCF0 bit by TOB0OFF pin input is prohibited).

HZA0DCT0	High-impedance output trigger bit
0	No operation
1	Pins are made to go into a high-impedance state by software and the HZA0DCF0 bit is set to 1.

HZA0DCC0	High-impedance output control clear bit
0	No operation

HZA0DCF0	High-impedance output status flag
0	Indicates that output of the target pin is enabled. • This bit is cleared to 0 when the HZA0DCE0 bit = 0. • This bit is cleared to 0 when the HZA0DCC0 bit = 1.

(35) A/D converter n scan mode register (ADnSCM)

The ADnSCM register is set as follows.

ADnSCM register = 0180H/8180H

ADnSCM (n = 0, 1) — Address: AD0SCM FFFFF220H, AD1SCM FFFFF2A0H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit name	ADnCE	ADnCS	0	0	0	ADnPLM	ADnTRG1	ADnTRG0	ADnPS	0	0	0	0	0	0Note	0
Set value	0/1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0

ADnCE	A/D conversion operation control
0	Stops conversion operation.
1	Enables conversion operation.

ADnCS	Status of A/D converter n
0	A/D conversion stopped

ADnPLM	ADnTRG1	ADnTRG0	Normal operation mode specification
0	0	1	Hardware trigger mode

ADnPS	A/D power save mode specification
1	A/D operational mode

Note When using A/D converters 0 and 1, be sure to set bit 1 to "1".
This setting can be performed at the same time as other ADnSCM register bits.

Caution Be sure to set bits 0 to 6 and 11 to 13 to “0”.

(36) A/D converter n clock select register (ADnOCKS)

The ADnOCKS register is set as follows.

ADnOCKS register = 12H

ADnOCKS (n = 0, 1) — Address: AD0OCKS FFFFF270H, AD1OCKS FFFFF274H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	0	ADnOCKSEN	0	0	ADnOCKS1	ADnOCKS0
Set value	0	0	0	1	0	0	1	0

ADnOCKSEN	Clock operation control
1	Enables operation clock supply of A/D converter n.

ADnOCKS1	ADnOCKS0	Input clock selection of A/D converter n (f_{AD01})
1	0	$f_{XX}/4$ (when f_{XX} = 64 MHz)

Cautions 1. Set f_{AD01} to 16 MHz or lower.

2. When A/D converter n is used, be sure to set the ADnOCKS register and set the ADnSCM.ADnPS bit to 1, as well as to read the A/D conversion result register.

3. Be sure to set bits 2, 3, and 5 to 7 to "0".

(37) A/D converter n conversion time control register (ADnCTC)

The ADnCTC register is set as follows.

ADnCTC register = 0CH

ADnCTC (n = 0, 1) — Address: AD0CTC FFFFF222H, AD1CTC FFFFF2A2H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	0	0	ADnFR3	ADnFR2	ADnFR1	ADnFR0
Set value	0	0	0	0	1	1	0	0

ADnFR3	ADnFR2	ADnFR0	ADnFR0	Specification of number of conversion clocks
1	1	0	0	Number of conversion clocks = 32 (conversion time = 2.00 μs)

Caution Be sure to set bits 4 to 7 to "0".

(38) A/D converter n conversion channel specification register (ADnCHEN)

The ADnCHEN register is set as follows.

ADnCHEN register = 0001H

ADnCHEN (n = 0, 1) — Address: AD0CHEN FFFFF224H, AD1CHEN FFFFF2A4H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit name	ADn CHEN 15	ADn CHEN 14	ADn CHEN 13	ADn CHEN 12	ADn CHEN 11	ADn CHEN 10	ADn CHEN 9	ADn CHEN 8	ADn CHEN 7	ADn CHEN 6	ADn CHEN 5	ADn CHEN 4	ADn CHEN 3	ADn CHEN 2	ADn CHEN 1	ADn CHEN 0
Set value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

ADnCHEN0	Specification of analog input pin
1	Enables specification of ANIn0 pin.

(39) A/D converter n control register (ADnCTL0)

The ADnCTL0 register is set as follows.

ADnCTL0 register = 00H

ADnCTL0 (n = 0, 1) — Address: AD0CTL0 FFFFF230H, AD1CTL0 FFFFF2B0H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	0	0	0	0	ADnMD1	ADnMD0
Set value	0	0	0	0	0	0	0	0

ADnMD1	ADnMD0	Specification of extended operating mode
0	0	Normal operating mode

(40) A/D converter n trigger select register (ADnTSEL)

The ADnTSEL register is set as follows.

AD0TSEL register = 11H

AD1TSEL register = 13H

ADnTSEL (n = 0, 1) Address: AD0TSEL FFFFF231H, AD1TSEL FFFFF2B1H

	7	6	5	4	3	2	1	0
After reset	0	0	0	1	0	0	0	0
Bit name	0	0	0	1	0	0	ADn TRGSEL11	ADn TRGSEL10
Set value	0	0	0	1	0	0	0/1	1

AD0TRGSEL11	AD0TRGSEL10	In hardware trigger mode: Trigger specification
0	1	ITRG2

AD1TRGSEL11	AD1TRGSEL10	In hardware trigger mode: Trigger specification
1	1	ITRG4

(41) Operational amplifier n control register 0 (OPnCTL0)

The OPnCTL0 register is set as follows.

OPnCTL0 register = 00H

OP0CTL0 Address: FFFFF260H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	0	OP0EN	OP0GA3	OP0GA2	OP0GA1	OP0GA0
Set value	0	0	0	0	0	0	0	0

OP1CTL0 Address: FFFFF2E0H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	OP12EN	OP11EN	OP10EN	OP1GA3	OP1GA2	OP1GA1	OP1GA0
Set value	0	0	0	0	0	0	0	0

OP12EN	Operation control of operational amplifier 2
0	Operation disabled (not used)

OP11EN	Operation control of operational amplifier 1
0	Operation disabled (not used)

OP0EN	Operation control of operational amplifier 0
0	Operation disabled (not used)

OP10EN	Operation control of operational amplifier 0
0	Operation disabled (not used)

OPnGA3	OPnGA2	OPnGA1	OPnGA0	Gain specification of operational amplifier
0	0	0	0	×2.500

Caution Be sure to set bits 5 to 7 of the OP0CTL0 register and bit 7 of the OP1CTL0 register to “0”.

(42) Comparator n control register 0 (CMPnCTL0)

The CMPnCTL0 register is set as follows.

CMPnCTL0 register = 00H

CMP0CTL0 Address: FFFFF261H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	0	CMP0FEN	0	0	0	CMP0LEN
Set value	0	0	0	0	0	0	0	0

CMP1CTL0 Address: FFFFF2E1H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	CMP12FEN	CMP11FEN	CMP10FEN	0	CMP12LEN	CMP11LEN	CMP10LEN
Set value	0	0	0	0	0	0	0	0

CMP12FEN	Operation control of comparator 2 (full range)
0	Operation disabled (not used)

CMP11FEN	Operation control of comparator 1 (full range)
0	Operation disabled (not used)

CMP0FEN	Operation control of comparator 0 (full range)
0	Operation disabled (not used)

CMP10FEN	Operation control of comparator 0 (full range)
0	Operation disabled (not used)

CMP12LEN	Operation control of comparator 2 (low range)
0	Operation disabled (not used)

CMP11LEN	Operation control of comparator 1 (low range)
0	Operation disabled (not used)

CMP0LEN	Operation control of comparator 0 (low range)
0	Operation disabled (not used)

CMP10LEN	Operation control of comparator 0 (low range)
0	Operation disabled (not used)

Caution Be sure to set bits 1 to 3, and 5 to 7 of the CMP0CTL0 register and bits 3 and 7 of the CMP1CTL0 register to “0”.

(43) Comparator n control register 2 (CMPnCTL2)

The CMPnCTL2 register is set as follows.

CMPnCTL2 register = 00H

CMP0CTL2 Address: FFFFF263H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	0	0	0	0	0	CMP0SEL
Set value	0	0	0	0	0	0	0	0

CMP1CTL2 Address: FFFFF2E3H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	0	0	0	CMP12SEL	CMP11SEL	CMP10SEL
Set value	0	0	0	0	0	0	0	0

CMP12SEL	Specification of compare signal of comparator 2
0	Before operational amplifier 2 amplification

CMP11SEL	Specification of compare signal of comparator 1
0	Before operational amplifier 1 amplification

CMP0SEL	Specification of compare signal of comparator 0
0	Before operational amplifier 0 amplification

CMP10SEL	Specification of compare signal of comparator 0
0	Before operational amplifier 0 amplification

Caution Be sure to set bits 1 to 7 of the CMP0CTL2 register and bits 3 to 7 of the CMP1CTL2 register to “0”.

(44) Comparator n control register 3 (CMPnCTL3)

The CMPnCTL3 register is set as follows.

CMPnCTL3 register = 00H

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CMP0CTL3 Address: FFFFF264H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	CMP0FDS	0	0	CMP0FDE	CMP0LDS	0	0	CMP0LDE
Set value	0	0	0	0	0	0	0	0

CMP1CTL3 Address: FFFFF2E4H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	CMP1FDS	CMP12FDE	CMP11FDE	CMP10FDE	CMP1LDS	CMP12LDE	CMP11LDE	CMP10LDE
Set value	0	0	0	0	0	0	0	0

CMPnFDS	Specification of output generation of comparator (full range)
0	Logical product (AND) detection

CMP12FDE	Edge detection control of comparator 2 (full range)
0	Edge detection disabled

CMP11FDE	Edge detection control of comparator 1 (full range)
0	Edge detection disabled

CMP0FDE	Edge detection control of comparator 0 (full range)
0	Edge detection disabled

CMP10FDE	Edge detection control of comparator 0 (full range)
0	Edge detection disabled

CMPnLDS	Specification of output generation of comparator (low range)
0	Logical product (AND) detection

CMP12LDE	Edge detection control of comparator 2 (low range)
0	Edge detection disabled

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CMP11LDE	Edge detection control of comparator 1 (low range)
0	Edge detection disabled

CMP0LDE	Edge detection control of comparator 0 (low range)
0	Edge detection disabled

CMP10LDE	Edge detection control of comparator 0 (low range)
0	Edge detection disabled

(45) Comparator output digital noise elimination registers nL, nF (CMPNFCnL, CMPNFCnF)

The CMPNFCnL and CMPNFCnF registers are set as follows.

CMPNFCnL register = 00H

CMPNFCnF register = 00H

CMPNFCnL (n = 0, 1) Address: CMPNFC0L FFFFF278H, CMPNFC1L FFFFF27CH

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	CMPnNFEN	0	0	0	0	CMPnNFC2	CMPnNFC1	CMPnNFC0
Set value	0	0	0	0	0	0	0	0

CMPNFCnF (n = 0, 1) Address: CMPNFC0F FFFFF27AH, CMPNFC1F FFFFF27EH

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	CMPnNFEN	0	0	0	0	CMPnNFC2	CMPnNFC1	CMPnNFC0
Set value	0	0	0	0	0	0	0	0

CMPnNFEN	Setting of digital noise elimination
0	Does not perform digital noise elimination (through)

CMPnNFC2	CMPnNFC1	CMPnNFC0	Sampling clock selection
0	0	0	f_{XX}/32

Caution Be sure to set bits 3 to 6 to “0”.

(46) A/D trigger rising edge, falling edge specification registers (ADTR, ADTF)

The ADTR and ADTF registers are set as follows.

ADTR register = 00H

ADTF register = 00H

ADTR — Address: FFFFF2F2H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	0	0	0	0	ADTR1	ADTR0
Set value	0	0	0	0	0	0	0	0

ADTF — Address: FFFFF2F0H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	0	0	0	0	ADTF1	ADTF0
Set value	0	0	0	0	0	0	0	0

ADTFn	ADTRn	Valid edge specification
0	0	No edge detected

(47) Comparator output interrupt rising edge, falling edge specification registers (CMPOR, CMPOF)

The CMPOR and CMPOF registers are set as follows.

CMPOR register = 00H

CMPOF register = 00H

CMPOR Address: FFFFF2F6H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	0	0	CMPOR1F	CMPOR1L	CMPOR0F	CMPOR0L
Set value	0	0	0	0	0	0	0	0

CMPOF Address: FFFFF2F4H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	0	0	0	0	CMPOF1F	CMPOF1L	CMPOF0F	CMPOF0L
Set value	0	0	0	0	0	0	0	0

CMPOFnF	CMPORnF	Valid edge specification
0	0	No edge detected

CMPOFnL	CMPORnL	Valid edge specification
0	0	No edge detected

(48) Digital noise elimination 0 control register n (INTNFCn)

The INTNFCn register is set as follows.

INTNFCn register = 00H

INTNFCn (n = 14 to 16)

Address: INTNFC14 FFFFF310H, INTNFC15 FFFFF312H, INTNFC16 FFFFF314H

	7	6	5	4	3	2	1	0
After reset	0	0	0	0	0	0	0	0
Bit name	INTNFENn	0	0	0	0	INTNFCn2	INTNFCn1	INTNFCn0
Set value	0	0	0	0	0	0	0	0

INTNFENn	Setting of digital noise elimination
0	Digital noise elimination disabled

INTNFCn2	INTNFCn1	INTNFCn0	Sampling clock selection
0	0	0	$f_{XX}/4$

(49) Interrupt control registers (ADnIC)

The ADnIC register is set as follows.

ADnIC register = 04H

ADnIC (n = 0, 1) — Address: AD0IC FFFFF1BCH, AD1IC FFFFF1BEH

	7	6	5	4	3	2	1	0
After reset	0	1	0	0	0	1	1	1
Bit name	ADnIF	ADnMK	0	0	0	ADnPR2	ADnPR1	ADnPR0
Set value	0	0	0	0	0	1	0	0

ADnIF	Interrupt request flag[Note]
0	Interrupt request signal not issued

ADnMK	Interrupt mask flag
0	Interrupt servicing enabled

ADnPR2	ADnPR1	ADnPR0	Interrupt priority specification bit
1	0	0	Specifies level 4.

Note The flag ADnIF is reset automatically by the hardware if an interrupt request signal is acknowledged.

(50) Interrupt control registers (TB0OVIC)

The TB0OVIC register is set as follows.

TB0OVIC register = 01H

TB0OVIC — Address: FFFFF142H

	7	6	5	4	3	2	1	0
After reset	0	1	0	0	0	1	1	1
Bit name	TB0OVIF	TB0OVMK	0	0	0	TB0OVPR2	TB0OVPR1	TB0OVPR0
Set value	0	0	0	0	0	0	0	1

TB0OVIF	Interrupt request flag[Note]
0	Interrupt request signal not issued

TB0OVMK	Interrupt mask flag
0	Interrupt servicing enabled

TB0OVPR2	TB0OVPR1	TB0OVPR0	Interrupt priority specification bit
0	0	1	Specifies level 1.

Note The TB0OVIF flag is reset automatically by the hardware if an interrupt request signal is acknowledged.

(51) Interrupt mask register 1 (IMR1)

The IMR1 register is set as follows.

IMR1 register = FDFFH

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IMR1 (IMR1H/IMR1L)

Address: IMR1 FFFFF102H
IMR1L FFFFF102H, IMR1H FFFFF103H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
After reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit name	TB1 CCMK0	TB1 OVMK	TB0 CCMK3	TB0 CCMK2	TB0 CCMK1	TB0 CCMK0	TB0 OVMK	CMP MK1F	CMP MK1L	CMP MK0F	CMP MK0L	PMK18	PMK17	PMK16	PMK15	PMK14
Set value	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1

TB1CCMK0	Interrupt mask flag setting
1	INTTB1CC0 interrupt servicing disabled

TB1OVMK	Interrupt mask flag setting
1	INTTB1OV interrupt servicing disabled

TB0CCMK3	Interrupt mask flag setting
1	INTTB0CC3 interrupt servicing disabled

TB0CCMK2	Interrupt mask flag setting
1	INTTB0CC2 interrupt servicing disabled

TB0CCMK1	Interrupt mask flag setting
1	INTTB0CC1 interrupt servicing disabled

TB0CCMK0	Interrupt mask flag setting
0	INTTB0CC0 interrupt servicing disabled

TB0OVMK	Interrupt mask flag setting
1	INTTB0OV interrupt servicing enabled

CMPMK1F	Interrupt mask flag setting
1	INTCMP1F interrupt servicing disabled

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CMPMK1L	Interrupt mask flag setting
1	INTCMP1L interrupt servicing disabled

CMPMK0F	Interrupt mask flag setting
1	INTCMP0F interrupt servicing disabled

CMPMK0L	Interrupt mask flag setting
1	INTCMP0L interrupt servicing disabled

PMK18	Interrupt mask flag setting
1	INTP18 interrupt servicing disabled

PMK17	Interrupt mask flag setting
1	INTP17 interrupt servicing disabled

PMK16	Interrupt mask flag setting
1	INTP16 interrupt servicing disabled

PMK15	Interrupt mask flag setting
1	INTP15 interrupt servicing disabled

PMK14	Interrupt mask flag setting
1	INTP14 interrupt servicing disabled

(52) Interrupt mask register 5 (IMR5)

The IMR5 register is set as follows.

IMR5 register = FF3FH

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IMR5 (IMR5H/IMR5L)

Address: IMR5 FFFFF10AH
IMR5L FFFFF10AH, IMR5H FFFFF10BH

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
After reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit name	1	ADT1 MK	ADT0 MK	TM3 EQMK0	TM2 EQMK0	TM1 EQMK0	TM0 EQMK0	AD2 MK	AD1 MK	AD0 MK	IIC MK	CB2 TMK	CB2 RMK	CB2 REMK	UA2 TMK	UA2 RMK
Set value	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1

ADTIMK	Interrupt mask flag setting
1	INTADT1 interrupt servicing disabled

ADT0MK	Interrupt mask flag setting
1	INTADT0 interrupt servicing disabled

TM3EQMK0	Interrupt mask flag setting
1	INTTM3EQ0 interrupt servicing disabled

TM2EQMK0	Interrupt mask flag setting
1	INTTM2EQ0 interrupt servicing disabled

TM1EQMK0	Interrupt mask flag setting
1	INTTM1EQ0 interrupt servicing disabled

TM0EQMK0	Interrupt mask flag setting
1	INTTM0EQ0 interrupt servicing enabled

AD2MK	Interrupt mask flag setting
1	INTAD2 interrupt servicing disabled

AD1MK	Interrupt mask flag setting
0	INTAD1 interrupt servicing enabled

(2/2)

AD0MK	Interrupt mask flag setting
0	INTAD0 interrupt servicing enabled

IICMK	Interrupt mask flag setting
1	INTIIC interrupt servicing disabled

CB2TMK	Interrupt mask flag setting
1	INTCB2T interrupt servicing disabled

CB2RMK	Interrupt mask flag setting
1	INTCB2R interrupt servicing disabled

CB2REMK	Interrupt mask flag setting
1	INTCB2RE interrupt servicing disabled

UA2TMK	Interrupt mask flag setting
1	INTUA2T interrupt servicing disabled

UA2RMK	Interrupt mask flag setting
1	INTUA2R interrupt servicing disabled

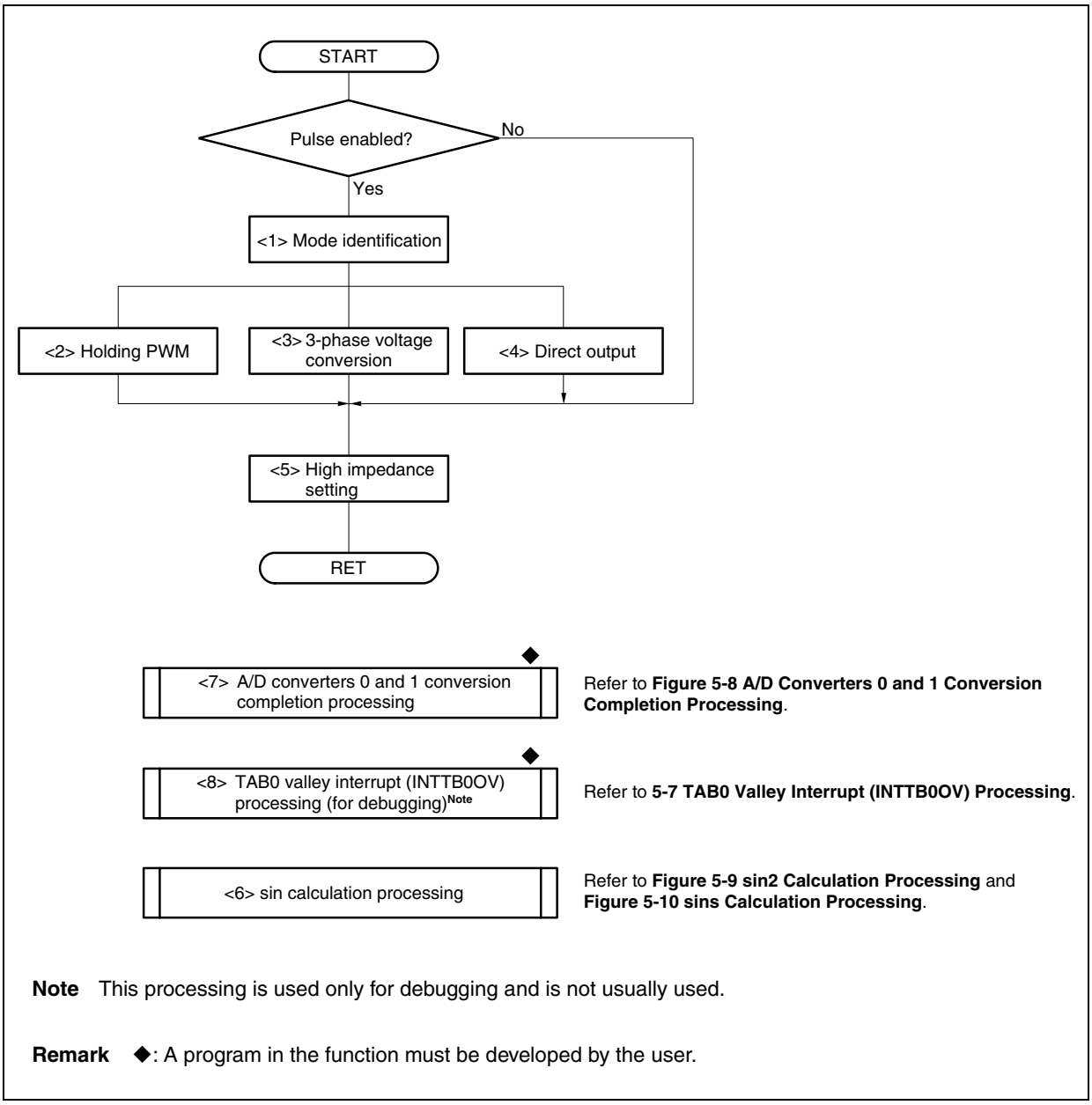
CHAPTER 3 PROGRAM CONFIGURATION

This chapter explains the program configuration of the 3-phase PWM driver. The user should set the PWM pulse.

3.1 Configuration of 3-Phase PWM Driver

The configuration of the 3-phase PWM driver is illustrated below.

Figure 3-1. Phase PWM Driver Configuration (1/2)



Note This processing is used only for debugging and is not usually used.

Remark ◆: A program in the function must be developed by the user.

Figure 3-1. 3-Phase PWM Driver Configuration (2/2)

<1> Mode identification: Identifies the operation mode of the 3-phase PWM driver.
<2> Holding PWM: Sets in the output lock mode the PWM duty ratio previously set by the 3-phase PWM driver.
<3> 3-phase voltage conversion: Performs 3-phase voltage conversion in the dq conversion mode.
<4> Direct output: Individually sets values of phases U, V, and W.
<5> High impedance setting: Switches the port state of the U, $\overline{U}$, V, $\overline{V}$, W, and $\overline{W}$ phase pins between the high-impedance state and PWM output state.
<6> sin calculation processing: sin calculation by Taylor's expansion. Called by <3>.
<7> A/D converters 0 and 1 conversion completion processing: Interrupt servicing that occurs after completion of conversion by A/D converters 0 and 1
<8> TAB0 valley interrupt (INTTB0OV) processing: TAB0 valley interrupt (INTTB0OV) processing. Used for debugging.

3.2 Global Variables

The global variables used for the 3-phase PWM driver are listed below.

Table 3-1. Global Variables

Symbol	No.	Type	Usage	Set Value
bk_hi_z	(1)	unsigned char	Flag holding high-impedance state	0: PWM output pin is in a high-impedance state. 1: PWM output pin is ready for PWM output.
bk_phase_u	(2)	signed int	Holds duty ratio of phase U.	0 to 800
bk_phase_v	(3)	signed int	Holds duty ratio of phase V.	0 to 800
bk_phase_w	(4)	signed int	Holds duty ratio of phase W.	0 to 800
test_pwm_mode	(5)	unsigned char	For debugging (usually commented out)	0: Direct mode 1: dq conversion mode 2: Output lock mode
test_pwm_flag	(6)	unsigned char	For debugging (usually commented out)	0: PWM output disabled 1: PWM output enabled
test_value0	(7)	signed int	For debugging (usually commented out)	In direct mode: 0 to 800 In dq conversion mode: –400 to 400
test_value1	(8)	signed int	For debugging (usually commented out)	In direct mode: 0 to 800 In dq conversion mode: –400 to 400
test_value2	(9)	signed int	For debugging (usually commented out)	In direct mode: 0 to 800 In dq conversion mode: –400 to 400

[Explanation of global variables]

(1) bk_hi_z
This variable holds the status of the PWM output pin when the 3-phase PWM driver was previously driven.

(2) bk_phase_u
This variable holds the set value of the TAB0CCR1 register (U-phase duty ratio) when the 3-phase PWM driver was previously driven in the output lock mode.

(3) bk_phase_v
This variable holds the set value of the TAB0CCR2 register (V-phase duty ratio) when the 3-phase PWM driver was previously driven in the output lock mode.

(4) bk_phase_w
This variable holds the set value of the TAB0CCR3 register (W-phase duty ratio) when the 3-phase PWM driver was previously driven in the output lock mode.

(5) test_pwm_mode
This variable is a RAM area that is used for debugging the 3-phase PWM driver. It specifies pwm_mode to the pwm function in the taa_zero() function. It is usually commented out.

(6) test_pwm_flag
This variable is a RAM area that is used for debugging the 3-phase PWM driver. It specifies pwm_flag to the pwm function in the taa_zero() function. It is usually commented out.

(7) test_value0
This variable is a RAM area that is used for debugging the 3-phase PWM driver. It specifies pwm_value0 to the pwm function in the taa_zero() function. It is usually commented out.

(8) test_value1
This variable is a RAM area that is used for debugging the 3-phase PWM driver. It specifies pwm_value1 to the pwm function in the taa_zero() function. It is usually commented out.

(9) test_value2
This variable is a RAM area that is used for debugging the 3-phase PWM driver. It specifies pwm_value2 to the pwm function in the taa_zero() function. It is usually commented out.

3.3 Definitions of Constants

The constants used for the 3-phase PWM driver are listed in the following table.

Table 3-2. Constants

Symbol	No.	Usage	Constant
MAXPULSE	(1)	Resolution of motor rotation angle	10,000
SGETA	(2)	sin jack-up constant	14
CARRIERPULSE	(3)	Carrier frequency (set value of TAB0CCR0 register)	799

[Explanation of constants]

(1) MAXPULSE

This constant indicates the resolution of the motor rotation angle, and is used with the sin2 function.
It expresses 0° to 360° at a resolution of 10,000.

(2) SGETA

This is a jack-up constant for the sins function.

(3) CARRIERPULSE

This is a set value of carrier frequency.
The TAB0 count clock period can be calculated by the expression below.

$$\text{TAB0 count clock period} = \frac{2}{f_{XX}}$$

Remark f_{XX}: Peripheral clock

The carrier period can be calculated by this expression.

Carrier period = (Set value of TAB0CCR0 register + 1) × 2 × TAB0 count clock period

Example: Set value of carrier frequency where the carrier frequency is 20 kHz (carrier period: 50 μs) and the peripheral clock (f_{XX}) is 64 MHz

$$\begin{aligned}\text{Set value of TAB0CCR0 register} &= \{(\text{Carrier period} \times f_{XX}) / (2 \times 2)\} - 1\\ &= (50 \times 64) / 4 - 1\\ &= 3200 / 4 - 1\\ &= 800 - 1\\ &= 799\end{aligned}$$

Therefore, TAB0CCR0 = CARRIERPULSE = 799.

3.4 Setting of Dead Time

The dead time is set by using the TAB0DTC register and is calculated by the following expression.

Dead time = Set value of TAB0DTC register × TAB0 count clock period

Example: Set value of the TAB0DTC register when the dead time is 4 μs and the peripheral clock (fxx) is 64 MHz

TAB0DTC = Dead time × fxx / 2
= 4 × 64 / 2
= 256 / 2
= 128

Therefore, TAB0DTC = 128.

3.5 Determining PWM Pulse

The relationship between the duty ratios of phase U, V, and W, and the values of the TAB0CCR1 to TAB0CCR3 registers is shown below.

(1) Calculating output width of upper-arm phase

The output widths of phases U, V, and W are calculated by the following expressions (including dead time).

U-phase output width = {(TAB0CCR0 + 1 – TAB0CCR1) × 2 – TAB0DTC} × TAB0 count clock period

V-phase output width = {(TAB0CCR0 + 1 – TAB0CCR2) × 2 – TAB0DTC} × TAB0 count clock period

W-phase output width = {(TAB0CCR0 + 1 – TAB0CCR3) × 2 – TAB0DTC} × TAB0 count clock period

(2) Calculating output width of lower-arm phase

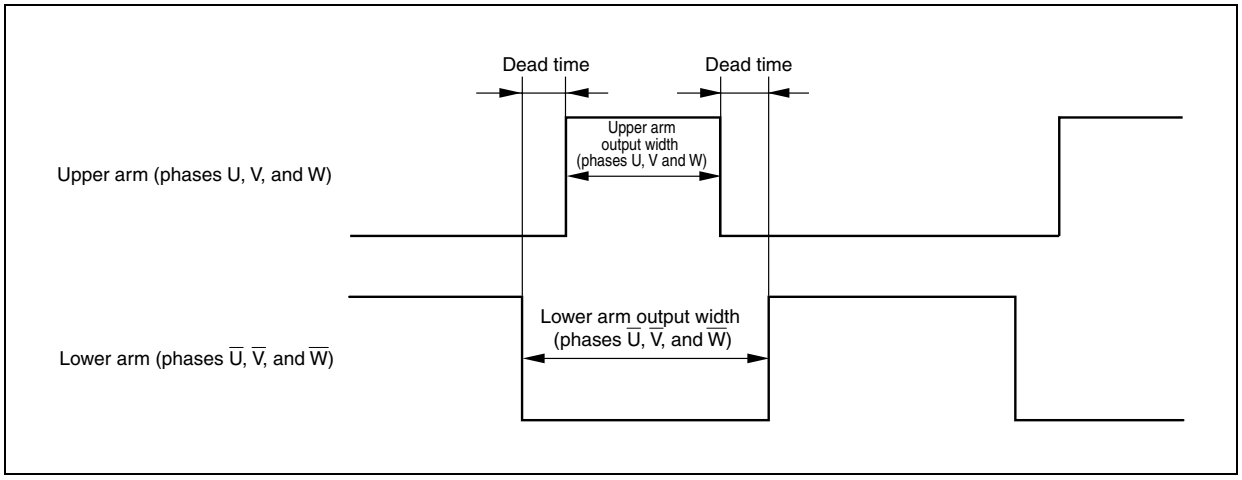
The output widths of phases $\overline{U}$, $\overline{V}$, and $\overline{W}$ are calculated by the following expressions (including dead time).

$\overline{U}$-phase output width = {(TAB0CCR0 + 1 – TAB0CCR1) × 2 + TAB0DTC} × TAB0 count clock period

$\overline{V}$-phase output width = {(TAB0CCR0 + 1 – TAB0CCR2) × 2 + TAB0DTC} × TAB0 count clock period

$\overline{W}$-phase output width = {(TAB0CCR0 + 1 – TAB0CCR3) × 2 + TAB0DTC} × TAB0 count clock period

Figure 3-2. Pulse Calculation in 6-Phase PWM Output Mode



3.6 A/D Conversion

3.6.1 Conversion start trigger timing of A/D converters 0 and 1 for synchronization operation

The 3-phase PWM driver implements a synchronization operation by using TAB0, TMQOP0, and TAA0. Therefore, any timing can be set for the conversion start trigger of A/D converters 0 and 1. Because the timing of comparison match of TAA0 during a synchronization operation is synchronized with the operating clock of TAB0, it is calculated by using the TAB0 count clock period.

The timing of the conversion start trigger of A/D converters 0 and 1 can be calculated by the following expression.

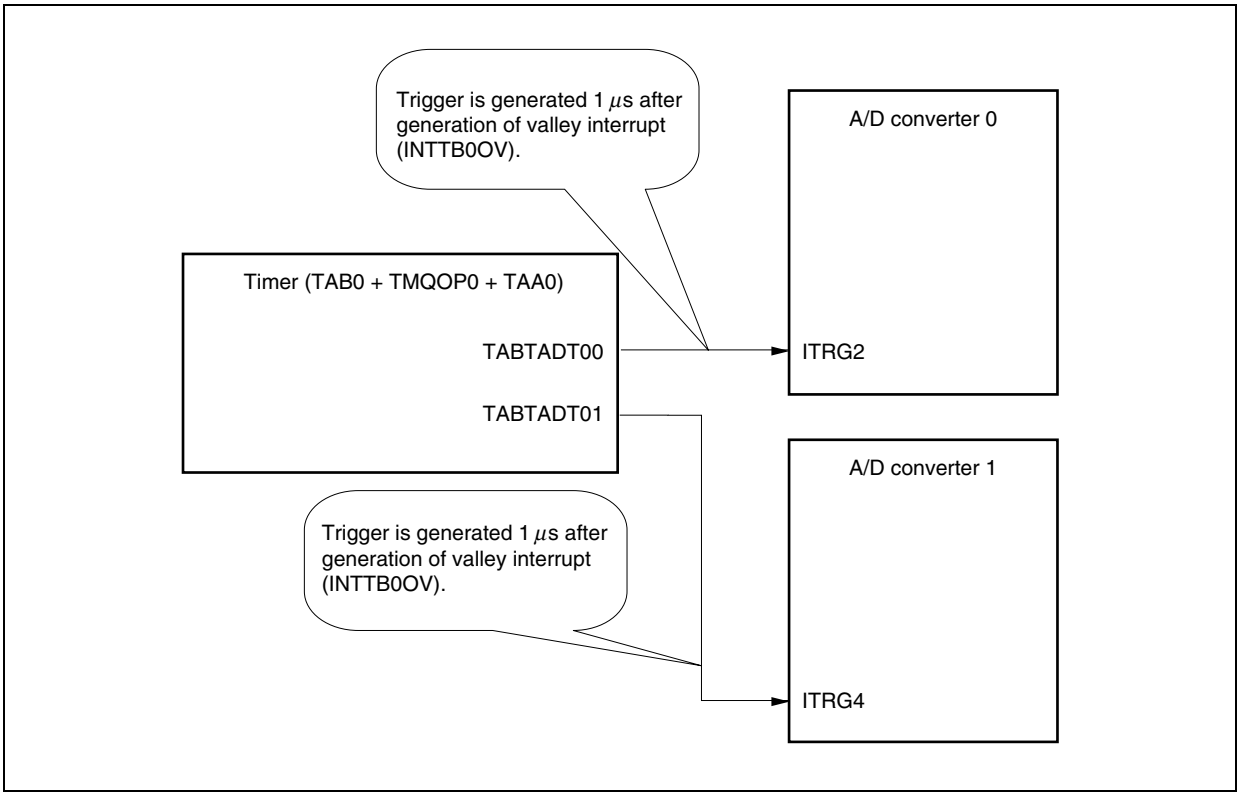
Conversion start trigger timing of A/D converter n = TAA0CCRn × TAB0 count clock period

Remark n = 0 or 1

Example: TAA0 comparison match timing where the timing of the conversion start trigger of A/D converter n is 1 μs after the TAB0 valley interrupt (INTTB0OV) of carrier period and the peripheral clock (fxx) is 64 MHz

Set value of TAA0CCRn register = (Conversion start trigger timing of A/D converter n × fxx) / 2
= (1 × 64) / 2
= 32

Figure 3-3. Conversion Start Trigger Source of A/D Converters 0 and 1 of 3-Phase PWM Driver



With the 3-phase PWM driver, the timing of conversion start trigger of A/D converters 0 and 1 is the same. To change the conversion start time, set the TAA0CCR0 and TAA0CCR1 registers in accordance with the above expression.

3.6.2 A/D conversion completion time

With the 3-phase PWM driver, the AD0CTC register is set as follows.

```
AD0CTC = 0x0C; /*A/D0 conversion clock 32 (2 us)*/
```

The A/D conversion clock time is 32 clocks and the A/D conversion completion time is 2 μs.

3.7 Arguments

The arguments used in the 3-phase PWM driver are listed in the table below.

Table 3-3. Arguments

Symbol	No.	Type	Usage	Set Value
pwm_mode	(1)	unsigned char	Sets 3-phase PWM mode.	0: Direct mode 1: dq conversion mode 2: Output lock mode[Note]
pwm_flag	(2)	unsigned char	PWM output flag	0: PWM output disabled (high-impedance state) 1: PWM output enabled (PWM output)
value0	(3)	signed int	Set value 0	In direct mode: 0 to 800 In dq conversion mode: –400 to 400
value1	(4)	signed int	Set value 1	In direct mode: 0 to 800 In dq conversion mode: –400 to 400
value2	(5)	signed int	Set value 2	In direct mode: 0 to 800 In dq conversion mode: 0 to MAXPULSE

Note If the output is locked in the output lock mode at a high pulse duty ratio, the IGBT driver may generate heat and be damaged. Therefore, set the output lock mode after thoroughly evaluating the pulse duty ratio in the overall system.

[Explanation of arguments]

(1) pwm_mode

This argument sets a mode of the 3-phase PWM driver.

(2) pwm_flag

This argument sets the output status of the PWM output pin.

(3) value0

This argument is a set value in each mode.

In direct mode: U-phase output width. Set this value in a range of 0 to 800 (CARRIERPULSE + 1).

In dq conversion mode: Executes 3-phase voltage conversion used for vector calculation. This value is equivalent to d-axis current in the dq conversion mode.
This value is set in a range of (–400 to 400)[Note].

In output lock mode: None
This argument is not used in the output lock mode.

Remark Refer to the next page for **Note**.

(4) value1

This argument is a set value in each mode.

In direct mode: V-phase output width. Set this value in a range of 0 to 800 (CARRIERPULSE + 1).

In dq conversion mode: Executes 3-phase voltage conversion used for vector calculation. This value is equivalent to q-axis current in the dq conversion mode.
This value is set in a range of (–400 to 400)[Note].

In output lock mode: None
This argument is not used in the output lock mode.

(5) value2

This argument is a set value in each mode.

In direct mode: W-phase output width. Set this value in a range of 0 to 800 (CARRIERPULSE + 1).

In dq conversion mode: Executes 3-phase voltage conversion used for vector calculation. This value is equivalent to the rotation coordinate (θ).
This value is set in a range of (0 to MAXPULSE – 1)[Note].

In output lock mode: None
This argument is not used in the output lock mode.

Note The PWM pulse duty ratio may exceed 100% in the dq conversion mode, depending on the d and q axes and the rotation coordinate (θ). Therefore, thoroughly evaluate the values of value0, value1, and value2.

CHAPTER 4 FILE CONFIGURATION

This chapter explains the file configuration of the 3-phase PWM driver.

4.1 File Configuration

The 3-phase PWM driver consists of the following 10 files.

(1) Source files

<1> main.c: MAIN processing
<2> pt_unit.c: 3-phase PWM driver file
<3> init.c: Initialization processing
<4> common.c: Definitions of constants and global variable declaration
<5> sin2.c: sin calculation processing

(2) Include file

common.h: This is a header file that allows other files to access the global variables defined by common.c by using the EXTERN instruction.
Read this header file to use definitions of constants and global variables with the other file by dividing the file.
If definitions of constants or a global variable is used, the user should define both the common.c and common.h files.

(3) Project-related files

<1> libm.a: Mathematic library[Note]
<2> libc.a: Standard library[Note]
<3> ig3_start.s: Startup routine of 3-phase PWM driver
<4> ig3_link.dir: Link directive file of 3-phase PWM driver

Note libm.a and libc.a are libraries that are automatically allocated by the project manager when a project is generated.

4.2 Explanation of Source Files

Source File Name	Function Name	Explanation
main.c	main()	MAIN processing. Nothing is written in the main routine of the 3-phase PWM driver.
	ad0_function()	Conversion completion processing of A/D converter 0
	ad1_function()	Conversion completion processing of A/D converter 1
	tab_zero()	Interrupt servicing of carrier period
pt_unit.c	pwm()	Driver that performs 3-phase PWM control
	hi_z()	Driver that controls the output pin for 3-phase PWM
Init.c	hinit()	Initializes the on-chip peripheral I/O of the V850E/IG3 (μPD70F3454GC-8EA-A).
	ainit()	Initializes the global variables used for the 3-phase PWM driver.
common.c	–	Defines constants and declares a global variable area.
sin2.c	sin2()	Executes sin calculation.
	sins()	Executes sin calculation.

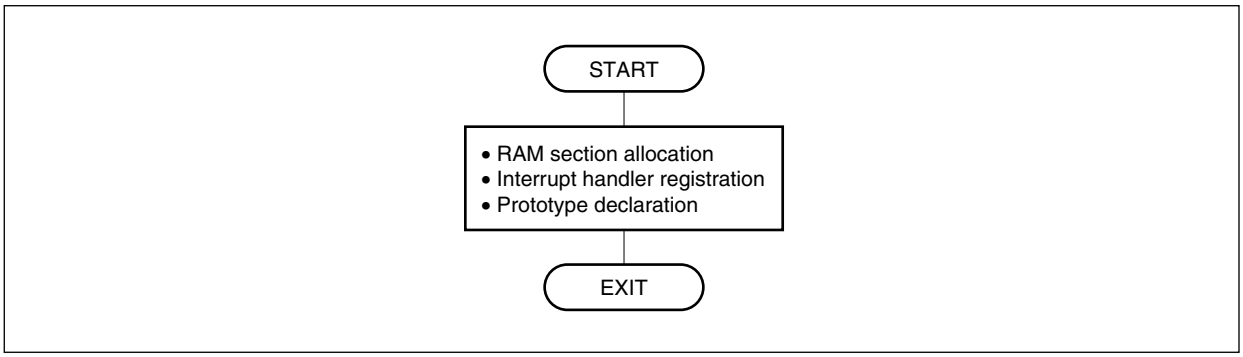
CHAPTER 5 FLOWCHART

This chapter explains each processing of the 3-phase PWM driver by using flowcharts.

5.1 Initialization Processing

The flowchart of the initialization processing is shown below.

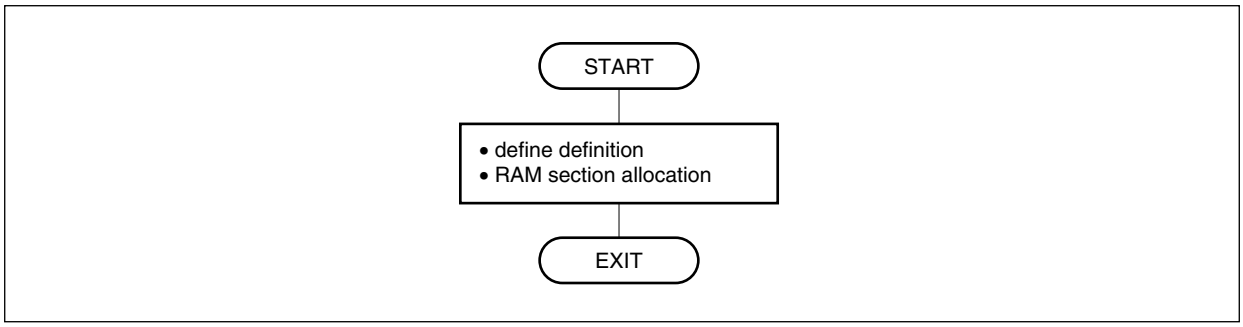
Figure 5-1. Initialization Processing



5.2 Global Variable Processing (common.c)

The flowchart of the global variable processing (common.c) is shown below.

Figure 5-2. Global Variable Processing (common.c)

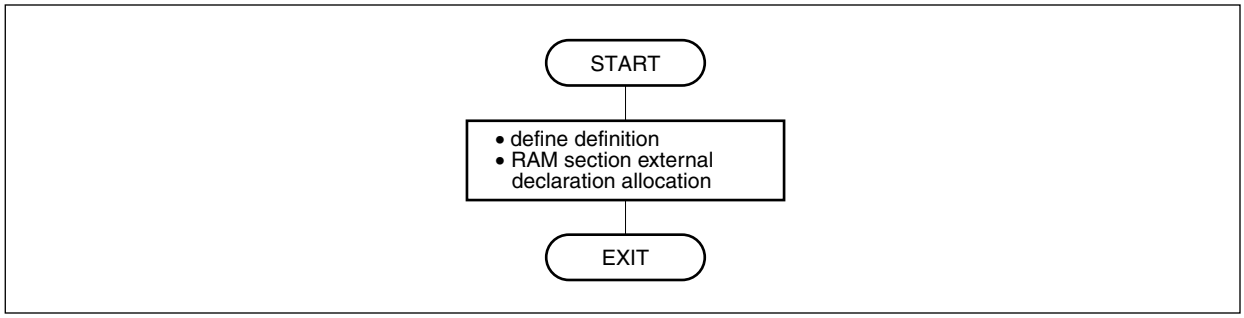


5.3 Global Variable Processing (common.h)

common.h is externally defined by the EXTERN instruction. common.h is called by main.c, pt_unit.c, init.c, and sin2.c.

The flowchart of global variable processing (common.h) is shown below.

Figure 5-3. Global Variable Processing (common.h)

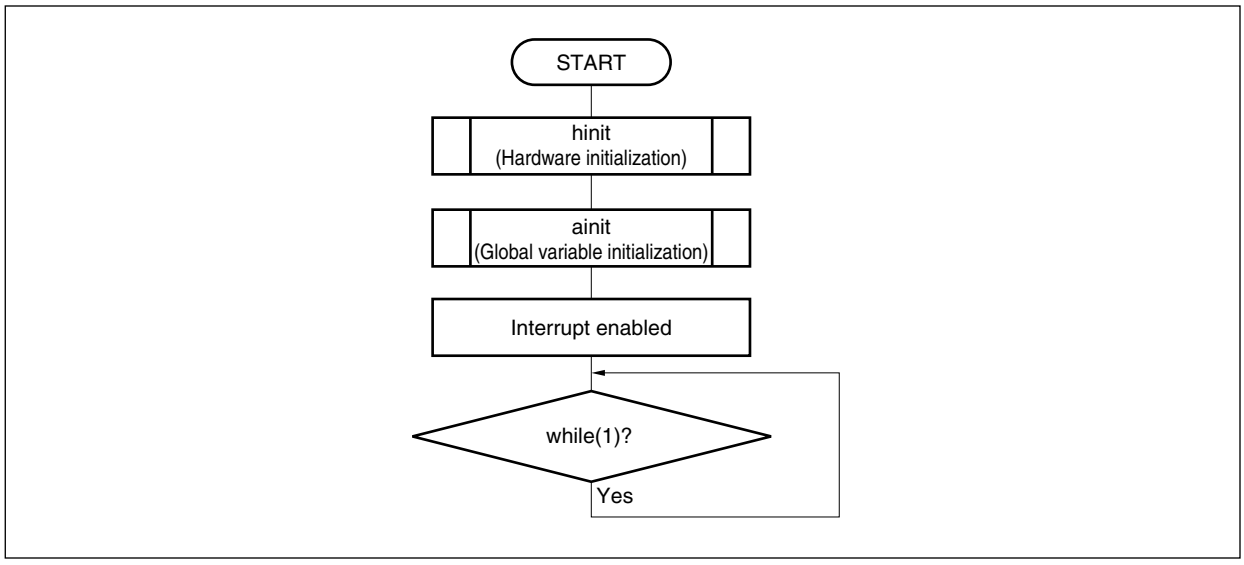


5.4 MAIN Processing

The MAIN processing initializes the hardware and global variables of the 3-phase PWM driver.

The following flowchart illustrates the MAIN processing.

Figure 5-4. MAIN Processing

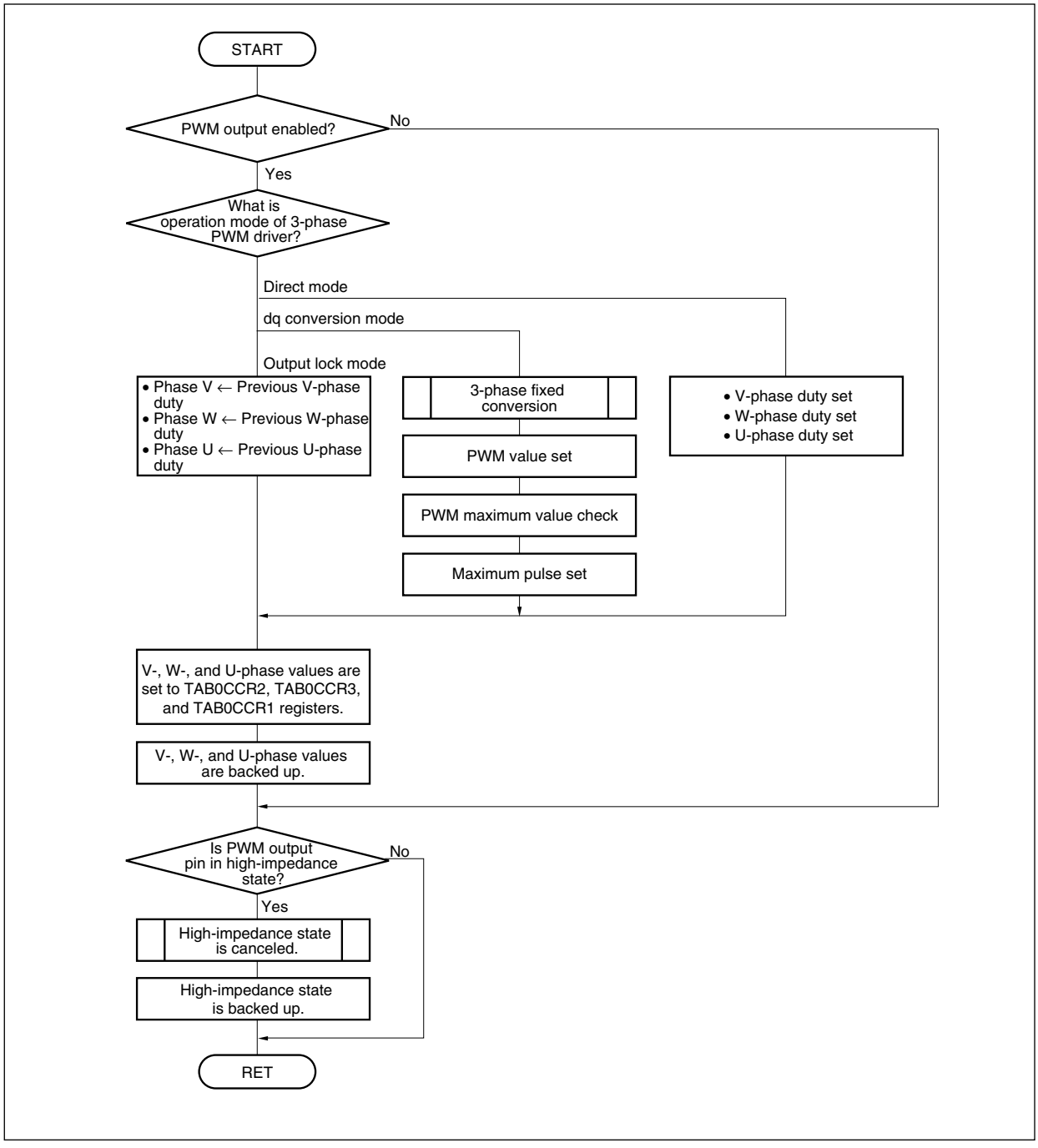


5.5 PWM Processing

Three modes of PWM processing are available: direct mode, dq conversion mode, and output lock mode. The 3-phase PWM driver writes the TAB0CCR0 to TAB0CCR3, TAB0OPT1, TAA0CCR0, and TAA0CCR1 registers all at once when the TAB0 valley interrupt (INTTB0OV) is generated after the TAB0CCR1 register is written. Therefore, be sure to call the PWM processing with the tab_zero processing when setting the registers in the PWM processing (after the TAB0CCR1 register is written, the next writing of a register is prohibited until the TAB0 valley interrupt (INTTB0OV) is generated).

The flowchart of the PWM processing is shown below.

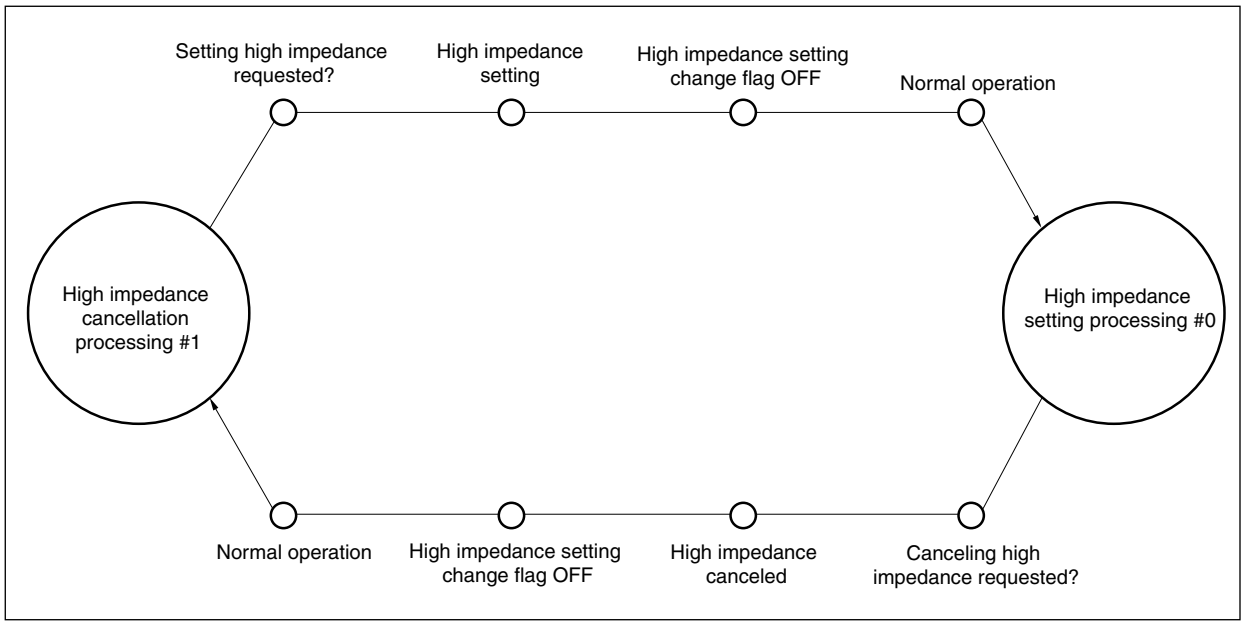
Figure 5-5. PWM Processing



5.6 High-Impedance Setting Processing

The flowchart of high-impedance setting processing is shown below.

Figure 5-6. High-Impedance Setting Processing



5.7 TAB0 Valley Interrupt (INTTB0OV) Servicing

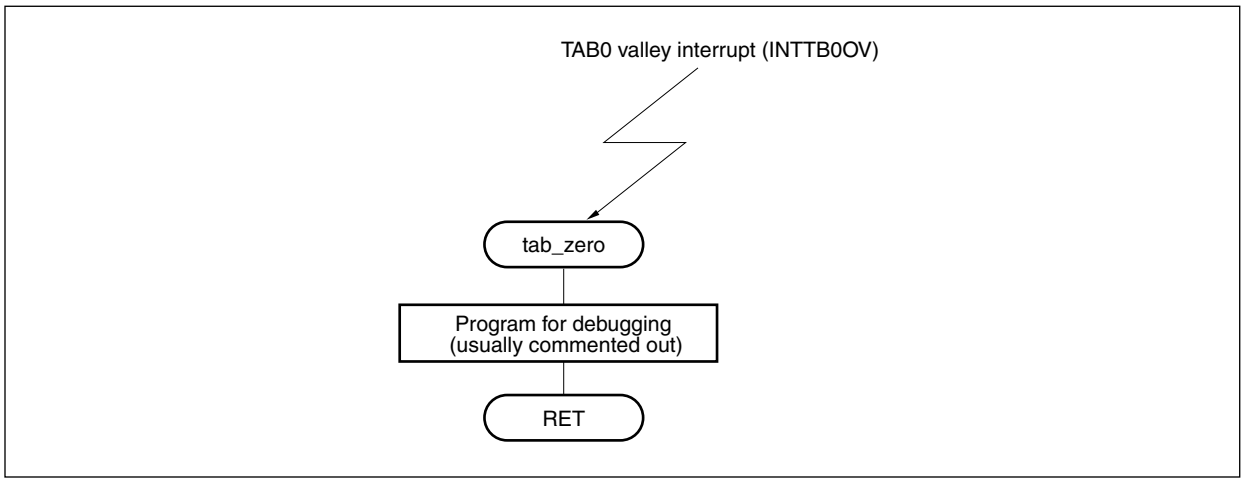
This processing is performed when the TAB0 valley interrupt (INTTB0OV) of carrier period is generated. It is used by the 3-phase PWM driver only for debugging and is not usually used. Therefore, program description is commented out.

When using the 3-phase PWM driver, delete the program for debugging.

Note that the priority level of the TAB0 valley interrupt (INTTB0OV) is 1.

The following flowchart illustrates the TAB0 valley interrupt (INTTB0OV) servicing.

Figure 5-7. TAB0 Valley Interrupt (INTTB0OV) Servicing



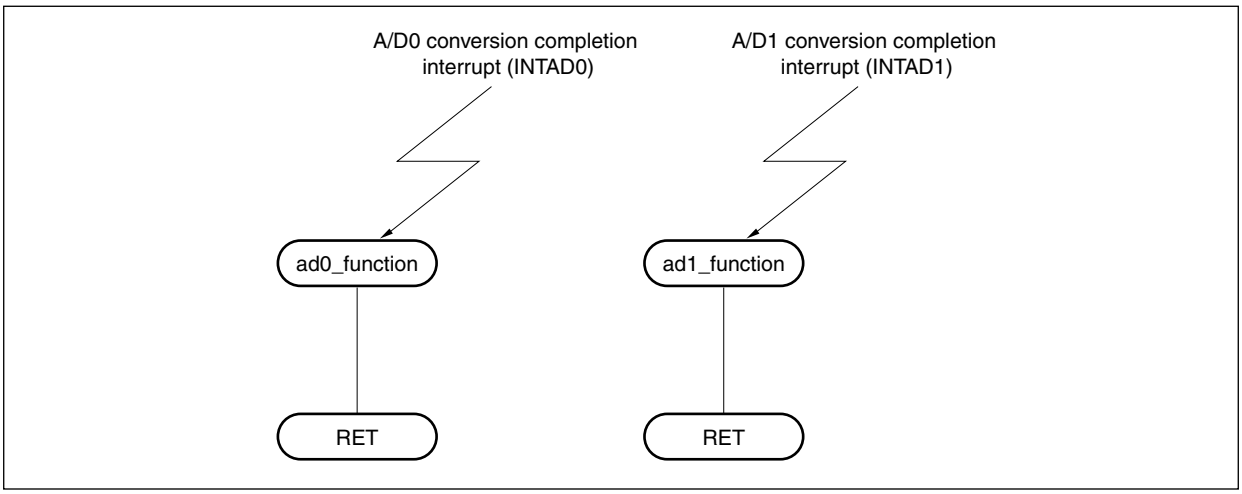
5.8 A/D Converters 0 and 1 Conversion Completion Processing

This function is called after conversion by A/D converters 0 and 1 is completed. The 3-phase PWM driver programs nothing in the function.

The priority level of the A/Dn conversion completion interrupt (INTADn) is 4 (n = 0 or 1).

The following flowchart illustrates the A/D converters 0 and 1 conversion completion processing.

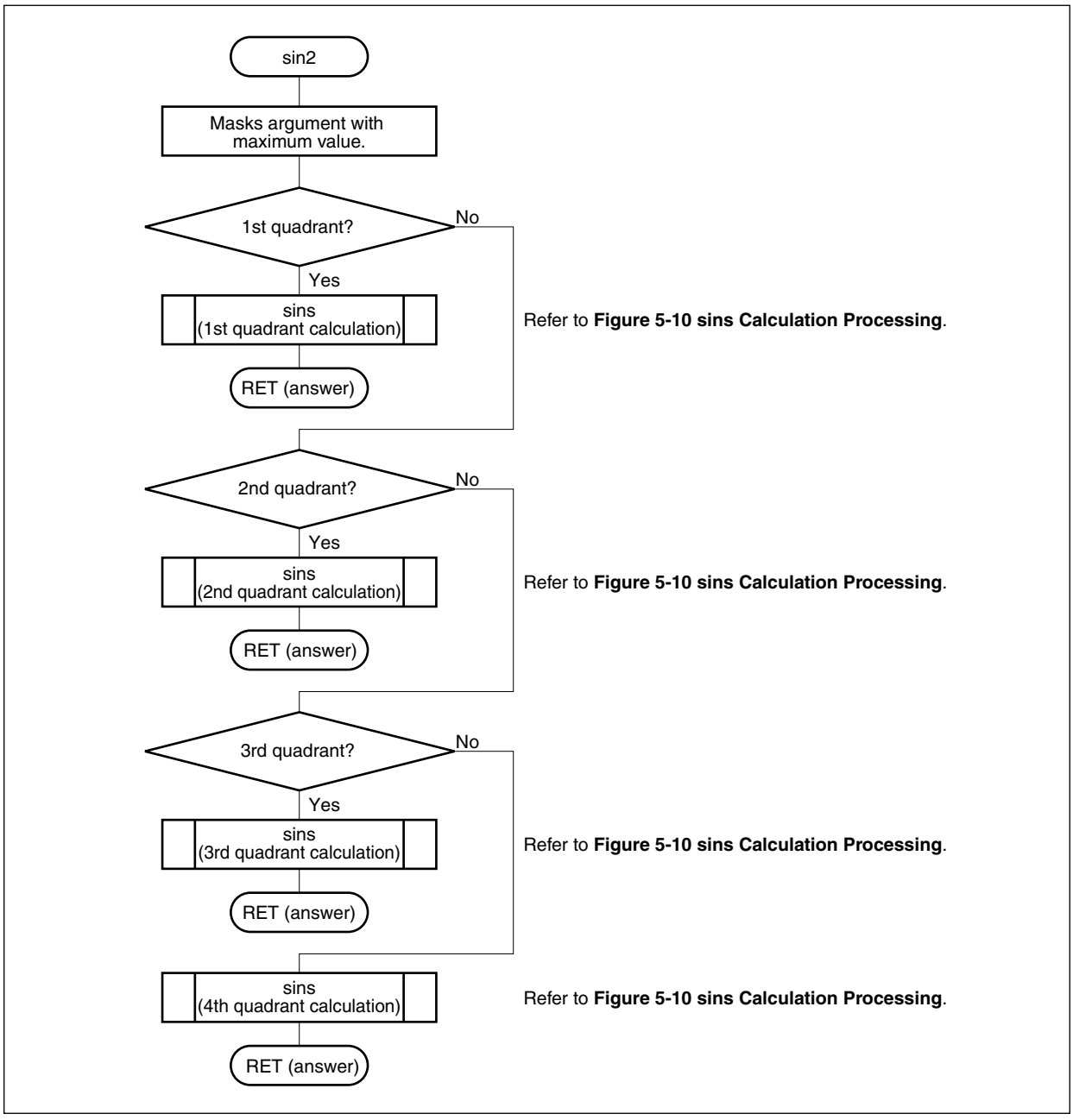
Figure 5-8. A/D Converters 0 and 1 Conversion Completion Processing



5.9 sin2 Calculation Processing

This function executes sin calculation by Taylor's expansion.
The following flowchart illustrates the sin2 calculation processing.

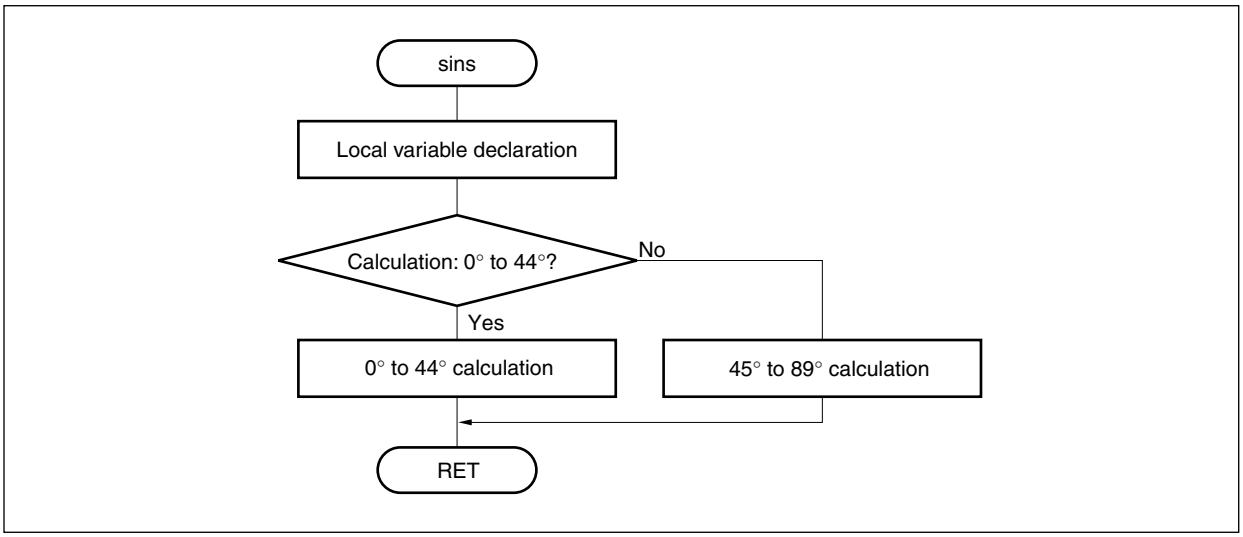
Figure 5-9. sin2 Calculation Processing



5.10 sins Calculation Processing

This function executes sins calculation by Taylor's expansion. It is called by sin2.
The following flowchart illustrates the sins calculation processing.

Figure 5-10. sins Calculation Processing



CHAPTER 6 SETTINGS

6.1 Settings of 3-Phase PWM Driver

The settings of the 3-phase PWM driver are shown below.

Table 6-1. Settings of 3-Phase PWM Driver

Parameter	Set Value
Operating clock of microcontroller	64 MHz (input clock: 8 MHz)
PWM output pin	TOB0T1 to TOB0T3, TOB0B1 to TOB0B3
Carrier frequency	20 kHz
Culling rate	1/1
Dead time	4 μs
A/D conversion start trigger timing of ANI00	1 μs after TAB0 valley interrupt (INTTB0OV) of carrier period
A/D conversion start trigger timing of ANI10	1 μs after TAB0 valley interrupt (INTTB0OV) of carrier period
A/D conversion completion time of ANI00	2 μs
A/D conversion completion time of ANI10	2 μs
Priority level of A/D0 conversion completion interrupt (INTAD0) of ANI00	Level 4
Priority level of A/D1 conversion completion interrupt (INTAD1) of ANI10	Level 4
Operating mode of A/D converters 0 and 1	Set the trigger for INTTA0CC0 and INTTA0CC1 in hardware trigger mode of normal operation mode.
Synchronization operation	Performed

APPENDIX A INTERFACE BETWEEN MODULES

The following table shows the interfaces between the modules of the 3-phase PWM driver.

Table A-1. Interfaces Between Modules of 3-phase PWM Driver (1/2)

Transmission Module	Interface	Type	Symbol	Explanation	Reception Module
main()	Mode setting	B	pwm_mode	For setting 3-phase PWM mode 0x00: Direct mode 0x01: dq conversion mode 0x02: Output lock mode	pwm()
	Output enable	B	pwm_flag	Enables PWM output. 0x00: Changes mode of PWM output pin to high-impedance mode. 0x01: Changes mode of PWM output pin to PWM output mode.	
	Set 0	W	value0	Control value 0 In direct mode: U-phase duty (0 to 800) In dq conversion mode: d-axis current (−400 to 400)	
	Set 1	W	value1	Control value 1 In direct mode: V-phase duty (0 to 800) In dq conversion mode: q-axis current (−400 to 400)	
	Set 2	W	value2	Control value 2 In direct mode: W-phase duty (0 to 800) In dq conversion mode: Rotor rotation position (0 to 9,999)	
	x	LW	x	Passes x value of sin2 calculation processing. 0 to 9,999	sin2()

Remark B: Byte type
W: Word type
LW: Local word type

Table A-1. Interfaces Between Modules of 3-phase PWM Driver (2/2)

Transmission Module	Interface	Type	Symbol	Explanation	Reception Module
pwm()	pt_unit status	W	pwm() output	Passes status after pwm processing. 0x00 to 0x03, 0xff: Return value from hi-z function	main()
	x	LW	x	Passes x value of sin2 calculation processing. 0 to 9,999	sin2()
	High-impedance mode setting	B	hi_mode	Enables high-impedance mode. 0x00: High-impedance mode 0x01: Cancels high-impedance mode.	hi_z()
	hi_z flag	B	hi_flag	High-impedance mode setting change flag 0x00: High-impedance state is not changed. 0x01: Changing high-impedance state is enabled.	
Hi_z()	High-impedance state	W	hi_z() output	Passes status after high-impedance processing. 0x00: High-impedance state 0x01: Cancels high-impedance state. 0x02: None 0x03: Other mode	main() pwm()
sin2()	sin2answer	LW	sin2() output	Returns sin2 calculation result. Maximum value: 0x3fff Minimum value: 0xffffc001	main() pwm()
	x	LW	x	Passes x value for sins calculation processing. 0 to 2,499	sins()
sins()	sinanswer	LW	sins	Returns sins calculation result.	sin2()
				Maximum value: 0x3fff	
				Minimum value: 0xffffc001	

Remark B: Byte type
W: Word type
LW: Local word type

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