V850E2/MN4

Complementary PWM Output Function

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Introduction

This application note describes the setting method of the complementary PWM output function, gives an overview of the operation of the sample code, and explains its use.

Target Device

V850E2/MN4 microcontrollers

Contents

1. Outline

1.1 Application System

The system (sample code) uses a target board designed for a V850E2/MN4 microcontroller. Please contact a Renesas Electronics sales representative or agent with regard to obtaining or receiving technical support for the target board.

1.2 Development Environment

1.2.1 Software Development Environment

Integrated development environment: CubeSuite+
Multi (Green Hills software)
IAR Embedded Workbench (IAR Systems)

C compiler: CX

Hardware environment

On-chip debugging emulator: QB-V850MINI

Target board: QB-V850E2MN4DUAL-TB

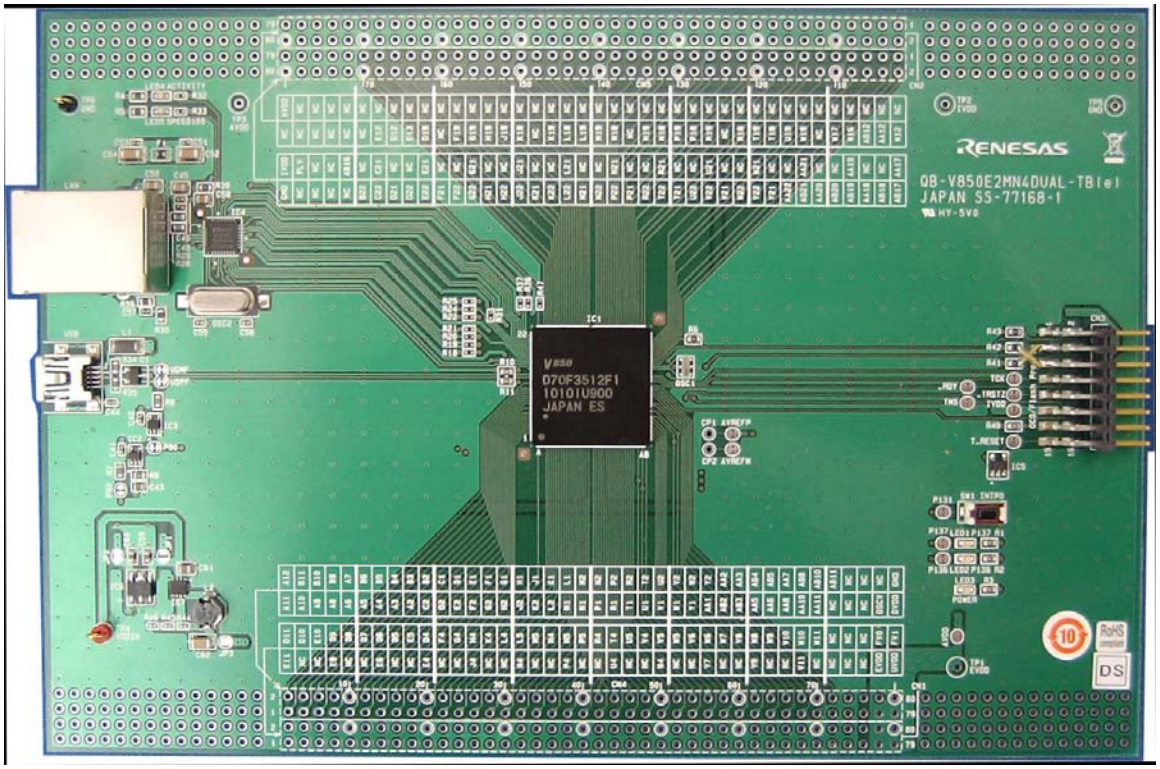

Figure 1.1 V850E2/MN4 Target Board

2. System Overview

This section provides an overview of the system.

2.1 Hardware Configuration

The hardware configuration is shown below.

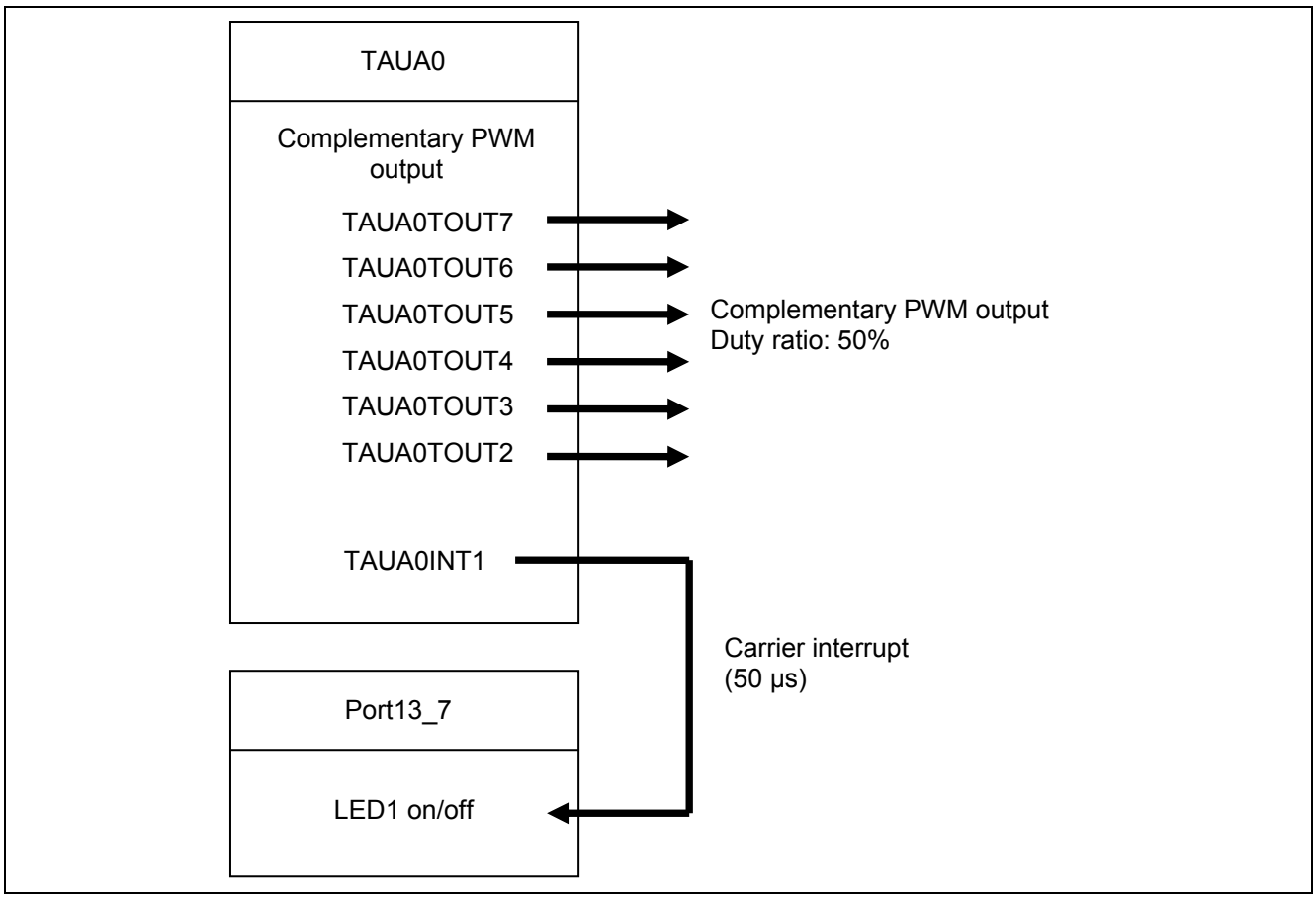

Figure 2.1 Hardware Configuration

2.2 Hardware Specifications

2.2.1 Interface

The user interface elements of the system are listed below.

Table 2.1 User Interface

Item	Interface Element	Function
LED1	Orange LED	During PWM output: On, off (50 µs period)

A V850E2/MN4 pin interface listing for the system is shown below.

Table 2.2 Pin Interface

Pin Name	Function
P136/INTP4/CAN1TXD/TXD5/SCL5/SCK5	LED1 on/off control
P82/S_D18/TA0_I2/TA0_O2/TE0_TI1	Complementary PWM output (U-phase high side)
P83/S_D19/TA0_I3/TA0_O3/	Complementary PWM output (U-phase low side)
P84/S_D20/TA0_I4/TA0_O4/TE0_TA	Complementary PWM output (V-phase high side)
P85/S_D21/TA0_I5/TA0_O5/	Complementary PWM output (V-phase low side)
P86/S_D22/TA0_I6/TA0_O6/TE0_TB	Complementary PWM output (W-phase high side)
P87/S_D23/TA0_I7/TA0_O7/	Complementary PWM output (W-phase low side)

2.2.2 Peripheral Functions

The peripheral functions used by the system are listed below.

Table 2.3 Peripheral Functions

Peripheral Function	Control System Function
Timer array unit A0 (TAUA0)	Complementary PWM output (Six: TAUA0TOUT2 to TAUA0TOUT7)

(1) Timer Array Unit A0 (TAUA0)

Complementary PWM output

Complementary PWM output is implemented on channels 0 to 7 by means of modulation using the six-phase triangle PWM output function and real-time output function of the timer array unit. The carrier modulation method of the six-phase triangle PWM output function is triangle wave modulation.

In addition, for the control period (50 μs) of the system, the channel 1 interrupt is used as a real-time trigger interrupt (synchronized with the PWM period).

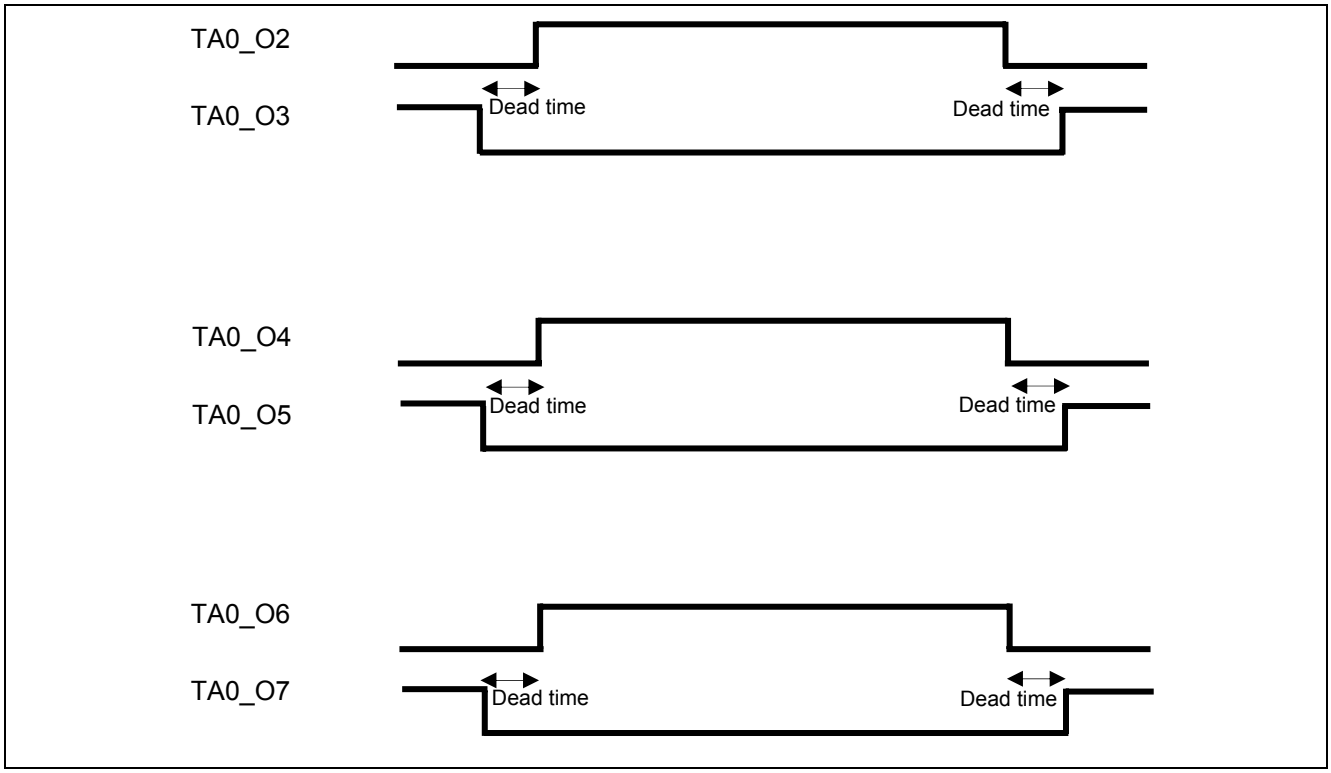

Figure 2.2 Complementary PWM Output Waveforms (PWM Output with Dead Time)

The correspondences between the timer array unit TAUA0 functions mentioned above and the channels used are shown below.

Table 2.4 Timer Array Unit Channels Used

Number	Control System Function
Channel 0	PWM output period setting
Channel 1	Real-time trigger setting
Channel 2	U-phase duty value setting
Channel 3	U-phase dead time value setting
Channel 4	V-phase duty value setting
Channel 5	V-phase dead time value setting
Channel 6	W-phase duty value setting
Channel 7	W-phase dead time value setting

2.2.3 Interrupt

The system uses the following interrupt.

Table 2.5 Interrupt Used

Interrupt	Function
INTTAUA0I1	Real-time trigger interrupt (control period: 50 μs)

2.3 Basic Specifications of Software

2.3.1 Basic Specifications of Software

The basic specifications of the system's software are shown below.

Table 2.6 Basic Specifications of Software

Setting Function	Complementary PWM output
Carrier frequency (PWM)	20 [kHz]

2.3.2 Abbreviated Software Flowcharts

Abbreviated flowcharts of the system's software are shown below.

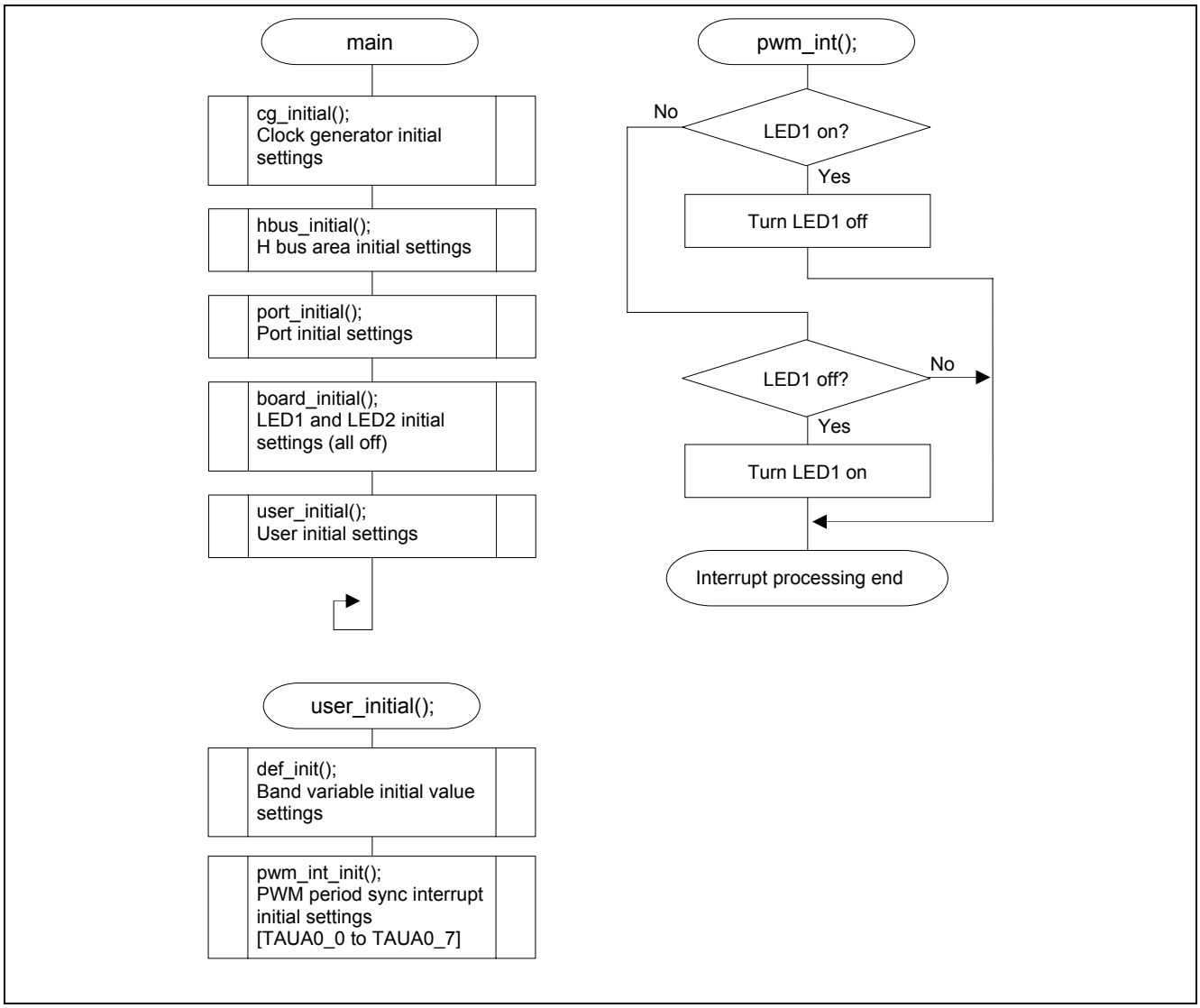

Figure 2.3 Abbreviated Software Flowcharts (Main, PWM Period Sync Interrupt)

3. Peripheral Functions

This section describes the peripheral functions used by the system.

(1) Timer Array Unit A0

Complementary PWM output: Six-phase triangle PWM output (PWM with dead time) and real-time output

3.1 Timer Array Unit A (TAUA) Functions

Timer array unit A (TAUA) comprises four 16-bit timer units, each of which has 16 channels. Each channel has a 16-bit counter and 16-bit data register. The 16-bit timer units can be used independently, and multiple 16-bit timers can be combined to implement sophisticated timer functions.

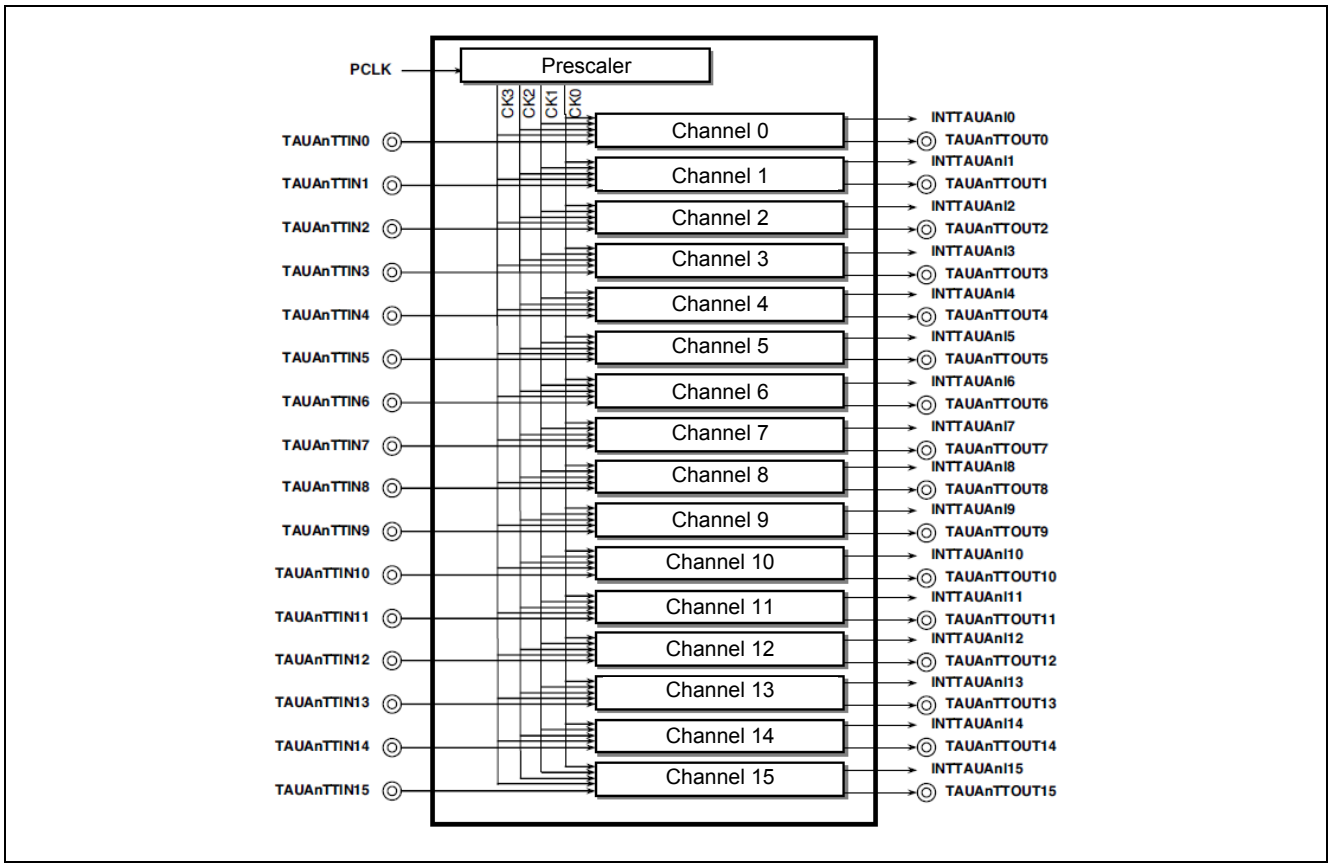

Figure 3.1 TAUA I/O Signals

The system uses TAUA0 to generate complementary PWM output. The correspondences between the channels used by the system and the control functions are shown below.

Table 3.1 Timer Array Unit Channels Used and Control Functions

Number	Control System Function	Timer Operating Mode	
Channel 0	PWM output period setting	Six-phase triangle PWM output function	
Channel 1	Real-time trigger PWM control period	Interrupt culling function (the system uses a culling count of 1)	
Channel 2	PWM output	Six-phase triangle PWM output function	U-phase duty value setting
Channel 3			U-phase dead time value setting
Channel 4			V-phase duty value setting
Channel 5			V-phase dead time value setting
Channel 6			W-phase duty value setting
Channel 7			W-phase dead time value setting

3.1.1 Complementary Modulation Output Function

The complementary modulation output function uses a six-phase triangle PWM output function and a linked real-time output function to generate six PWM with dead time (complementary PWM) outputs, three high arm and three low arm. The PWM period of the system is set at 20 kHz (50 µs). The basic timing of the complementary modulation output is shown below.

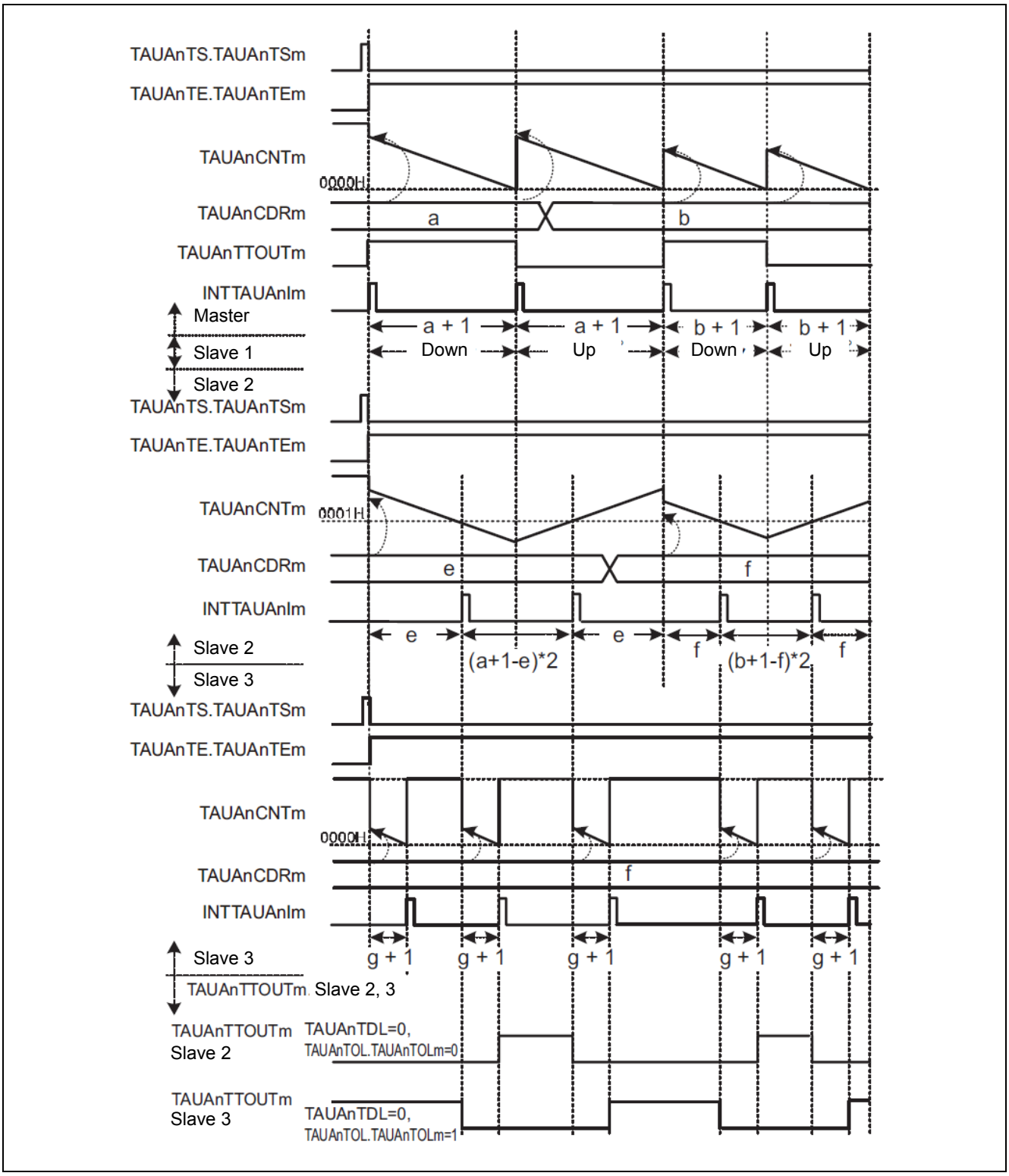

Figure 3.2 Basic Timing Example of Complementary Modulation Output

The settings of channels 0 to 7, which are used by the complementary modulation output function, are listed below.

Table 3.2 Complementary Modulation Output Function Settings

Channel	Item	Description
Channel 0 (master)	Source clock	CK0
	Count clock frequency	66.6 MHz
	Interrupt period	25 µs (PWM period of 50 µs not used)
	Channel data register 0 (TAUA0CDR0) setting value	1666 (25 µs (for triangle wave))
Channel 1	Source clock	CK0
	Count clock frequency	Master interrupt (INTTAUA0I0)
	Interrupt period	50 µs (control period: same as PWM period)
	Channel data register 1 (TAUA0CDR1) setting value	1
Channel 2	Source clock	CK0
	Count clock frequency	66.6 MHz
	Channel data register 2 (TAUA0CDR2) setting value	833 (modulation factor: 50%)
Channel 3	Source clock	CK0
	Count clock frequency	66.6 MHz
	Dead time value	2 µs
	Channel data register 3 (TAUA0CDR3) setting value	132 (2 µs)
Channel 4	Source clock	CK0
	Count clock frequency	66.6 MHz
	Channel data register 4 (TAUA0CDR4) setting value	833 (modulation factor: 50%)
Channel 5	Source clock	CK0
	Count clock frequency	66.6 MHz
	Dead time value	2 µs
	Channel data register 5 (TAUA0CDR5) setting value	132 (2 µs)
Channel 6	Source clock	CK0
	Count clock frequency	66.6 MHz
	Channel data register 6 (TAUA0CDR6) setting value	833 (modulation factor: 50%)
Channel 7	Source clock	CK0
	Count clock frequency	66.6 MHz
	Dead time value	2 µs
	Channel data register 7 (TAUA0CDR7) setting value	132 (2 µs)

3.1.2 From Modulation Factor to PWM Duty Setting

The duty setting of the complementary modulation output is accomplished with multiple channels functioning in a linked manner. The period is set on one channel and the duty and dead time are set on the others. The system uses fixed values for period and dead time, and the duty of the U, V, and W phases is controlled by the channel data registers of channels 2, 4, and 6.

In contrast to the other PWM functions, the function for generating complementary PWM output uses a smaller channel data register value to produce a larger duty value. Therefore, when the channel data register value is reduced the duty value decreases. The expressions for calculating the values (when dead time is ignored) are shown below.

- PWM period = (setting value of channel 0 channel data register (TAUA0CDR0) + 1) × 2 × count clock period
- Duty [%] = {(setting value of channel 0 channel data register (TAUA0CDR0) +1 – setting value of TAUA0CDRn) / (setting value of channel 0 channel data register (TAUA0CDR0) + 1)} × 100
- 0% output = setting value of TAUA0CDRn ≥ setting value of channel 0 channel data register (TAUA0CDR 0) + 1)
- 100% output = TAUA0CDRn = 0000H

Remark: n = 2, 4, 6

The method of calculating the setting value of the channel data register (the PWM duty) from the modulation factor, described above, is such that when the modulation factor is a value of 0% to 100%, the relationship between the modulation factor and the setting value of the channel data register is as shown below.

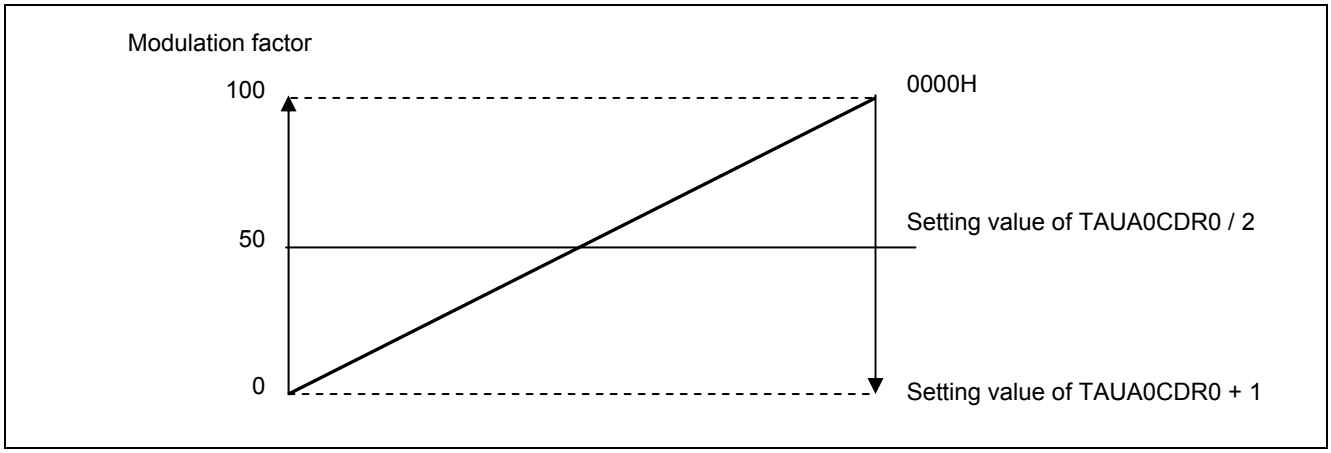

Figure 3.3 Relationship between Modulation Factor and Channel Data Register

The following expression shows this relationship between the value of the channel data register (TAUA0CDRn), which sets the duty, and the modulation factor.

Setting value of TAUA0CDRn = TAUA0CDR0 – (modulation factor × TAUA0CDR0)

Remark: n = 2, 4, 6

The system sets the modulation factor of all TAUA0CDRn registers to 50%.

Setting value of TAUA0CDRn = TAUA0CDR0 – (0.5 × TAUA0CDR0)
= 1666 – (0.5 × 1666)
= 833

Remark: n = 2, 4, 6

3.1.3 Settings of Complementary Modulation Output Function

The system makes initial settings to the channels used for six-phase triangle PWM as described below.

(1) TAUA0 Channel Stop Trigger Register 2 (TAUA0TT)

This register stops operation on the individual channels of TAUA0. The bits corresponding to the channels used by the complementary PWM output function (channels 0 to 7) are set to 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TAUA0TT	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

TAUA0 channels 0 to 7

(2) TAUA0 Prescaler Clock Select Register (TAUA0TPS)

This register selects among 16 types of prescaler output ($fCLK/2^0$ to $fCLK/2^{15}$). The system sets CK0 to CK3 to fCLK (66.6 MHz).

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TAUA0TPS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CK3 CK2 CK1 CK0

(3) TAUA0 Channel Mode OS Register 0 (TAUA0CMOR0)

This register sets the operating mode of the timer channel. The timer channel is used to control the PWM period of 50 µs. The system selects CK0 (66.6 MHz) as the count clock , so TAUA0CKS (bits 15 and 14) is set to 00. Since TAUA0CMOR0 functions as a timer channel, TAUA0MAS (bit 11) is set to 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TAUA0CMOR0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

(4) TAUA0 Channel Mode OS Register 1 (TAUA0CMOR1)

This register sets the real-time trigger as the control period (interrupt culling function). This function requires that the control period be the same as the PWM period. In addition, the source clock setting and the TAUA0CKS (bits 15 and 14) value must be the same for the timer channel and slave channels. TAUA0CCS (bits 13 and 12) is set to 11 to select the timer channel interrupt (INTTAUA0I0) as the timer count clock. Also, TAUA0MD (bits 4 to 1) is set to 0011 to set the operating mode to event count mode.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TAUA0CMOR1	0	0	1	1	0	0	0	0	0	0	0	0	0	1	1	0

(5) TAUA0 Channel Mode OS Registers 2, 4, and 6 (TAUA0CMOR2, TAUA0CMOR4, and TAUA0CMOR6)

These registers set the operating mode of slave channel n (n = 2, 4, 6). This setting controls the duty of the PWM output from TAUA0TTOUTn / TAUA0TTOUTn + 1. The source clock setting and the TAUA0CKS (bits 15 and 14) value must be the same for the timer channel and slave channels. TAUA0CCS (bits 13 and 12) is set to 00 to select the count clock selected for the timer channel as the timer count clock. The timer channel up/down output trigger signal is selected as the timer state trigger, so TAUA0STS (bits 10 to 8) is set to 111. In addition, TAUA0MD (bits 4 to 1) is set to 1001 to set up/down count mode as the operating mode. Bit 0 is cleared to 0 to prevent generation of an interrupt at timer-start.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TAUA0CMORn	0	0	0	0	0	1	1	1	0	0	0	1	0	0	1	0

Remark: n = 2, 4, 6

(6) TAUA0 Channel Mode OS Registers 3, 5, and 7 (TAUA0CMOR3, TAUA0CMOR5, and TAUA0CMOR7)

These registers set the operating mode of slave channel n (n = 3, 5, 7). This setting controls the dead time of the PWM output from TAUA0TTOUTn / TAUA0TTOUTn – 1. The TAUA0CKS (bits 15 and 14) value must be the same for the timer channel and slave channels. TAUA0CCS (bits 13 and 12) is set to 00 to select the count clock selected for the timer channel as the timer count clock. The dead time trigger is selected as the timer state trigger, so TAUA0STS (bits 10 to 8) is set to 110. In addition, TAUA0MD (bits 4 to 1) is set to 0100 to one count mode as the operating mode. Bit 0 is set to 1 to enable the dead time trigger (start trigger) interrupt during counting.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TAUA0CMORn	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0	1

Remark: n = 3, 5, 7

(7) TAUA0 Channel Data Register 0 (TAUA0CDR0)

This register sets the PWM period. It is set to 1666 to specify a carrier frequency of 20 kHz (50 µs).

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TAUA0CDR0	0	0	0	0	0	1	1	0	1	0	0	0	0	0	1	0

(8) TAUA0 Channel Data Register 1 (TAUA0CDR1)

This register sets the interrupt culling count. The setting value is used as the triangle wave interrupt period, so it must be an odd value (1, 3, or 5). Since the value should be the same as the PWM period, a setting of 1 is used.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TAUA0CDR1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

(9) TAUA0 Channel Data Registers 2, 4, and 6 (TAUA0CDR2, TAUA0CDR4, and TAUA0CDR6)

These registers set the PWM duty. The system uses a duty ratio of 50%, so a setting of 833 is used. In a motor control program it is necessary to update the setting values in TAUA0CDR2, TAUA0CDR4, and TAUA0CDR6 each time a PWM period interrupt occurs.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TAUA0CDRn	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0	1

Remark: n = 2, 4, 6

(10) TAUA0 Channel Data Registers 3, 5, and 7 (TAUA0CDR3, TAUA0CDR5, and TAUA0CDR7)

These registers set the dead time value. The system maintains a dead time of 2 µs, so a setting of 132 is used.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TAUA0CDRn	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0

Remark: n = 3, 5, 7

(11) TAUA0 Channel Real-Time Output Control Register (TAUA0TRC)

This register sets the real-time trigger of slave channel 1. Each bit in TAUA0TRC corresponds with a channel.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TAUA0TRC	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

(12) TAUA0 Channel Output Enable Register (TAUA0TOE)

This register enables timer output on pins TA0_O0 and TA0_O2 to TA0_O7. Each bit in TAUA0TOE corresponds with a channel.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TAUA0TOE	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1

(13) TAUA0 Channel Output Mode Register (TAUA0TOM)

This register sets the output mode of each channel. The timer channel (channel 0) is cleared to 0, and the slave channels (channels 2 to 7) are set to 1. The output mode of the slave channels is determined by this register and the output operating mode setting of the channel output configuration register (TAUA0TOC).

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TAUA0TOM	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0

(14) TAUA0 Channel Output Configuration Register (TAUA0TOC)

This register sets the output mode of each channel. For triangle wave modulation, each slave channel is set to 1. The timer channel is cleared to 0, and the slave channels (channels 2 to 7) are set to 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TAUA0TOC	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0

(15) Timer Output Level Register 0 (TAUA0TOL)

This register sets the output logic of each channel, controlling the forward and reverse phases. The system uses the TAUA0 channel real-time output register (TAUA0TRO) to logically invert the real-time output, so all bits in this register are cleared to 0.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TAUA0TOL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(16) TAUA0 Channel Dead Time Output Enable Register (TAUA0TDE)

The bits corresponding to the channels on which triangle PWM with dead time is generated are set to 1. Each pair of even/odd slave channels must have the same setting. (This setting takes effect only when the corresponding bits in TAUA0TOEn, TAUA0TOMn, and TAUA0TOCn are set to 1.)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TAUA0TDE	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0

Remark: n = 2 to 7

(17) TAUA0 Channel Dead Time Output Mode Register (TAUA0TDM)

The timing for adding dead time is set to 0 (at detection of duty cycle of higher even channel). Each pair of even/odd slave channels must have the same setting. (This setting takes effect only when the corresponding bits in TAUA0TOEn, TAUA0TOMn, TAUA0TOCn, and TAUA0TDEn are set to 1.)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TAUA0TDM	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Remark: n = 2 to 7

(18) TAUA0 Channel Dead Time Output Level Register (TAUA0TDL)

The phase for adding dead time is set to 1 (reverse phase). (This setting takes effect only when the corresponding bits in TAUA0TOEn, TAUA0TOMn, TAUA0TOCn, and TAUA0TDEn are set to 1.)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TAUA0TDL	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0

Remark: n = 2 to 7

(19) TAUA0 Channel Real-Time Output Enable Register (TAUA0TRE)

The bits corresponding to the channels on which the real-time output function is enabled are set to 1. The system generates real-time output (including modulation) on slave channels 2 to 7, so bits 2 to 7 are set to 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TAUA0TRE	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0

(20) TAUA0 Channel Real-Time Output Register (TAUA0TRO)

This register is a timer output buffer for the real-time output function. It is set to the output value of the timer of each channel. To control forward and reverse phases, the bits in TAUA0TRO that correspond to (TAUA0TO2, TAUA0TO3), (TAUA0TO4, TAUA0TO5), and (TAUA0TO6, TAUA0TO7) must be set exclusively. Caution is necessary, because the same waveforms will be output from (TAUA0TO2, TAUA0TO3), (TAUA0TO4, TAUA0TO5), and (TAUA0TO6, TAUA0TO7) if they are set to the same value.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TAUA0TRO	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0

(21) TAUA0 Channel Real-Time Output Control Register (TAUA0TRC)

The bit corresponding to the channel on which the real-time output trigger is generated is set to 1. The system uses channel 1 as the real-time output trigger generation channel, so bit 1 is set to 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TAUA0TRC	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

(22) TAUA0 Channel Modulation Output Enable Register (TAUA0TME)

This register enables/disables the PWM and real-time output modulation function. The setting changes each PWM period according to the Hall effect sensor value, so the setting shown below applies to the initial period only. The system sets bits 7 to 2 to 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TAUA0TME	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0

3.1.4 Starting Operation of Complementary Modulation Output Function

To start complementary modulation output, the bits in timer channel start register 0 (TS0) corresponding to channels 0 to 7 are set to 1. This starts PWM (three channels each of forward phase and reverse phase) output.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TAUA0TS	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

This is a trigger register, so when read the value of each bit is always 0. Whether timer operation is enabled or not can be checked by reading timer channel enable status register 0.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TAUA0TE	0	0	0	0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

For details of register functions and important notes, see V850E2/MN4 User's Manual [Hardware] (R01UH0011EJ).

Website and Support

Renesas Electronics Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry

Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Feb 27, 2012	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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