V850E2/MN4

A/D Converter Control

R01AN0923EJ0100
Rev.1.00
Feb 13, 2012

Introduction

This document explains how to set up the A/D converter (ADC) and also gives an outline of the operation and describes the procedures for using a sample program. The sample program converts the scan list of channel group (CG) 0 by using the software trigger in one-shot mode. The number of times conversion of the scan list is repeated can be set from one to four per CG in a specific register for a given channel, but is set to one in the sample program. Having finished converting the scan list, the sample program turns on an LED to reflect the result.

Target Device

V850E2/MN4 Microcontrollers

Contents

1. Overview

This sample program converts the scan list of CG0 by using the software trigger in one-shot mode. The number of times conversion of the scan list is repeated can be set from one to four per CG in a specific register for a given channel, but is set to one in the sample program.

An A/D conversion flow is given below. See section 4.1 “Flow Charts” for the details of the individual operations.

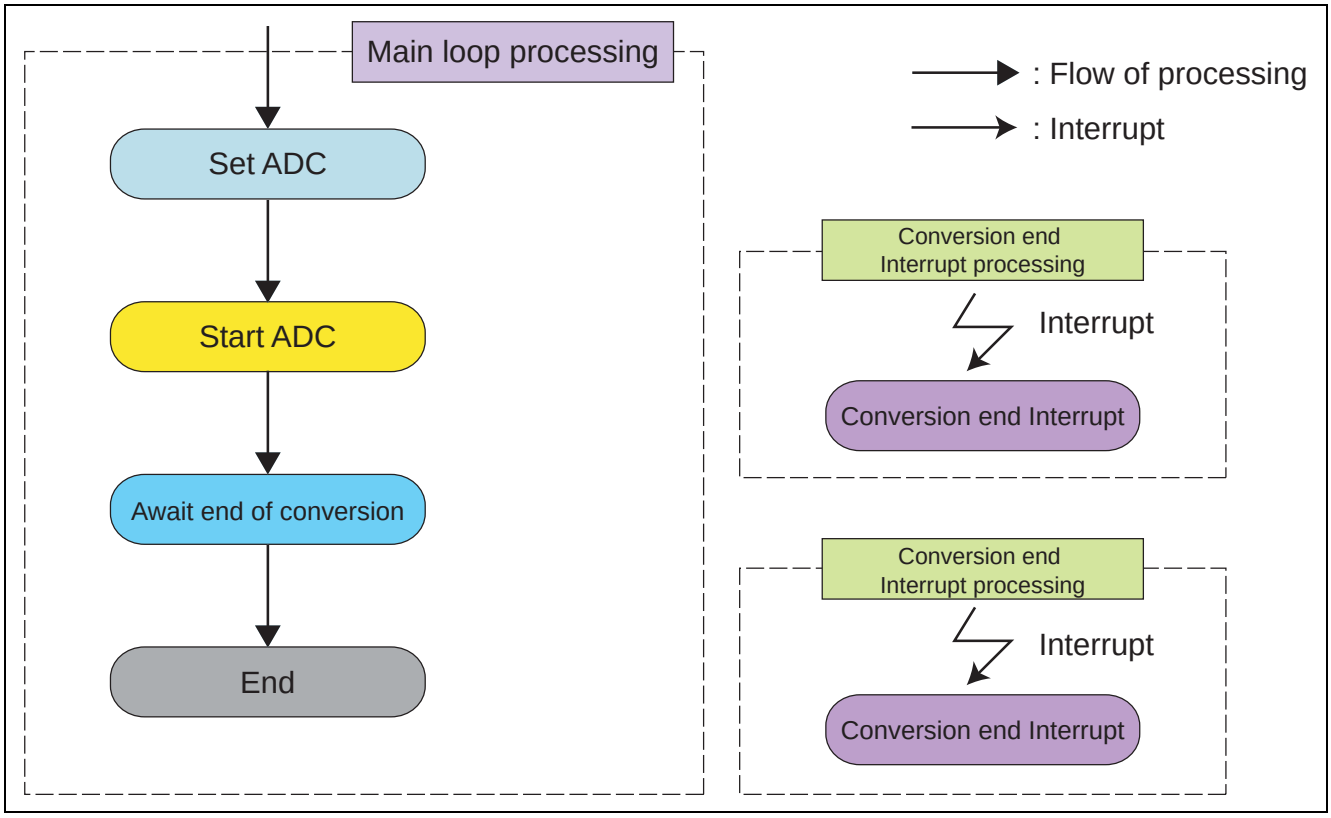

Figure 1.1 A/D Conversion Flow

1.1 Initialization

The general registers and functional pins are initialized.

<Port setup>

- Port n function control expansion registers (PFCEn)
- Port n function control registers (PFCn)
- Port n mode control registers (PMCn)
- Port n mode registers (PMn)

1.2 Basic Operation of the A/D Converter

This section describes the basic procedure of A/D conversion.

1. To optimize the start-up time between power being turned on and the start of conversion, adjust the stabilization time setting in the ADC stabilization counter register (ADCAnCNT).
2. To enable the A/D converter (set ADCAnCTL0.ADCAnCE to 1), switch the power on and set up the resolution, the ADCAn clock, the trigger mode, the conversion mode, the interrupt generation, the channel group, and other settings in the following registers.
   - ADCAnCTL1 register
   - ADCAnCGi registers
   - ADCAnIOCi registers
   - ADCAnTSELi registers
3. To check that a result of A/D conversion is within a certain value range, enable the conversion result limit comparison function for the desired channels (ADCAnCTL2.ADCAnRCKm) with upper and lower limits, and specify the lower limit in the ADCAnLL register and the upper limit in the ADCAnUL register.
4. To discharge the capacitor in the common sample-and-hold circuit before the conversion, set ADCAnCTL1.ADCAnDISC to 1 to enable the discharge function.
5. To enable or disable the buffer amplifier, set ADCAnCTL1.ADCAnBPC.
6. To enable the ADC, set ADCAnCTL0.ADCAnCE to 1. After the stabilization time has elapsed after power is turned on or after the standby mode is exited, the A/D converter is ready for A/D conversion.
7. Depending on the specified trigger mode, A/D conversion is started by a given channel group (CG).
   - Software trigger (setting ADCAnTRGi.ADCAnSTTi to 1)
   - Hardware trigger (input signals ADCAnTTRGi)
   If the A/D conversion of multiple CGs is triggered, the order of A/D conversion depends on the priority of the CGs.
8. When the A/D conversion on the channel specified by the ADCAnIOCi register end, the A/D conversion end interrupt (INTADCAnTi) for the given channel is generated.
9. Read the results from the A/D conversion result registers, ADCAnLCR, ADCAnDBiCR, and ADCAnCmCR.
10. Monitor the following registers.
    - ADCAnSTR1: To check whether the result of A/D conversion has been overwritten before being read according to the field of application.
    - ADCAnSTR0: To check whether the result of A/D conversion is within a specified range (only if the conversion result limit comparison function is enabled).
11. To set the A/D converter again, disable the A/D converter by setting ADCAnCTL0.ADCAnCE to 0.

2. Usage Environment

This section explains the circuit diagram and development environment to run this sample program.

2.1 Circuit Diagram

See “V850E2/MN4 Target Board User Manual: QB-V850E2MN4DUAL-TB (R20UT0683XJ)” for the details of the circuit diagram.

The main hardware resource used in this sample program is the A/D conversion pin (ANI00).

The LEDs are connected to port 13. The P13_7 pin is used for LED1. The P13_6 pin is used for LED2

2.2 Development Environment

It is necessary to install the tools that are listed below to run the sample program.

- CubeSuite+

The integrated development environment CubeSuite+ from Renesas Electronics provides various software development tools that are necessary for the user to develop applications. The user can use these tools seamlessly and easily in various development stages including coding, assembly, compilation, debugging using an emulator or simulator, and flash programming.

- MINICUBE

MINICUBE is a general-purpose in-circuit emulator from Renesas Electronics which adopts the JTAG interface system. It allows the user to debug an onboard real processor and provides highly transparent and stable emulation functionalities. An adapter is required to connect a TB board to MINICUBE.

- Multi

Green Hills software, Inc. integrated development tool suit.

- IAR Embedded Workbench

IAR Systems integrated development tool suit.

3. Software

This section describes the organization of the compressed files to be downloaded.

3.1 File Organization

The compressed files to be downloaded consist of the files that are listed below.

File Name (Tool Structure)	Description	Common Source File	CubeSuite+ File	Multi File
crtE.s	Hardware initialization processing		●	
startup.s				●
V850E2MN4.dir	Link directive file		●	
V850E2_MN4 ADC.ld				●
vector.s	Vector table			●
adc.h	Variable and function declarations	●		
main.c	Main processing	●		
initial.c	Software initialization processing	●		
adc_control.c	A/D converter control	●		
interrupt.c	Interrupt processing	●		

4. Sample Application

This section explains the A/D conversion of this sample program.

4.1 Flow Charts

The flow charts of this sample program are given below.

4.1.1 Main Processing

The main processing sets up and then starts A/D conversion. The A/D conversion is repeated and its state is indicated by the LEDs. When A/D conversion ends, the signal for LED1 is inverted.

Overwriting of a result of A/D conversion before it is read leads to the generation of an error interrupt (INTADCAnTERR) indicating this, and LED2 is turned on in response.

See section 4.1.2 for the details of the individual transfer processing.

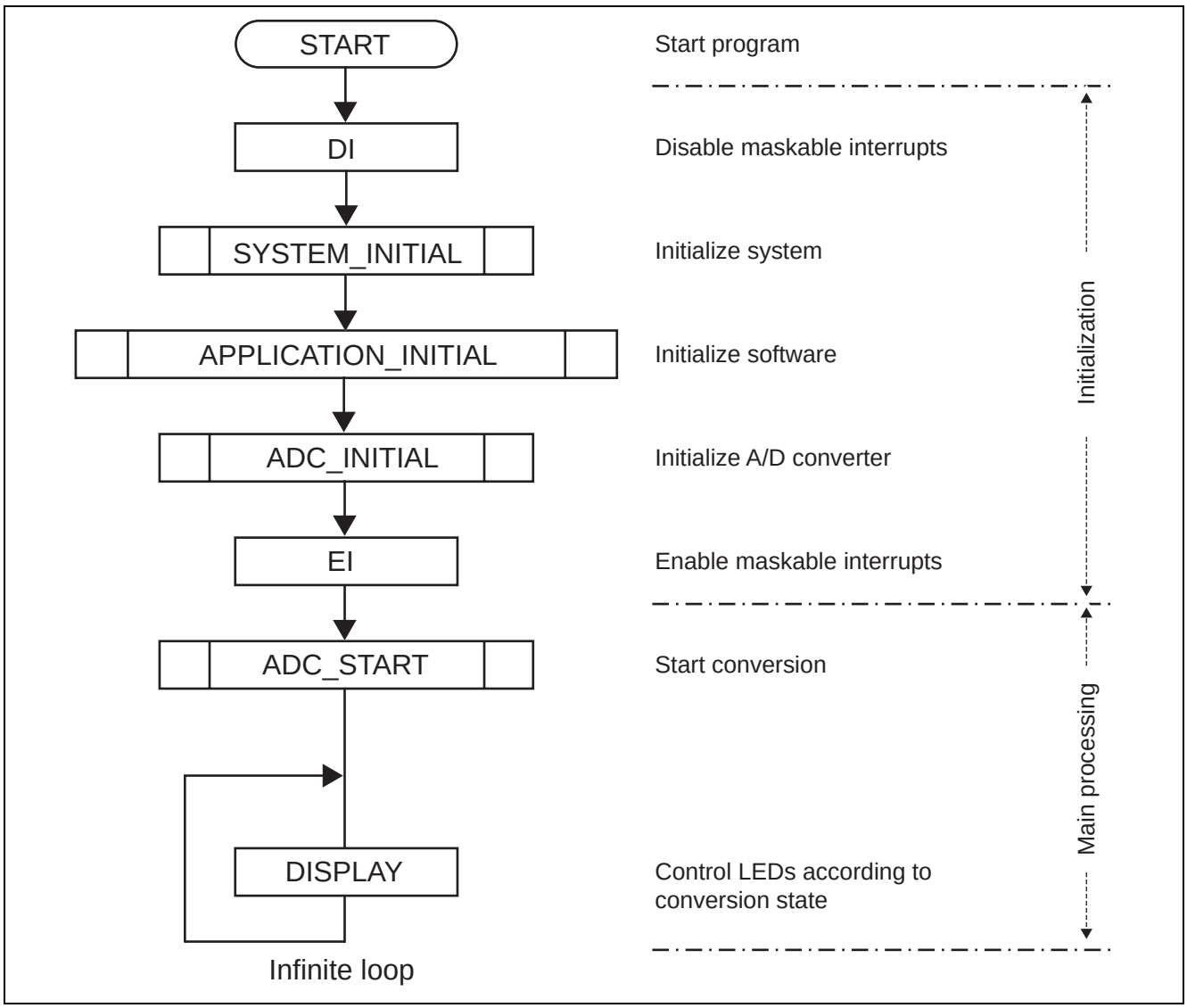

Figure 4.1 Main Processing Flowchart

4.1.2 Interrupt Processing Flow

When A/D conversion ends or an A/D conversion error occurs, interrupt processing is executed accordingly.

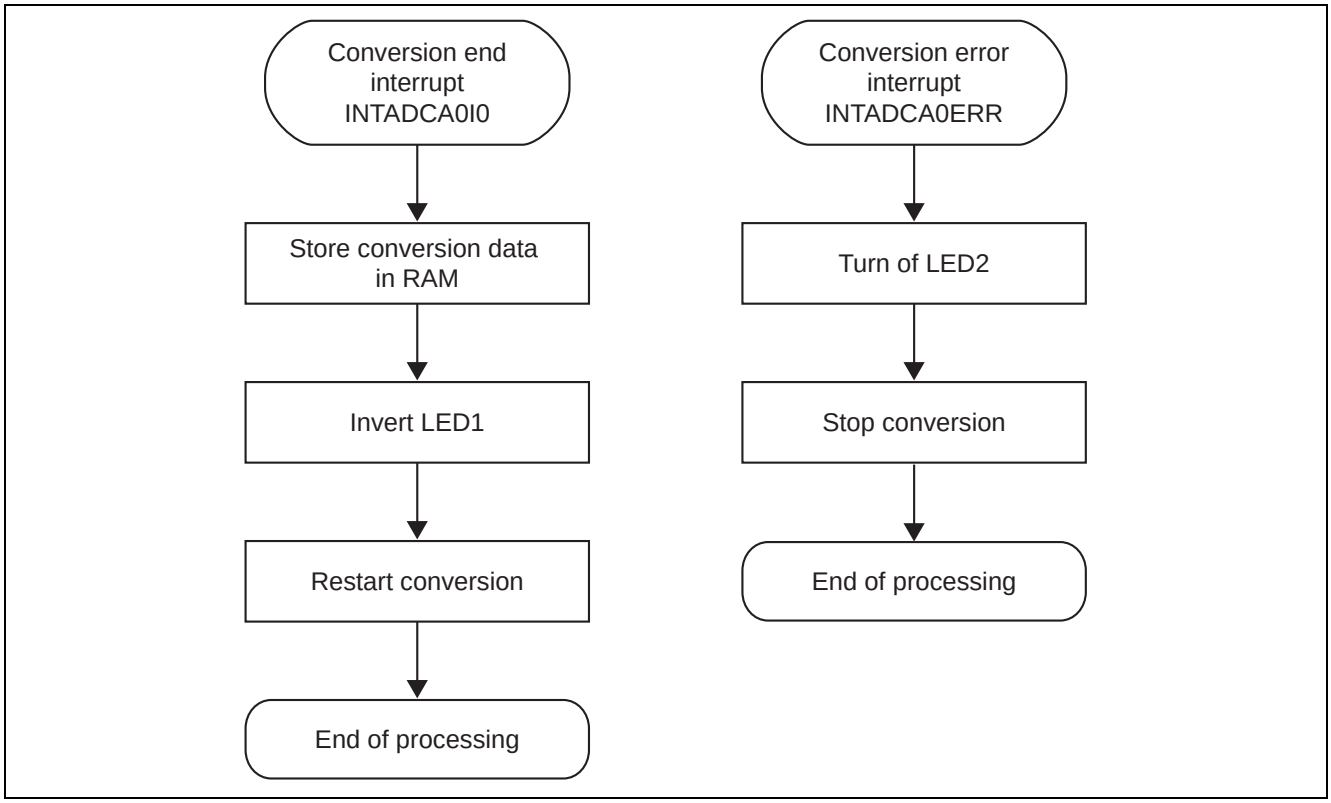

Figure 4.2 Interrupt Processing

4.2 Register Setup

This section explains how to set up the relevant registers according to the flow charts shown in section 4.1. The registers described below must be configured to control the A/D converter.

4.2.1 Port Setup

The LEDs are connected to port 13. The pertinent control registers must be set up as shown in the table below. The P13_7 pin is used for LED1. The P13_6 pin is used for LED2.

Macro	Pin	PMC	PFCE	PFC	PM	Corresponding function
PORT	P13_6	0	0	0	0	Port mode, output
	P13_7	0	0	0	0	Port mode, output

Setting examples

```
/* P13_6: LED2; port mode; output*/
/* P13_7: LED1; port mode; output*/
PFCE13 = 0x0000;
PFC13  = 0x0000;
PMC13  = 0x0000;
PM13   = 0x0000;
```

4.2.2 A/D Converter Stabilization Counter Register (ADCAnCNT)

This register specifies the stabilization time of the A/D converter.

Access This register can be read or written in 8-bit units.

Address <ADCAn_base_OS> + 114_H

Initial value 00_H. This register is initialized by any reset.

7	6	5	4	3	2	1	0
ADCAnCNT[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 25-13 ADCAnCNT Register Contents

Bit Position	Bit Name	Description
7 to 0	ADCAn CNT[7:0]	These bits specify the stabilization counter value. Stabilization time = ADCAnCNT[7:0] × clock cycles (PCLK)

Figure 4.3 ADCAnCNT Register Format

Setting example

```
ADCA0CNT   = 0xff;        /* stabilization counter */
```

4.2.3 A/D Converter Mode Control Register 1 (ADCAnCTL1)

This register specifies the conversion mode and controls the conversions.

Access This register can be read or written in 32-bit units.

Address <ADCAn_base_OS> + 104_H

Initial value $0100\ 0008_H$. This register is initialized by any reset.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADCAnT2ETS [1:0]		ADCAnT1ETS [1:0]		ADCAnT0ETS [1:0]		0	ADCAn CRAC	0	0	ADCAn MD1	ADCAn MD0	0	0	ADCAn DISC	ADCAn RCL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADCAn CTYP	0	0	ADCAnSTL	ADCAnFR[3:0]				0	ADCAnTRM[2:0]			ADCAn BPC	0	0	ADCAn GPS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 25-10 ADCAnCTL1 Register Contents (1/3)

Bit Position	Bit Name	Description
31 to 26	ADCAn TiETS[1:0]	These bits specify the valid edge of the hardware trigger signal ADCAnTTRGi. ADCAn TiETS1 / ADCAn TiETS0 / Valid Edge 0 / 0 / No valid edge detection (no acknowledgment) 0 / 1 / Rising edge 1 / 0 / Falling edge 1 / 1 / Rising and falling edges
24	ADCAn CRAC	This bit specifies the alignment of the A/D conversion and diagnostic conversion results. 0: Right-aligned 1: Left-aligned
21	ADCAnMD1	This bit specifies the A/D conversion start trigger for all CGs. 0: Software trigger 1: Hardware trigger and software trigger This setting is valid for all CGs. Triggers are only detected when the A/D converter is enabled. For details, see *25.3.5 "Starting A/D conversion (start triggers)" on page 1670* .
20	ADCAnMD0	This bit specifies the A/D conversion mode for CG0. 0: One-shot conversion mode The number of repetitions is specified by ADCAnCTL0.ADCAnSCTi[1:0] for each CG. 1: Continuous conversion mode This setting applies to the A/D conversion of CG0 only. CG1 and CG2 are always operated in the one-shot conversion mode. For details, see *25.3.4 "A/D conversion modes" on page 1667* .
17	ADCAnDISC	This bit enables or disables the discharge function. 0: Disable 1: Enable For details, see *25.3.15 "Discharge function (product dependent)" on page 1699* .

Figure 4.4 ADCAnCTL1 Register Format (1/3)

Table 25-10 ADCAnCTL1 Register Contents (2/3)

Bit Position	Bit Name	Description
16	ADCAnRCL	This bit specifies whether the A/D conversion results in ADCAnCmCR and ADCAnDBiCR are retained after reading them. 0: Retain the A/D conversion result until it is overwritten by the next A/D conversion result. 1: Clear the A/D conversion result after reading it.
15	ADCAnCTYP	This bit specifies the resolution mode. 0: 12-bit resolution (product dependent) 1: 10-bit resolution
12	ADCAnSTL	This bit specifies the ADCAnCNVi signal level. 0: When ADCAnCNVi = L, CGi is not undergoing conversion. When ADCAnCNVi = H, CGi is undergoing conversion. 1: When ADCAnCNVi = H, CGi is not undergoing conversion. When ADCAnCNVi = L, CGi is undergoing conversion.
11 to 8	ADCAnFR [3:0]	These bits specify the ADCAn clock ADCAnTCLK.

ADCAnFR[3:0]	ADCAn Clock
0000	PCLK/2
0001	PCLK/3
0010	PCLK/4
0011	PCLK/5
0100	PCLK/6
0110	PCLK/8
1000	PCLK/10
1010	PCLK/12
1100	PCLK/14
1110	PCLK/16
Other than the above	Setting prohibited

Figure 4.5 ADCAnCTL1 Register Format (2/3)

Table 25-10 ADCAnCTL1 Register Contents (3/3)

Bit Position	Bit Name	Description
6 to 4	ADCAnTRMi (product dependent)	These bits specify the interrupt behavior when the start trigger for the A/D conversion of a higher priority CG is input (or when transitioning to the ADCHALT mode is requested). 0: Interrupt the current A/D conversion of CGi, and start the A/D conversion of the higher priority CG (or enter the ADCHALT mode). 1: Finish the current CGi channel conversion, interrupt A/D conversion of the CG, and start the A/D conversion of the higher priority CG (or enter the ADCHALT mode). A/D conversion of CGi is continued as soon as all pending A/D conversions of higher priority CGs have been completed (or the ADCHALT mode has been exited). The priority is as follows: ADCHALT > CG2 > CG1 > CG0 For details, see *(1) "Order of A/D conversion" on page 1666*.
3	ADCAnBPC	This bit enables or disables the buffer amplifier function. 0: Disable 1: Enable For details, see *25.3.16 "Buffer amplifier function" on page 1699* .
0	ADCAnGPS	This bit turns ADCAn on or off. 0: Power off 1: Power on The A/D converter needs time to stabilize after being turned on. (For details, see *25.3.17 "Stabilization control" on page 1700*).

Figure 4.6 ADCAnCTL1 Register Format (3/3)

Setting example

```
ADCA0CTL1  = 0x00028001;        /* no detection of hard edge;
                                   right aligned conversion result;
                                   software trigger;
                                   one shot mode;
                                   discharge on;
                                   keep conversion result after read-out;
                                   10bit resolution mode;
                                   ADCATCNV0,1,2=L means no conversion;
                                   ADCATCNV0,1,2=H means running conversion;
                                   1/2 A/D Frequency configuration */
```

4.2.4 A/D Converter Channel Group Register i (ADCAnCGi)

This register creates a scan list for the corresponding CG. The channels specified in the scan list are converted in ascending order.

In addition, ADCAnCG0.ADCAnDIAG can be used to enable or disable the diagnosis of A/D conversion that uses the reference voltage signal (ADDIAGOUT).

Access This register can be read or written in 32-bit units. Because this register has a master/slave configuration, a new A/D conversion channel can be specified for the master register during A/D conversion. The timing at which the master register value is transferred to the slave register is as follows:

- If CGi is not undergoing A/D conversion, the value is transferred one clock cycle (PCLK) after writing to the master register.
- If CGi is undergoing A/D conversion, the value is transferred when the CGi scan list conversion currently being executed ends.
- If the CGi stop trigger bit (the ADCAnSPi bit) is set after a write to this register, the value is transferred when A/D conversion stops.

Address <ADCAn_base_USER> + i × 4_H

Initial value $0000\ 0000_H$. This register is initialized by any reset.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADCAn DIAG	0	0	0	0	0	0	0	ADCAnCGiS[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADCAnCGiS[15:00]															
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 25-11 ADCAnCGi Register Contents

Bit Position	Bit Name	Description
31	ADCAnDIAG	This bit enables or disables the diagnostic A/D conversion that uses the reference voltage signal ADDIAGOUT and is executed at the end of the A/D conversion of CG0. 0: Disable A/D conversion that uses the ADDIAGOUT signal. 1: Convert the ADDIAGOUT signal. This bit can only be specified for ADCAnCG0. Clear this bit for the ADCAnCG1 and ADCAnCG2 registers.
23 to 00	ADCAnCGiS [23:00]	These bits specify the analog input signals to be converted for CGi. 0: Do not convert the analog input ADCAnIm. 1: Convert the analog input ADCAnIm. **Note**Clear bits corresponding to channels that are not provided by this microcontroller.

Figure 4.7 ADCAnCGi Register Format

Setting example

```
ADCA0CG0   = 0x00000001;          /* conversion of ADDIAGOUT(AVdd) is not available;
                                     ANI00 conversion */
```

4.2.5 A/D Converter Interrupt Control Register i (ADCAnIOCi)

The A/D conversion end interrupt INTADCAnTi can be generated when the A/D conversion of a certain channel has been completed.

This register specifies the channels for which the interrupt INTADCAnTi is generated on the completion of A/D conversion.

If ADCAnIOCi is cleared to 0000 0000H, the interrupt INTADCAnTi is automatically generated on the completion of A/D conversion of CGi.

Access This register can be read or written in 32-bit units. It can be written at any time, even when the A/D converter is enabled (by setting ADCAnCTL0.ADCAnCE to 1). The new value takes effect after the current A/D conversion of CGi has been completed.

Address <ADCAn_base_USER> + $0C_H$ + i × 4_H

Initial value $0000\ 0000_H$. This register is initialized by any reset.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADCAnCG0IDG	0	0	0	0	0	0	0	ADCAnCGil[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADCAnCGil[15:00]															
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 25-12 ADCAnIOCi Register Contents

Bit Position	Bit Name	Description
31	ADCAn CG0IDG	This bit specifies whether the interrupt INTADCAnTi is generated on completion of the A/D conversion that uses the reference voltage when the diagnostic mode is enabled for CG0 (by setting ADCAnCG0.ADCAnDIAG to 1). 0: Do not generate the A/D conversion end interrupt INTADCAnTi. 1: Generate the A/D conversion end interrupt INTADCAnTi. This bit can only be specified for ADCAnIOC0. Clear this bit for the ADCAnIOC1 and ADCAnIOC2 registers. For details, see *(1) "A/D conversion circuit diagnosis" on page 1685.*
23 to 00	ADCAn CGil[23:00]	These bits specify whether the A/D conversion end interrupt INTADCAnTi is generated on A/D conversion completion of channel m. 0: Do not generate the A/D conversion end interrupt INTADCAnTi. 1: Generate the A/D conversion end interrupt INTADCAnTi. **Note**Clear bits corresponding to channels that are not provided by this microcontroller.

Note Because the ADCAnIOCi register is associated with the ADCAnCGi register, their buffer registers must be updated simultaneously. Because the update is performed when the ADCAnCGi register is written to, always write to the ADCAnIOCi register before the ADCAnCGi register when changing the interrupt generation for a CG.

Figure 4.8 ADCAnIOCi Register Format

Setting example

```
ADCA0IOC0  = 0x00000001;        /* ADCATINT0 does not output at the end of channel diag conversion;
                                   ADCATINT0 output at the end of channel 00 (CG0) conversion */
```

4.2.6 A/D Converter Mode Control Register 0 (ADCAnCTL0)

This register enables or disables the A/D converter. In addition, it specifies the number of repetitions in the one-shot conversion mode and whether to generate error interrupt requests when an A/D conversion is overwritten before it is read.

Access This register can be read or written in 16-bit units.

Address <ADCAn_base_OS> + 100_H

Initial value 0000_H. This register is initialized by any reset.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	ADCAn OEM4	ADCAnOEM[3:1]			ADCAn OEM0	ADCAn CE	0	ADCAnSCT2 [1:0]		ADCAnSCT1 [1:0]		ADCAnSCT0 [1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 25-9 ADCAnCTL0 Register Contents (1/2)

Bit Position	Bit Name	Description
12	ADCAn OEM4	This bit specifies whether the error interrupt INTADCAnTERR is generated when an A/D conversion result in the ADCAnLCR register is overwritten before it is read. 0: Generate the error interrupt INTADCAnTERR when an A/D conversion result is overwritten. 1: Do not generate the error interrupt INTADCAnTERR. For details, see *(1) "Conversion result overwrite check function" on page 1682.*
11 to 9	ADCAn OEM[3:1]	These bits specify whether the error interrupt INTADCAnTERR is generated when an A/D conversion result in an ADCAnDBiCR register is overwritten before it is read. 0: Generate the error interrupt INTADCAnTERR when an A/D conversion result is overwritten. 1: Do not generate the error interrupt INTADCAnTERR. CGI is controlled by the ADCAnOEM(i+1) bit. For details, see *(1) "Conversion result overwrite check function" on page 1682.*

Figure 4.9 ADCAnCTL0 Register Format (1/2)

Table 25-9 ADCAnCTL0 Register Contents (2/2)

Bit Position	Bit Name	Description
8	ADCAn OEM0	This bit specifies whether the error interrupt INTADCAnTERR is generated when an A/D conversion result in the ADCAnCmCR register is overwritten before it is read. 0: Generate the error interrupt INTADCAnTERR when an A/D conversion result is overwritten. 1: Do not generate the error interrupt INTADCAnTERR. For details, see *(1) "Conversion result overwrite check function" on page 1682.*
7	ADCAnCE	This bit enables or disables the A/D converter. 0: Disable the A/D converter. 1: Enable the A/D converter. Note that A/D conversion only starts when there is a hardware or software trigger (ADCAnTRGi.ADCAnSTTi) if ADCAnCTL0.ADCAnCE is set to 1. Also note that the A/D converter needs time to stabilize after it has been enabled. Start triggers are acknowledged even immediately after turning the power on. A/D conversion starts after the stabilization counter ADCAnCNT reaches 00_H.
5 to 0	ADCAn SCTi[1:0]	These bits specify the number of scan list conversions for CG1, CG2, and CG0 while it is in the one-shot conversion mode.

ADCAn SCTi1	ADCAn SCTi0	Number of CGi Scan List Conversions
0	0	1
0	1	2
1	0	3
1	1	4

Figure 4.10 ADCAnCTL0 Register Format (2/2)

Setting example

```
ADCA0CTL0 = 0x0080;
            /* ADCATERR which is generated by ADCA0LCR register overwrite admitted;
            ADCATERR which is generated by ADCA0DBiCR register overwrite admitted;
            ADCATERR which is generated by ADCA0CmCR register overwrite admitted;
            A/D Controller enable ON;
            1-time conversion of CG0 scanlist(channel 00) */
```

4.2.7 A/D Converter Software Trigger Register i (ADCAnTRGi)

This trigger register is the trigger register for starting the A/D conversion of CGi.

Access This register can be written in 8-bit units. When this register is read, 00_H is always returned.

Address <ADCAn_base_USER> + $A4_H + i \times 4_H$

Initial value 00_H. This register is initialized by any reset.

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	ADCAn STTi
W	W	W	W	W	W	W	W

Table 25-19 ADCAnTRGi Register Contents

Bit Position	Bit Name	Description
0	ADCAnSTTi	This bit starts the A/D conversion of CGi. 0: No function 1: Start the A/D conversion of CGi.

Figure 4.11 ADCAnTRGi Register Format

Setting example

```
ADCA0TRG0 = 0x01;       /* conversion start */
```

4.2.8 A/D Conversion Result Registers (ADCAnLCR, ADCAnCmCR, and ADCAnDBiCR)

ADCAnLCR — A/D converter latest conversion result register

ADCAnCmCR — A/D converter conversion result register for channel m

ADCAnDBiCR — DMA buffer register of CGi

Access This register can be read in 32-bit units.

- The upper 16 bits store the A/D conversion result status.
- The lower 16 bits store the A/D conversion result.

Address <ADCAn_base_USER> + $A0_H$

Initial value $0300\ 0000_H$. This register is initialized by any reset.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	ADCAn LCG[1:0]		ADCAn LER1	ADCAn LER0	ADCAn LUR	ADCAnLCN[4:0]				
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADCAnLCR[15:00]															
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 25-23 ADCAnLCR Register Contents (1/2)

Bit Position	Bit Name	Description
25, 24	ADCAn LCG[1:0]	These bits indicate the CG to which the conversion result stored in ADCAnLCR[15:00] belongs.

ADCAn LCG1	ADCAn LCG0	Channel Group
0	0	CG0
0	1	CG1
1	0	CG2
1	1	None

Bit Position	Bit Name	Description
23	ADCAn LER1	This bit indicates the overwrite error status. 0: Not overwritten 1: Overwritten This error flag is cleared by setting ADCAnSTC2.ADCAnLERC1.
22	ADCAn LER0	This bit indicates the status of the A/D conversion result limit comparison. 0: The conversion results are within the specified range. 1: The conversion results are not within the specified range. This error flag is cleared by setting ADCAnSTC2.ADCAnLERC0.
21	ADCAn LUR	This bit indicates the update status of the A/D conversion result. 0: The A/D conversion result has been read from the ADCAnLCR register. 1: The A/D conversion result is new and has not been read from the ADCAnLCR register. This bit is cleared by reading it.
20 to 16	ADCAn LCN[4:0]	These bits indicate the channel number to which the conversion result stored in the ADCAnLCR[15:00] bits belongs. 00001 × m = CHm

Figure 4.12 ADCAnLCR Register Format (1/2)

Table 25-23 ADCAnLCR Register Contents (2/2)

Bit Position	Bit Name	Description
15 to 0	ADCAn LCR [15:00]	These bits indicate the A/D conversion result. The resolution and alignment depend on ADCAnCTL1.ADCAnCTYP and ADCAnCTL1.ADCAnCRAC as follows:

ADCAn CTL1. ADCAn CTYP	ADCAn CTL1. ADCAn CRAC	Resolution and Alignment	A/D Conversion Result Value Bit Position
0	0	12-bit resolution, right-aligned	[11:00] of ADCAnLCR[15:00]
0	1	12-bit resolution, left-aligned	[15:04] of ADCAnLCR[15:00]
1	0	10-bit resolution, right-aligned	[09:00] of ADCAnLCR[15:00]
1	1	10-bit resolution, left-aligned	[15:06] of ADCAnLCR[15:00]

Note When A/D conversion is performed by using the internal reference voltage, the A/D conversion result is stored in the ADCAnDGCR register, not in the ADCAnLCR, ADCAnCmCR, and ADCAnDBiCR registers. (For details, see *(4) "ADCAnDBiCRL – DMA buffer register of CGi (product dependent)" on page 1722.*)

Figure 4.13 ADCAnLCR Register Format (2/2)

Access This register can be read in 32-bit units.

- The upper 16 bits store the A/D conversion result status.
- The lower 16 bits store the A/D conversion result.

Address <ADCAn_base_USER> + $3C_H$ + m × 4_H

Initial value 0300 0000_H + m × 0001 0000_H. This register is initialized by any reset.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	ADCAn CmCG[1:0]		ADCAn CmER1	ADCAn CmER0	ADCAn CmUR	ADCAnCmCN[4:0]				
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADCAnCmCR[15:00]															
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Notes

1. The functions of each bit are the same as those of the ADCAnLCR register, except that here they affect the latest A/D conversion result for a specific channel instead of the latest A/D conversion results for all channels. (For details, see *Table 25-23 "ADCAnLCR Register Contents" on page 1716.*)
2. After a reset, the ADCAnCmCG[1:0] bits are set to 11_B.
3. If ADCAnCTL1.ADCAnRCL is cleared, the A/D conversion result in the ADCAnCmCR[15:00] bits is kept until it is overwritten by the next A/D conversion result.

   If ADCAnCTL1.ADCAnRCL is set, the ADCAnCmCR[15:00] bits are cleared by reading them.

Table 25-24 ADCAnCmCR Register Contents (1/2)

Bit Position	Bit Name	Description
25, 24	ADCAn CmCG [1:0]	These bits indicate the CG to which the conversion result stored in ADCAnCmCR[15:00] belongs.

ADCAn CmCG1	ADCAn CmCG0	Channel Group
0	0	CG0
0	1	CG1
1	0	CG2
1	1	None

Figure 4.14 ADCAnCmCR Register Format (1/2)

Table 25-24 ADCAnCmCR Register Contents (2/2)

Bit Position	Bit Name	Description
23	ADCAn CmER1	This bit indicates the overwrite error status. 0: Not overwritten 1: Overwritten This error flag reflects the value of ADCAnSTR1.ADCAnOWEm and is cleared by setting ADCAnSTC1.ADCAnQWECm.
22	ADCAn CmER0	This bit indicates the status of the A/D conversion result limit comparison. 0: The conversion results are within the specified range. 1: The conversion results are not within the specified range. This error flag reflects the value of ADCAnSTR0.ADCAnRCEm and is cleared by setting ADCAnSTC0.ADCAnRCECm.
21	ADCAn CmUR	This bit indicates the update status of the A/D conversion result. 0: The A/D conversion result has been read from the ADCAnCmCR register. 1: The A/D conversion result is new and has not been read from the ADCAnCmCR register. This bit is cleared by reading it.
20 to 16	ADCAn CmCN [4:0]	These bits indicate the channel number to which the conversion result stored in the ADCAnCmCR[15:00] bits belongs. 00001 × m = CHm
15 to 0	ADCAn CmCR [15:00]	These bits indicate the A/D conversion result. The resolution and alignment depend on ADCAnCTL1.ADCAnCTYP and ADCAnCTL1.ADCAnCRAC as follows:

ADCAn CTL1. ADCAn CTYP	ADCAn CTL1. ADCAn CRAC	Resolution and Alignment	A/D Conversion Result Value Bit Position
0	0	12-bit resolution, right-aligned	[11:00] of ADCAnCmCR[15:00]
0	1	12-bit resolution, left-aligned	[15:04] of ADCAnCmCR[15:00]
1	0	10-bit resolution, right-aligned	[09:00] of ADCAnCmCR[15:00]
1	1	10-bit resolution, left-aligned	[15:06] of ADCAnCmCR[15:00]

Note When A/D conversion is performed by using the internal reference voltage, the A/D conversion result is stored in the ADCAnDGCR register, not in the ADCAnLCR, ADCAnCmCR, and ADCAnDBiCR registers. (For details, see *(4) "ADCAnDBiCRL – DMA buffer register of CGi (product dependent)" on page 1722.*)

Figure 4.15 ADCAnCmCR Register Format (2/2)

Access This register can be read in 32-bit units.

- The upper 16 bits store the A/D conversion result status.
- The lower 16 bits store the A/D conversion result.

Address <ADCAn_base_USER> + $C4_H$ + i × 4_H

Initial value $0000\ 0000_H$ + i × $0100\ 0000_H$. This register is initialized by any reset.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	ADCAn DBiCG[1:0]		ADCAn DBiER1	ADCAn DBiER0	ADCAn DBiUR	ADCAnDBiCN[4:0]				
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADCAnDBiCR[15:00]															
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Note The functions of each bit are the same as those of the ADCAnLCR register, except that here they affect the latest A/D conversion result for CGi instead of the latest A/D conversion results for all CGs. (For details, see *Table 25-23 "ADCAnLCR Register Contents" on page 1716*.)

Table 25-25 ADCAnDBiCR Register Contents (1/2)

Bit Position	Bit Name	Description
25, 24	ADCAn DBiCG [1:0]	These bits indicate the CG to which the conversion result stored in ADCAnDBiCR[15:00] belongs. ADCAn DBiCG1 / ADCAn DBiCG0 / Channel Group 0 / 0 / CG0 0 / 1 / CG1 1 / 0 / CG2 1 / 1 / None The values of these bits are fixed because the conversion results and status of the same CG are always saved.
23	ADCAn DBiER1	This bit indicates the overwrite error status. 0: Not overwritten 1: Overwritten This error flag is cleared by setting ADCAnSTC2.ADCAnDBiERC1.
22	ADCAn DBiER0	This bit indicates the status of the A/D conversion result limit comparison. 0: The conversion results are within the specified range. 1: The conversion results are not within the specified range. This error flag is cleared by setting ADCAnSTC2.ADCAnDBiERC0.
21	ADCAn DBiUR	This bit indicates the update status of the A/D conversion result. 0: The A/D conversion result has been read from the ADCAnDBiCR register. 1: The A/D conversion result is new and has not been read from the ADCAnDBiCR register. This bit is cleared by reading it.

Figure 4.16 ADCAnDBiCR Register Format (1/2)

Table 25-25 ADCAnDBiCR Register Contents (2/2)

Bit Position	Bit Name	Description
20 to 16	ADCAn DBiCN [4:0]	These bits indicate the channel number to which the conversion result stored in the ADCAnDBiCR[15:00] bits belongs. 00001 × m = CHm
15 to 0	ADCAn DBiCR [15:00]	These bits indicate the A/D conversion result. The resolution and alignment depend on ADCAnCTL1.ADCAnCTYP and ADCAnCTL1.ADCAnCRAC as follows:

ADCAn CTL1. ADCAn CTYP	ADCAn CTL1. ADCAn CRAC	Resolution and Alignment	A/D Conversion Result Value Bit Position
0	0	12-bit resolution, right-aligned	[11:00] of ADCAnDBiCR[15:00]
0	1	12-bit resolution, left-aligned	[15:04] of ADCAnDBiCR[15:00]
1	0	10-bit resolution, right-aligned	[09:00] of ADCAnDBiCR[15:00]
1	1	10-bit resolution, left-aligned	[15:06] of ADCAnDBiCR[15:00]

Note When A/D conversion is performed by using the internal reference voltage, the A/D conversion result is stored in the ADCAnDGCR register, not in the ADCAnLCR, ADCAnCmCR, ADCAnDBiCR, and ADCAnDBiCRL registers. (For details, see *(5) "ADCAnDGCR – Diagnostic conversion result register" on page 1723.*)

Figure 4.17 ADCAnDBiCR Register Format (2/2)

Setting examples

```
adc_result[0] = ADCA0LCR;          /* read converted result */
adc_result[1] = ADCA0C00CR;        /* read converted result */
adc_result[2] = ADCA0DB0CR;        /* read converted result */
```

4.3 Function Specifications

This section describes the specifications for the functions that are used by the sample program.

4.3.1 Main Processing (main.c)

[Function Name]	main ()
[Function]	Calls necessary initialization functions before entering an infinite loop.
[Arguments]	None
[Return Value]	None
[Startup Method]	Enters the main function after hardware initialization.
[SFRs Used]	None
[Calling Function]	None
[Variables]	None
[File Name]	main.c
[Notes]	None

4.3.2 Software Initialization Processing (initial.c)

[Function Name]	port_initial()
[Function]	Sets up ports and their mode.
[Arguments]	None
[Return Value]	None
[Startup Method]	Call
[SFRs Used]	PFCE13, PFC13, PMC13, PM13
[Calling Function]	main()
[Variables]	None
[File Name]	initial.c
[Notes]	None

[Function Name]	cg_initial()
[Function]	Initializes the special clock frequency control register.
[Arguments]	None
[Return Value]	None
[Startup Method]	Call
[SFRs Used]	SFRCTL3
[Calling Function]	main()
[Variables]	None
[File Name]	initial.c
[Notes]	None

[Function Name]	hbus_initial()
[Function]	Initializes the AHB bus
[Arguments]	None
[Return Value]	None
[Startup Method]	Call
[SFRs Used]	ETARCFG0, ETARADRS0, ETARMASK0
[Calling Function]	main()
[Variables]	None
[File Name]	initial.c
[Notes]	None

[Function Name]	board_initial()
[Function]	Sets up the initial state of the LEDs.
[Arguments]	None
[Return Value]	None
[Startup Method]	Call
[SFRs Used]	P13
[Calling Function]	main()
[Variables]	None
[File Name]	initial.c
[Notes]	None

[Function Name]	ram_initial()
[Function]	Sets up the initial state of the user RAM.
[Arguments]	None
[Return Value]	None
[Startup Method]	Call
[SFRs Used]	None
[Calling Function]	main()
[Variables]	adc_result[]
[File Name]	initial.c
[Notes]	None

4.3.3 Control Processing (adc_control.c)

[Function Name]	adc_initial()
[Function]	Sets up the operation of the ADC.
[Arguments]	None
[Return Value]	None
[Startup Method]	Call
[SFRs Used]	ICADCA0ERR, ICADCA0I0, ADCA0CNT, ADCA0CTL1, ADCA0CG0, ACA0IOC0, ADCA0TSEL0, ADCA0CTL2, ADCA0LL, ADCA0UL, ADCA0CTL0, ADCA0TRG0
[Calling Function]	main()
[Variables]	None
[File Name]	adc_control.c
[Notes]	None

4.3.4 Interrupt Processing (interrupt.c)

[Function Name]	int_adca0i0()
[Function]	Processes A/D conversion end interrupt.
[Arguments]	None
[Return Value]	None
[Startup Method]	Request INTADCA0I0 is present in an unmasked state.
[SFRs Used]	ADCA0LCR, ADCA0TRG0, ADCA0C00CR, ADCA0DB0CR, P13
[Calling Function]	None
[Variables]	adc_result[]
[File Name]	interrupt.c
[Notes]	None

[Function Name]	int_adca0err()
[Function]	Processes A/D conversion error interrupt.
[Arguments]	None
[Return Value]	None
[Startup Method]	Request INTADCA0ERR is present in an unmasked state.
[SFRs Used]	P13, ADCA0CTL0
[Calling Function]	None
[Variables]	None
[File Name]	interrupt.c
[Notes]	None

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Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Feb 13, 2012	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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