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SH7080 Series

Using the DTC to Drive Clock Synchronous Data Transfer by the SCIF Mode

Introduction

This application note describes simultaneous transmission/reception of serial data by using the clock synchronous transfer function of the SCIF (serial communication interface with FIFO) and the data-transfer function of the DTC (data transfer controller). This application note is a summary for quick reference of information required in the design of user software.

Target Device

SH7086

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1. Specifications

In this sample application, the DTC's data-transfer functions and SCIF are used for clock-synchronous transmission and reception of serial data.

- The communications format is that for clock-synchronous transfer, and the rate of transfer is 100,000 bits/s.
- Thirty-two-byte block of data are simultaneously transmitted and received.
- DTC transfer for transmission is activated by the transmit FIFO data empty interrupt, with the transmit FIFO trigger number of the SCIF set to 8. The DTC transfers data for transmission from the on-chip RAM to the SCIF.
- DTC transfer for reception is activated by a receive FIFO data full interrupt, with the receive FIFO trigger number of the SCIF set to 1. The DTC transfers received data from the SCIF to the on-chip RAM.
- On completion of serial transmission and reception, interrupts are generated to perform end processing.

With the SCK3 pin as the output for the synchronizing clock signal, and the serial transmission and reception pins (TxD3 and RxD3) externally connected, the SCIF performs pseudo-full-duplex communications. An overview of operations in this sample application is shown in figure 1.

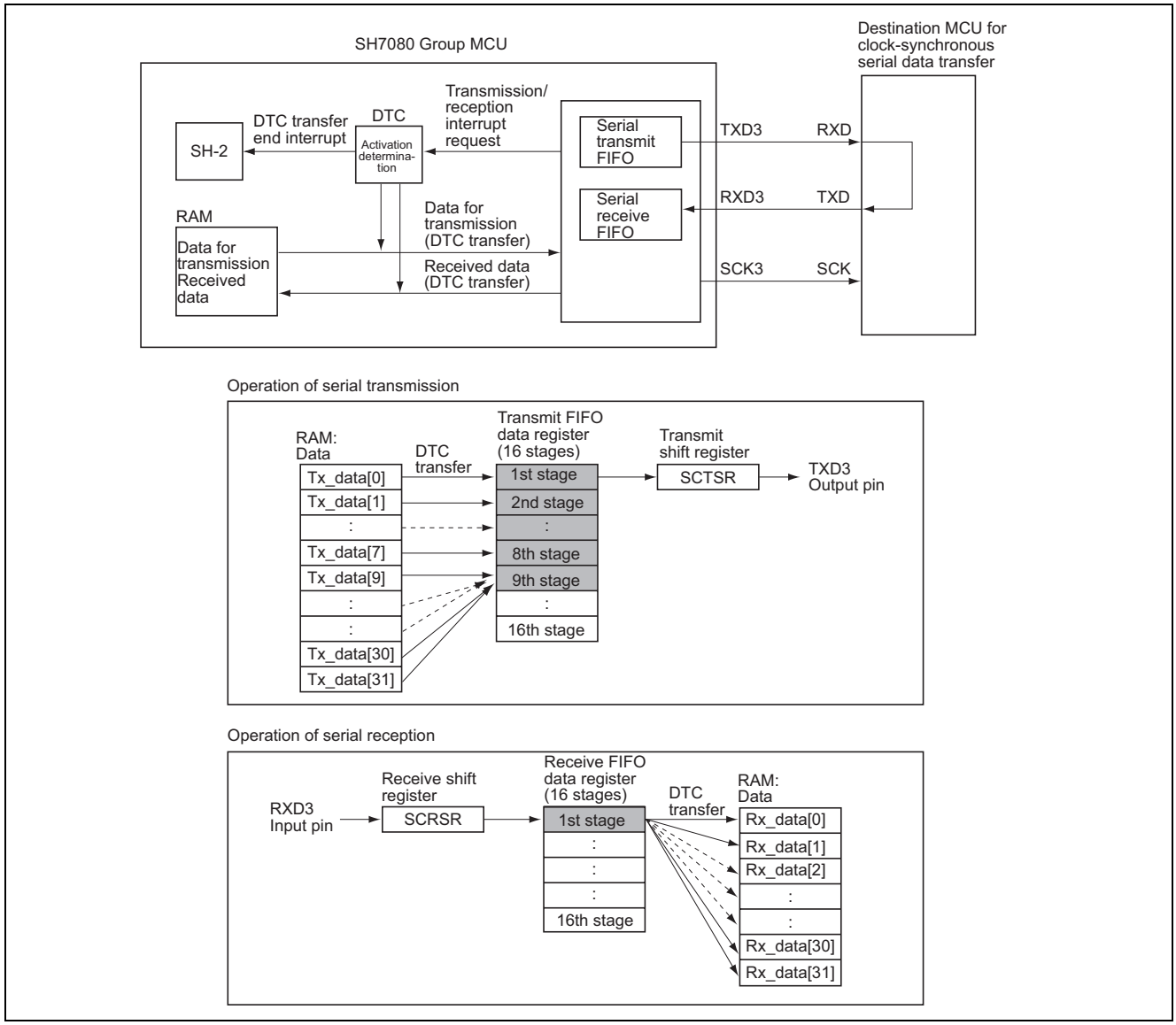


Figure 1 Overview of Transmission/Reception of Clock-Synchronous Data by the SCIF Using the DTC

2. Applicable Conditions

Applicable conditions for this sample application are shown in table 1.

Table 1 Applicable Conditions

Item	Setting	
Device	SH7086 (R5F70865)	
Device operating frequency	Internal clock	Iϕ = 80 MHz
	Bus clock	Bϕ = 40 MHz
	Peripheral clock	Pϕ = 40 MHz
	MTU2 clock	MPϕ = 40 MHz
	MTU2S clock	MIϕ = 40 MHz
Device operation mode	Single chip mode	
Development environment	High-performance Embedded Workshop Ver.4.03.00.001 SuperH RISC engine Standard Toolchain (V.9.1.0.0) SuperH RISC engine C/C++ Compiler (V.9.01.00) (manufactured by Renesas Technology)	
C compile options	Default setting -cpu=sh2 -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug -speed -gbr=auto -chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 -nologo	

3. Description of Modules Used

This section gives an operational overview of the main modules used in this sample application, i.e. the SCIF (Serial Communication Interface with FIFO) and DTC (Data Transfer Controller).

3.1 Operational Overview of Serial Communication Interface with FIFO (SCIF)

In clock synchronous transfer by the SCIF, transmission and reception of data are synchronized with clock pulses. An internal clock or an external clock signal from the SCK pin can be selected as the clock source. When an internal clock is selected, synchronizing clock signal is output from the SCK pin. When an external clock is selected, the synchronizing clock signal is input from the SCK pin. The length of the communications format is fixed to 8 bits.

An overview of clock synchronous mode is provided in table 2. In addition, a block diagram of the SCIF is shown in figure 2.

Table 2 Overview of SCIF (Synchronous Mode)

Item	Description
Number of channels	Single channel (SCIF3)
Clock source	For internal clock: Pϕ, Pϕ/4, Pϕ/16, Pϕ/64 (Pϕ: peripheral clock) For external clock: input clock on pin SCK3
Data format	Data length: 8 bits (fixed) Order: LSB first (fixed)
Bit rate	For internal clock: 250 to 5000 Kbps (Pϕ = 40 MHz) For external clock: up to 6666 Kbps (Pϕ= 40 MHz, external input clock of 6.6667 MHz)
Receive-error detection	Overrun errors
Interrupt request	• Transmit FIFO data empty interrupt (TXIF) • Receive FIFO data full interrupt (RXIF) • Break or overrun error interrupt (BRIF) • Receive error interrupt (ERIF)
Others	• When an internal clock has been selected, the synchronizing clock signal can be output from the SCK pin. • The following can be detected: the number of valid data stored in the transmit/receive FIFO data register, and the number of receive errors stored in the receive FIFO data register. • Data transfer by the DTC can be activated on detection of the transmit FIFO being empty or the receive FIFO being full.

Note: For details on the SCIF, see the section on serial communication interface with FIFO (SCIF) in SH7080 Series Hardware Manual.

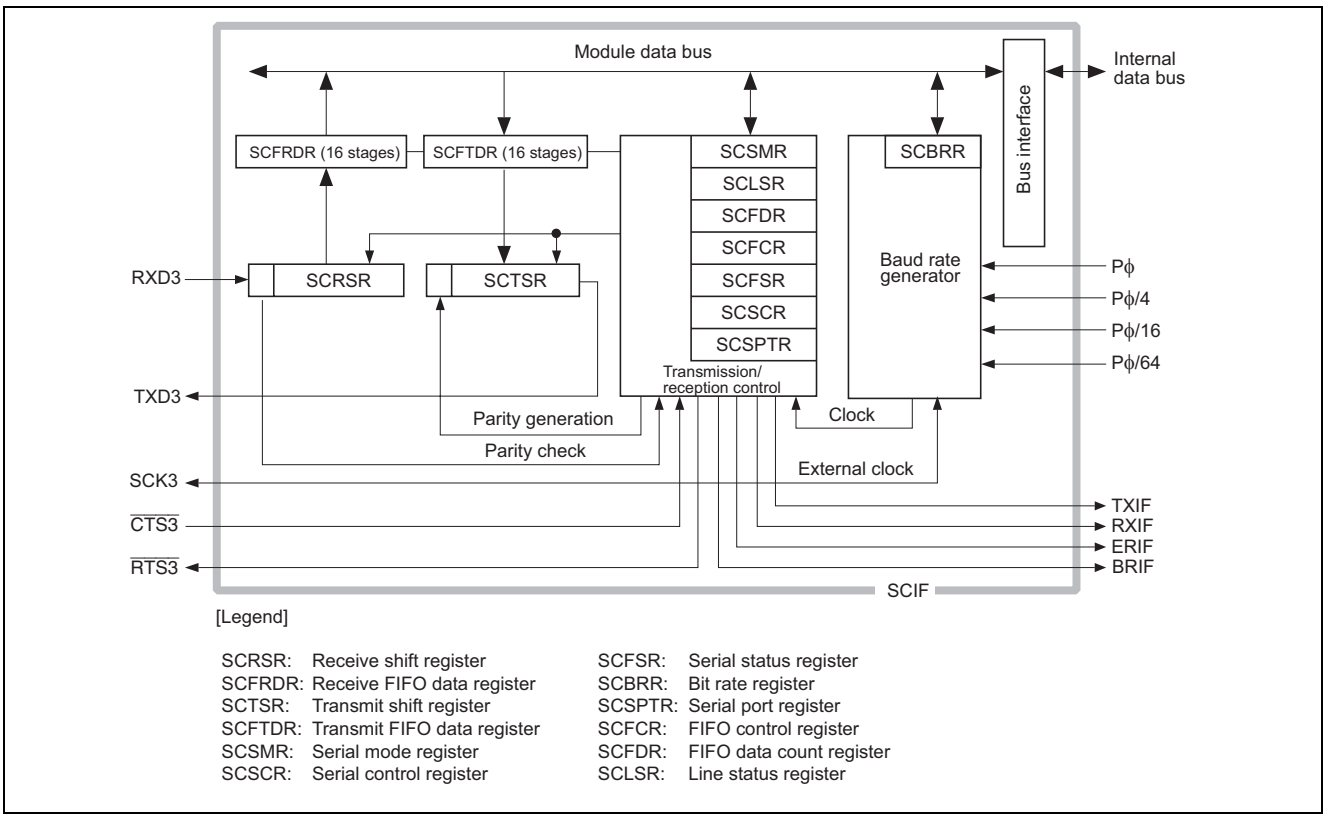


Figure 2 Brock Diagram of SCIF

- Receive Shift Register (SCRSR)
  SCRSR receives serial data. Data input at the RXD pin is loaded into SCRSR in the order received, LSB (bit 0) first, converting the data to parallel form. When one byte has been received, it is automatically transferred to SCRDR. The CPU cannot read from or write to SCRSR directly.

- Receive FIFO Data Register (SCFRDR)
  SCFRDR is a 16-stage 8-bit FIFO register that stores serial receive data. The SCIF completes the reception of one byte of serial data by moving the received data from the receive shift register (SCRSR) into SCFRDR for storage. Continuous reception is possible until 16 bytes are stored. The CPU can read from but not write to SCFRDR. If data is read when there is no received data in the SCFRDR, the value is undefined. When this register is full of received data, subsequent serial data are lost.

- Transmit Shift Register (SCTSR)
  SCTSR transmits serial data. The SCIF loads data for transmission from the transmit FIFO data register (SCFTDR) into SCTSR, and then transmits the data serially from the TXD pin, LSB (bit 0) first. After transmitting one data byte, the SCIF automatically loads the next data for transmission from SCFTDR into SCTSR and starts transmitting again. The CPU cannot read or write to SCTSR directly.

- Transmit FIFO Data Register (SCFTDR)
  SCFTDR is a 16-stage 8-bit FIFO register that stores data for serial transmission. When the SCIF detects that the transmit shift register (SCTSR) is empty, it moves data for transmission written in the SCFTDR into SCTSR and starts serial transmission. Continuous serial transmission is performed until there is no data for transmission left in SCFTDR. SCFTDR can always be written to by the CPU. When SCFTDR is full of data for transmission (16 bytes), no more data can be written. If writing of new data is attempted, the data are ignored.

- Serial Mode Register (SCSMR)
  SCSMR is a 16-bit register that specifies the SCIF serial communication format and selects the clock source for the baud rate generator. The CPU can always read from and write to SCSMR.

- Serial Control Register (SCSCR)
  SCSCR is a 16-bit register that operates the SCIF transmission/reception, enables or disables interrupt requests, and selects the transmit/receive clock source. The CPU can always read from and write to SCSCR.

- Serial Status Register (SCFSR)
  SCFSR is a 16-bit register. The upper 8 bits indicate the number of receive errors in the SCFRDR data, and the lower 8 bits indicate the status flag indicating SCIF operating state. The CPU can always read from and write to SCFSR, but cannot write 1 to the status flags (ER, TEND, TDFE, BRK, RDF, and DR). These flags can be cleared to 0 only if they have first been read (after being set to 1). Bits 3 (FER) and 2 (PER) are read-only bits that cannot be written.

- Bit Rate Register (SCBRR)
  SCBRR is an 8-bit register that, together with the baud rate generator clock source selected by the CKS1 and CKS0 bits in the serial mode register (SCSMR), determines the serial transmit/receive bit rate. The CPU can always read from and write to SCBRR. SCBRR is initialized to H'FF by a power-on reset.

- Serial Port Register (SCSPTR)
  SCSPTR is a 16-bit register that controls input/output and data for the pins multiplexed to the SCIF function. Bits 7 and 6 can control the $\overline{\text{RTS}}$ pin, bits 5 and 4 can control the $\overline{\text{CTS}}$ pin, and bits 3 and 2 can control the SCK pin. Bits 1 and 0 can be used to output data to the TXD pin, so that they control break of serial transfer.

- FIFO Control Register (SCFCR)
  SCFCR is a 16-bit register that resets the number of data in the transmit and receive FIFO registers, sets the trigger data number, and contains an enable bit for loop-back testing. SCFCR can always be read from and written to by the CPU.

- FIFO Data Count Register (SCFDR)
  SCFDR is a 16-bit register that indicates the number of data stored in the transmit FIFO data register (SCFTDR) and the receive FIFO data register (SCFRDR). It indicates the number of data for transmission in SCFTDR with the upper eight bits, and the number of received data in SCFRDR with the lower eight bits. SCFDR can always be read from by the CPU.

- Line Status Register (SCLSR)
  SCLSR is a 16-bit readable/writable register that can always be read from and written to by the CPU. However, a 1 cannot be written to the ORER flag. This flag can be cleared to 0 only if it has first been read from (after being set to 1).

3.2 Operational Overview of Data Transfer Controller (DTC)

Interrupt requests from on-chip peripheral modules can activate data transfer by the data transfer controller (DTC).

An overview of the DTC is given in Table 3. In addition, a block diagram of the DTC is shown in figure 3.

Table 3 Overview of DTC

Item	Description
Number of channel	Data can be transferred over any number of channels
Transfer mode	• Normal/repeat/block transfer modes are selectable • Transfer source and destination addresses can be selected from increment/decrement/fixed
Data transfer size	Size of data for data transfer can be specified as byte, word, or longword
Interrupt request	A CPU interrupt can be requested for the interrupt that activated the DTC • A CPU interrupt can be requested after one data transfer completion • A CPU interrupt can be requested after the specified data transfer completion
Others	• Chained transfer (multiple rounds of data transfer performed in response to a single activation source) is available • The transfer source and destination addresses can be specified by 32 bits to select a 4-Gbyte address space directly • Read skip of transfer information can be specified • Writeback skip is executed for the fixed transfer source and destination addresses • Short address mode is specifiable • Bus release timing is selectable from five types • Priority of the DTC activation can be selected from two types

Note: For details on the DTC, see the section on the data transfer controller (DTC) in SH7080 Series Hardware Manual.

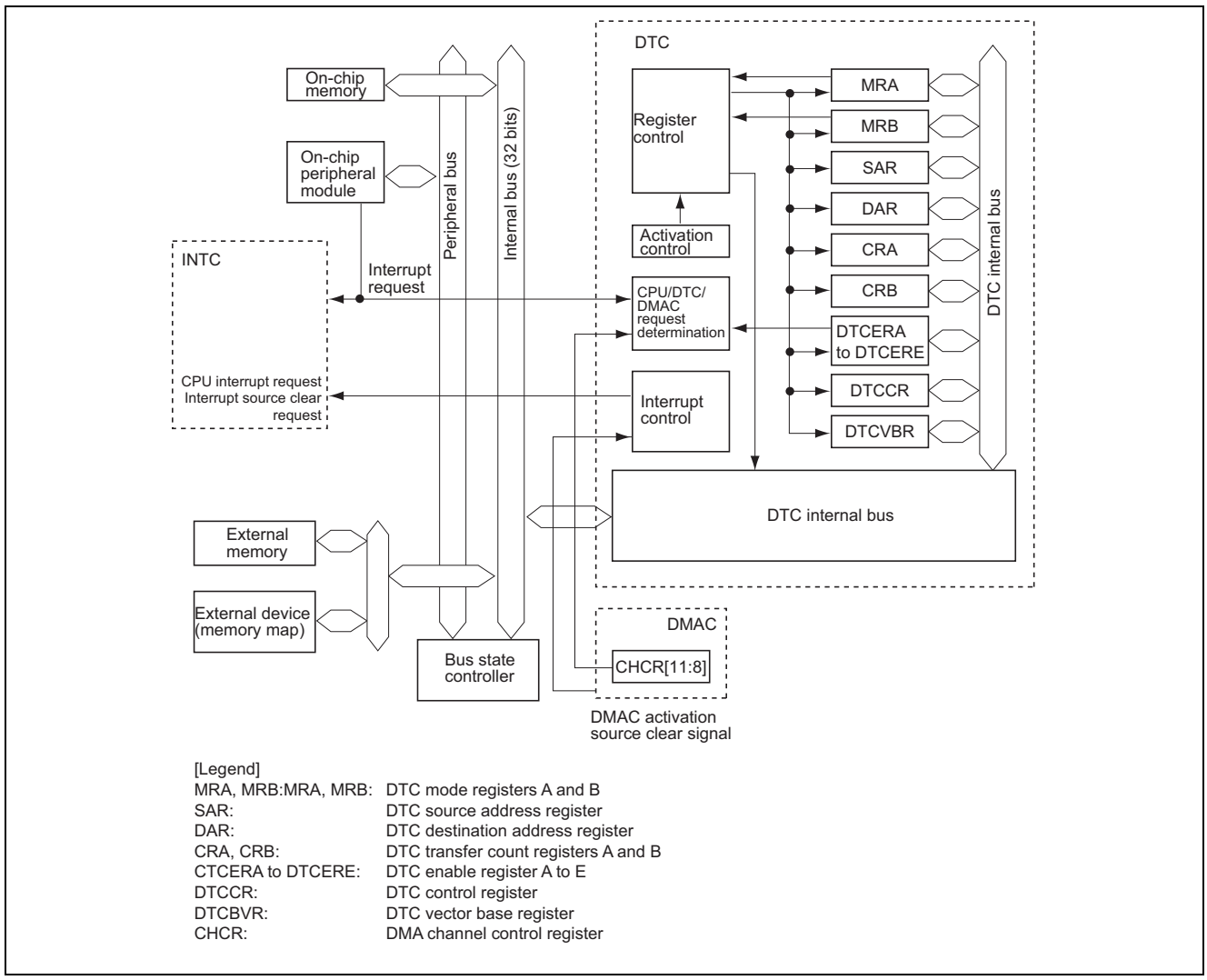


Figure 3 Block Diagram of DTC

- DTCC Mode register A (MRA)
  MRA selects DTC operating mode. MRA cannot be accessed directly by the CPU.

- DTC Mode register B (MRB)
  MRB selects DTC operating mode. MRB cannot be accessed directly by the CPU.

- DTC Source Address Register (SAR)
  SAR is a 32-bit register that designates the source address of data to be transferred by the DTC. SAR cannot be accessed directly from the CPU.

- DTC Destination Address Register (DAR)
  DAR is a 32-bit register that designates the destination address of data to be transferred by the DTC. DAR cannot be accessed directly from the CPU.

- DTC Transfer Count Register A (CRA)
  CRA is a 16-bit register that designates the number of times data are to be transferred by the DTC. CRA cannot be accessed directly from the CPU.

- DTC Transfer Count Register B (CRB)
  CRB is a 16-bit register that designates the number of times data are to be transferred by the DTC in block transfer mode. This register is not used in normal transfer mode and repeat transfer mode, and cannot be accessed directly from the CPU.

- DTC Enable Registers A to E (DTCERA to DTCERE)
  DTCER that is comprised of eight registers, DTCERA to DTCERE, is a register that specifies DTC activation interrupt sources. For the correspondence between interrupt sources and DTCE bits, refer to the hardware manual.

- DTC Control Register (DTCCR)
  DTCCR specifies transfer information read skip.

- DTC Vector Base Register (DTCVBR)
  DTCVBR is a 32-bit register that specifies the base address for vector table address calculation.

- DMA Channel Control Registers (CHCR)
  CHCR is a control register for the direct memory access controller (DMAC). This register is a 32-bit readable/writable register that controls the DMA transfer mode.

4. Principles of Operation

In this sample application, the SCIF is used for clock-synchronous transmission and reception to simultaneously transmit and receive 32-byte blocks of data. The data transfer function of the DTC module is used to transfer data for transmission and received data to and from the SCIF. A transmit FIFO data empty interrupt request from the SCIF activates the DTC to transfer data from the serial transmit FIFO register to the on-chip RAM. Also, a receive FIFO data full interrupt request from the SCIF activates the DTC to transfer data from the on-chip RAM to the serial transmit FIFO register.

The settings for the SCIF communication and DTC transfer in this sample application are listed in tables 4 and 5. In addition, the timing of operations in this sample application is shown in figure 4.

Table 4 Settings for SCIF

Item	Setting
Communications mode	Clock synchronous
Transfer rate	100,000 bps
Length of data	8 bits
Bit order	LSB first (fixed)
Synchronous clock	Synchronous clock is output from the SCK pin
FIFO data triggers	• Transmission: 8 • Reception: 1
Interrupt	• Transmit FIFO data empty (TXIF): activates the DTC for transmission • Receive FIFO data full (RXFI): activates the DTC for reception • Receive error interrupt (BRIF)
Channel	Channel 3

Table 5 Settings for DTC

Item	Settings for SCIF Transmission (DTC_TX)	Settings for SCIF Reception (DTC_RX)
Transfer mode	Normal mode	Normal mode
Number of unit transfers	32	32
Transfer size	Byte transfer	Byte transfer
Transfer source	On-chip RAM: Tx_data[32]	SCIF channel 0 Receive FIFO data register
Transfer destination	SCIF channel 0 Transmit FIFO data register	On-chip RAM: Rx_data[32]
Transfer source address	Address incremented	Transfer source address (transfer source fixed)
Transfer destination address	Transfer destination address (transfer destination fixed)	Address incremented
Activation source	SCIF transmit FIFO data empty interrupt (TXIF interrupt)	SCIF receive data full interrupt (RXIF interrupt)
Interrupt processing	After specified data have been transferred, generation of a CPU interrupt by the DTC activation source is enabled.	After specified data have been transferred, generation of a CPU interrupt by the DTC activation source is enabled.

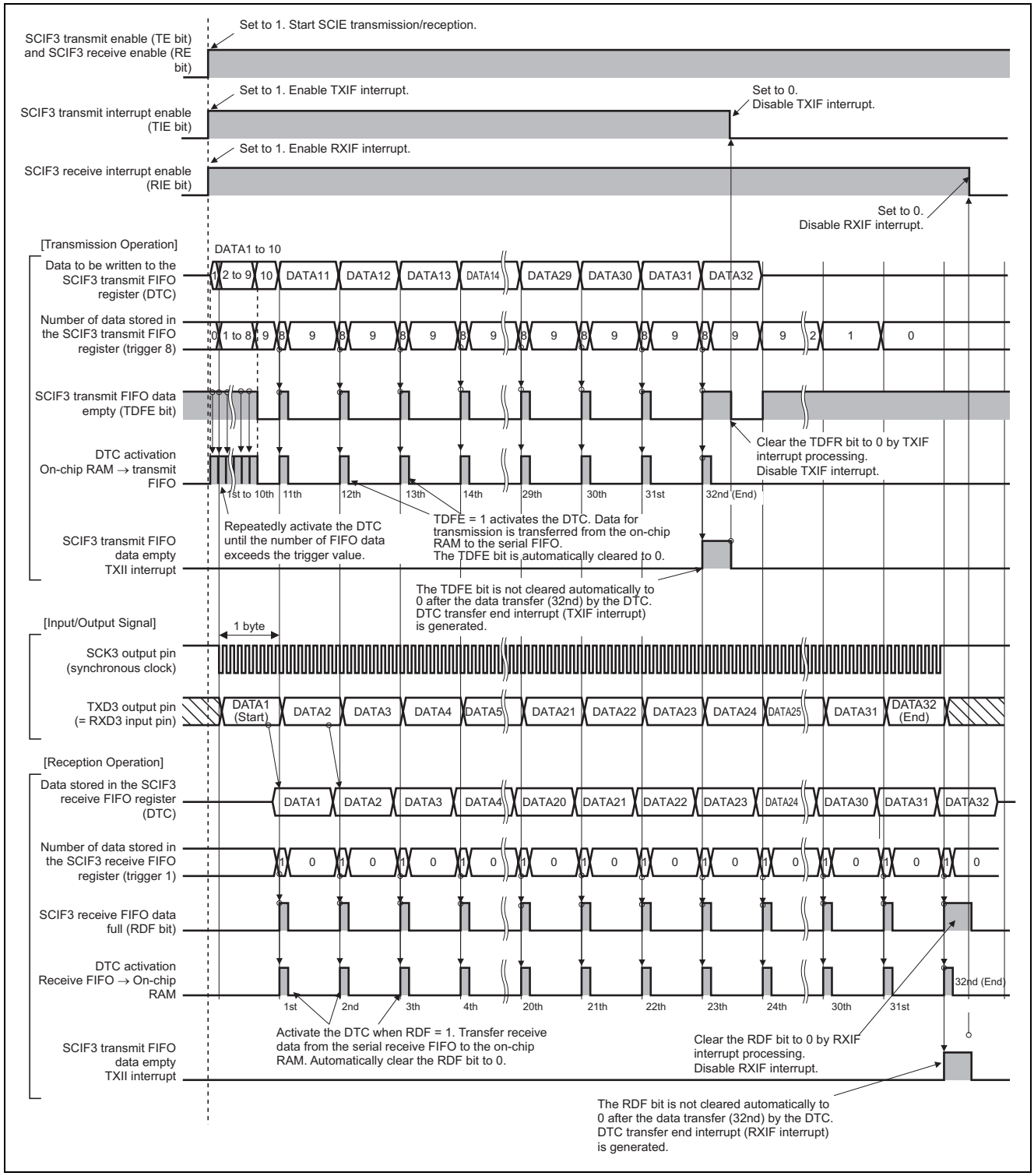


Figure 4 Simultaneous Transmission/Reception of Serial Data by Using the Data Transfer Function of the DTC

5. Description of Software

5.1 List of Functions

The functions used in this sample application are listed below.

Table 6 List of Functions

Function Name	Description
void main(void)	Main Routine • Initializes the DTC • Initializes the serial communication interface (SCIF) and enables the transmission and reception of serial data
void init_dtc(void)	DTC Initialization Routine Specifies the settings for DTC transfer. This function is called from the main() function
void init_io_scif(void)	SCIF Initialization Routine Specifies the settings for SCIF communication. This function is called from the main() function
void int_scif_rxif_end(void)	DTC Transfer End Interrupt Routine for Serial Reception The interrupt source is a SCIF receive data full interrupt (RXIF). This function is executed at the end of DTC transfer to receive serial data.
void int_scif_txif_end(void)	DTC transfer End Interrupt Routine for Serial Transmission The interrupt source is a SCIF transmit data empty interrupt (TXIF). This function is executed after a DTC transfer for transmitting serial data.
void int_scif_brif(void)	SCIF Receive Error Interrupt Routine Interrupt (BRIF) processing in case of an SCIF overrun error

5.2 Variables Used

The variables used in this sample application are listed below.

Table 7 List of Variables

Variable and Label Name	Description	Referenced in
unsigned char Tx_data[32]	Array that holds data for serial transmission	main()
unsigned char Rx_data[32]	Array that holds received serial data	main()
struct st_dtc_info DTC_RXIF	Structure variable that holds DTC transfer information for SCIF reception	init_dtc()
struct st_dtc_info DTC_TXIF	Structure variable that holds DTC transfer information for SCIF transmission	init_dtc()
void *vec_scif_rxif	Pointer variable that holds the first address of the DTC_RXIF structure variable, i.e. of the DTC transfer information. This variable is used to set the DTC vector table.	main()
void *vec_scif_txif	Pointer variable that holds the first address of the DTC_TXIF structure variable, i.e. of the DTC transfer information. This variable is used to set the DTC vector table.	main()

5.3 Section Settings

Allocation of the program sections in this sample application is shown below.

Table 8 Section Settings

Address	Section Name	Description
H'00000000	DVECTTBL	Reset vector table
	DINTTBL	Interrupt vector table
	PIntPRG	Interrupt function program
H'00000800	PResetPRG	Power-on reset program
H'00001000	P	Program area
	C$DSEC	Holds the address for initializing the D section
	C$BSEC	Holds the address for initializing the B section
	D	Holds the initial values of the corresponding variables
H'FFFF4000	B	Holds the valuables that do not have initial values
	R	Holds the valuables that have initial values
H'FFFFB794	DDTC_VECT_SCIF_RXIF	DTC vector address for SCIF reception Holds the address where the DTC transfer information is allocated
H'FFFFB79C	DDTC_VECT_SCIF_TXIF	DTC vector address for SCIF transmission Holds the address where the DTC transfer information is allocated
H'FFFFBC00	S	Stack area

5.4 Register Settings

This section describes the register settings used for this sample application. Note that the settings listed are those required for this sample application, not the initial values.

5.4.1 Settings for Clock Pulse Generator (CPG)

1. Frequency Control Register (FRQCR)
   Specifies the division ratio of the operation frequency to the output frequency of PLL circuit.

   Setting: H' 0249

Bit	Bit Name	Setting	Description
15	—	0	Reserved
14 to 12	IFC2 to IFC0	000	Internal Clock (Iϕ) Frequency Division Ratio 000: × 1, so Iϕ = 80 MHz for 10-MHz input clock.
11 to 9	BFC2 to BFC0	001	Bus Clock (Bϕ) Frequency Division Ratio 001: × 1/2, so MHz for 10-MHz input clock.
8 to 6	PFC2 to PFC0	001	Peripheral Clock (Pϕ) Frequency Division Ratio 001: × 1/2, so Pϕ = 40 MHz for 10-MHz input clock.
5 to 3	MIFC2 to MIFC0	001	MTU2S Clock (MIϕ) Frequency Division Ratio 001: × 1/2, so MIϕ = 40 MHz for 10-MHz input clock.
2 to 0	MPFC2 to MPFC0	001	MTU2 Clock (MPϕ) Frequency Division Ratio 001: × 1/2, so MPϕ = 40 MHz for 10-MHz input clock.

5.4.2 Settings for Power-Down Mode

1. Standby Control Register 2 (STBCR2)
   Controls the operation of modules in a power-down mode.

   Setting: H'28

Bit	Bit Name	Setting	Description
7	MSTP7	0	Module Stop Bit 7 Specifies whether the clock signal is supplied to RAM 0: Clock signal is supplied (RAM operates)
6	MSTP6	0	Module Stop Bit 6 Specifies whether the clock signal is supplied to ROM 0: Clock signal is supplied (ROM operates)
5	—	1	Reserved
4	MSTP4	0	Module Stop Bit 4 Specifies whether the clock signal is supplied to DTC 0: Clock signal is supplied (DTC operates)
3	MSTP3	1	Module Stop Bit 3 Specifies whether the clock signal is supplied to DMAC 1: Clock signal supplied to DMAC is halted
2 to 0	—	000	Reserved

2. Standby Control Register 3 (STBCR3)
   Controls the operation of modules in a power-down mode.

   Setting: H'BF

Bit	Bit Name	Setting	Description
7	MSTP15	1	Module Stop Bit 15 Specifies whether the clock signal is supplied to I2C2 1: Clock signal supplied to I2C2 is halted
6	MSTP14	0	Module Stop Bit 14 Specifies whether the clock signal is supplied to SCIF 0: Clock signal is supplied (SCIF operates)
5	MSTP13	1	Module Stop Bit 13 Specifies whether the clock signal is supplied to SCI_2 1: Clock signal supplied to SCI_2 is halted
4	MSTP12	1	Module Stop Bit 12 Specifies whether the clock signal is supplied to SCI_1 1: Clock signal supplied to SCI_1 is halted
3	MSTP11	1	Module Stop Bit 11 Specifies whether the clock signal is supplied to SCI_0 1: Clock signal supplied to SCI_0 is halted
2	MSTP10	1	Module Stop Bit 10 Specifies whether the clock signal is supplied to SSU 1: Clock signal supplied to SSU is halted
1, 0	—	11	Reserved

5.4.3 Settings for Data Transfer Controller (DTC)

1. DTC Control Register (DTCCR)
   Specifies transfer information read skip.

   Setting: H'10

Bit	Bit Name	Setting	Description
7 to 5	—	000	Reserved
4	RSS	1	0: Transfer read skip is not performed 1: Transfer read skip is performed when the vector numbers match.
3	RCHNE	0	0: Disables the chained transfer after repeat transfer
2, 1	—	00	Reserved
0	ERR	0	Transfer Stop Flag 0: No interrupt occurs

2. Register (MRA, MRB, SAR, DAR, CRA, and CRB) settings for DTC transfer for SCIF transmission (values from the DTC_TXIF variables)

- DTC Mode Register A (MRA)
  Selects a DTC operating mode (transfer information for SCIF transmission).
  Setting: H'08

Bit	Bit Name	Setting	Description
7, 6	MD1 and MD0	00	00: Normal transfer mode
5, 4	SZ1 and MD0	00	00: Byte-size transfer
3, 2	SM1 and MD0	10	10: SAT is incremented after a transfer
1, 0	—	00	Reserved

- DTC Mode Register B (MRB)
  Selects a DTC operating mode (transfer information for SCIF transmission).
  Setting: H'00

Bit	Bit Name	Setting	Description
7	CHNE	0	0: Disables chained transfer
6	CHNS	0	0: Chained transfer every time Since chained transfer is disabled, this setting has no effect.
5	DISEL	0	DTC Interrupt Select 0: A CPU interrupt request is generated only when the specified number of data transfers end
4	DTS	0	0: Specifies the destination as repeat or block area Since chained transfer is disabled, this setting has no effect.
3, 2	DM1 and DM0	00	0x: DAR is fixed
1, 2	—	00	Reserved

- DTC Source Address Register (SAR)
  SAR is a 32-bit register that designates the source address of data to be transferred by the DTC. This register specifies the address in RAM where the data for SCIF transmission is stored.
  Setting: the first address of the array variable Tx_data[]

- DTC Destination Address Register (DAR)
  DAR is a 32-bit register that designates the destination address of data to be transferred by the DTC. This register specifies the address of the transmission register for the SCIF.
  Setting: the address of transmit FIFO data register (SCFTDR)

- DTC Transfer Count Register A (CRA)
  CRA is a 16-bit register that designates the number of times data are to be transferred by the DTC.
  Setting: 0x20

- DTC Transfer Count Register B (CRB)
  CRB is a 16-bit register that designates the number of times data are to be transferred by the DTC in block transfer mode. Since the block transfer mode is not in use, the setting of this register has no effect.
  Setting: 0

3. Settings for Transfer Information DTC_RXIF Variable (MRA, MRB, SAR, DAR, CRA and CRB) for SCIF Reception

- DTC Mode Register A (MRA)
  Selects a DTC operating mode (transfer information for SCIF transmission).
  Setting: H'00

Bit	Bit Name	Setting	Description
7, 6	MD1 and MD0	00	00: Normal transfer mode
5, 4	SZ1 and MD0	00	00: Byte-size transfer
3, 2	SM1 and MD0	00	0x: SAR is fixed
1, 0	—	00	Reserved

- DTC Mode Register B (MRB)
  Selects a DTC operating mode (transfer information for SCIF transmission).
  Setting: H'08

Bit	Bit Name	Setting	Description
7	CHNE	0	0: Disables chained transfer
6	CHNS	0	0: Chained transfer every time Since chained transfer is disabled, this setting has no effect.
5	DISEL	0	DTC Interrupt Select 0: A CPU interrupt request is generated only when the specified number of data transfers end
4	DTS	0	0: Specifies the destination as repeat or block area Since chained transfer is disabled, this setting has no effect.
3, 2	MD1 and MD0	10	10: DAR is incremented after a transfer
1, 2	—	00	Reserved

- DTC Source Address Register (SAR)
  SAR is a 32-bit register that designates the source address of data to be transferred by the DTC. This register specifies the address of the register for SCIF reception.
  Setting: the address of the receive FIFO data register (SCFRDR)

- DTC Destination Address Register (DAR)
  DAR is a 32-bit register that designates the destination address of data to be transferred by the DTC. This register specifies the address in RAM where the data for SCIF reception is stored.
  Setting: the first address of the array variable Rx_data[]

- DTC Transfer Count Register A (CRA)
  CRA is a 16-bit register that designates the number of times data are to be transferred by the DTC.
  Setting: 0x20

- DTC Transfer Count Register B (CRB)
  CRB is a 16-bit register that designates the number of times data are to be transferred by the DTC in block transfer mode. Since the block transfer mode is not in use, the setting of this register has no effect.
  Setting: 0

4. DTC Vector Base Register (DTCVBR)
   DTCVBR is a 32-bit register that specifies the base address for vector table address calculation. This register is set to an address in the on-chip RAM.

   Setting: 0xFFFFB000

5. DTC Enable Register E (DTCERE)
   Specifies DTC activation interrupt sources.

   Setting: H'0300

Bit	Bit Name	Setting	Description
15	DTCE15	0	0: No corresponding interrupt source
14	DTCE14	0	0: No corresponding interrupt source
13	DTCE13	0	0: No corresponding interrupt source
12	DTCE12	0	0: No corresponding interrupt source
11	DTCE11	0	0: No corresponding interrupt source
10	DTCE10	0	0: No corresponding interrupt source
9	DTCE9	1	RXIF (receive data full interrupt) from the SCIF activates the DTC
8	DTCE8	1	TXIF (transmit FIFO data empty interrupt) from the SCIF activates the DTC
7	DTCE7	0	0: No corresponding interrupt source
6	DTCE6	0	0: No corresponding interrupt source
5	DTCE5	0	0: No corresponding interrupt source
4	DTCE4	0	0: No corresponding interrupt source
3	DTCE3	0	0: No corresponding interrupt source
2	DTCE2	0	0: No corresponding interrupt source
1	DTCE1	0	0: No corresponding interrupt source
0	DTCE0	0	0: No corresponding interrupt source

5.4.4 Settings for Serial Communication Interface with FIFO (SCIF)

1. Serial Control Register (SCSCR)

   Operates the SCIF transmission/reception, enables or disables interrupt requests, and selects the transmission/reception clock source.

   Setting: H'00F0

Bit	Bit Name	Setting	Description
15 to 8	—	00000000	Reserved
7	TIE	1	1: Transmit-FIFO-data-empty interrupt request (TXIF) is enabled
6	RIE	1	1: Receive-data-full interrupt (RXIF), receive-error interrupt (ERIF), and break interrupt (BRIF) requests are enabled
5	TE	1	0: Transmitter disabled 1: Transmission enabled
4	RE	1	0: Reception disabled 1: Reception enabled
3	REIE	0	0: Receive error interrupt (ERIF) request and break interrupt (BRIF) request are disabled. Note that the setting of this bit is valid only when the RIE bit is 0.
2	—	0	Reserved
1, 0	CKE1 and CKE0	00	Clock Synchronous Mode Internal clock, SCK pin used for synchronous clock output

2. FIFO Control Register (SCFCR)
   Resets the number of data in the transmit/receive FIFO registers, and sets the trigger data number.

   Setting: H'0000

Bit	Bit Name	Setting	Description
15 to 11	—	00000	Reserved
10 to 8	RSTRG2 to RSTRG0	000	000: $\overline{\text{RTS}}$ output active trigger These bits are valid only when modem control signals are enabled in asynchronous mode.
7, 6	RTRG1 and RTRG0	00	Receive FIFO Data Trigger 00: Trigger number = 1 (clock synchronous mode)
5, 4	TTRG1 and TTRG0	00	Transmit FIFO Data Trigger 1 and 0 00: Trigger number = 8
3	MCE	0	Enables modem control signals $\overline{\text{CTS}}$ and $\overline{\text{RTS}}$. 0: Modem signals disabled
2	TFRST	0	0: Reset operation of transmit FIFO data register disabled 1: Reset operation of transmit FIFO data register enabled
1	RFRST	0	0: Reset operation of receive FIFO data register disabled 1: Reset operation of receive FIFO data register enabled
0	LOOP	0	Internally connects the transmit output pin (TXD) and This bit receives input pin (RXD) while internally connecting the $\overline{\text{RTS}}$ and $\overline{\text{CTS}}$ pins, and enables loop-back testing. 0: Loop back test disabled

3. Serial Status Register (SCFSR)
   The upper 8 bits indicate the number of receive errors in the SCFRDR data, and the lower 8 bits indicate the status flag indicating SCIF operating state.

   Setting: H'0000

Bit	Bit Name	Setting	Description
15 to 12	PER3 to PER0	0000	Number of Parity Errors
11 to 8	FER3 to FER0	0000	Number of Framing Errors
7	ER	0	Receive Error 0: Receiving is in progress or has ended normally
6	TEND	0	Transmit End 0: Transmission is in progress (1: End of transmission)
5	TDFE	0	Transmit FIFO Data Empty 0: The number of data fro transmission written to SCFTDR is greater than the specified transmission trigger number 1: The number of data for transmission written to SCFTDR is less than or equal to the specified transmission trigger number
4	BRK	0	Break Detection 0: No break signal received
3	FER	0	Framing Error 0: No framing error
2	PER	0	0: No parity error
1	RDF	0	Receive FIFO Data Full 0: The number of data for transmission written to SCFRDR is less than the specified receive trigger number 1: The number of received data in SCFRDR is more than or equal to the specified receive trigger number
0	DR	0	Receive Data Ready 0: Receiving is in progress, or no received data remains in SCFRDR after receiving ended normally. Note that in clock synchronous mode, this bit is not set to 1.

4. Line Status Register (SCLSR)
   SCLSR is a 16-bit readable/writable register that can always be read from and written to by the CPU.

   Setting: H'0000

Bit	Bit Name	Setting	Description
15 to 1	—	0..0	Reserved
0	ORER	0	Overrun Error 0: Receiving is in progress or has ended normally 1: An overrun error has occurred A 1 cannot be written to the ORER flag. This flag can be cleared to 0 only if it has first been read from (after being set to 1).

5. Serial Mode Register (SCSMR)
   Specifies the communication format and selects the clock source for the baud rate generator.

   Setting: H' 0080

Bit	Bit Name	Setting	Description
15 to 8	—	0..0	Reserved
7	C/$\overline{A}$	1	1: Clock synchronous mode
6	CHR	0	0: 8-bit data In the clock synchronous mode, the data length is always eight bits, regardless of the CHR setting.
5	PE	0	0: Parity bit not added or checked In clock synchronous mode, a parity bit is neither added nor checked, regardless of the PE setting.
4	O/$\overline{E}$	0	Parity mode 0: Since PE is 0, the setting of this bit is ignored.
3	STOP	0	Stop Bit Length 0: One stop bit Since stop bits are not added in clock synchronous mode, the setting of this bit is ignored.
2	—	0	Reserved
1, 0	CKS1 and CKS0	00	Select the internal clock source of the on-chip baud rate generator 00: Pϕ

6. Bit Rate Register (SCBRR)
   This is an 8-bit register that, together with the baud rate generator clock source selected by the CKS1 and CKS0 bits in the serial mode register (SCSMR), determines the serial transmit/receive bit rate.

   Setting: SCBRR = 63 (H'40)

   The setting of this register is as follows:

- Clock synchronous mode: bit rate = 100,000 [bps]
- Specify the internal clock source for the on-chip baud rate generator as Pϕ (set the CKS[1:0] bits in SCSMR to B'00)
- Pϕ = 40 MHz

For details on the bit rate register (SCBRR), refer to the hardware manual.

5.4.5 Settings for I/O Port

1. Port E Data Register L (PEDRL)

   Stores port E data. When a value is written to PEDRL while the pin function is general output (port), the value is output directory from the pin. The value of port output pin PE6 (SCK3) is set to 1.

   Setting: H' 0040

Bit	Bit Name	Setting	Description
15	PE15DR	0	Output value for port-pin PE15
14	PE14DR	0	Output value for port-pin PE14
13	PE13DR	0	Output value for port-pin PE13
12	PE12DR	0	Output value for port-pin PE12
11	PE11DR	0	Output value for port-pin PE11
10	PE10DR	0	Output value for port-pin PE10
9	PE9DR	0	Output value for port-pin PE9
8	PE8DR	0	Output value for port-pin PE8
7	PE7DR	0	Output value for port-pin PE7
6	PE6DR	1	Output value for port-pin PE6
5	PE5DR	0	Output value for port-pin PE5
4	PE4DR	0	Output value for port-pin PE4
3	PE3DR	0	Output value for port-pin PE3
2	PE2DR	0	Output value for port-pin PE2
1	PE1DR	0	Output value for port-pin PE1
0	PE0DR	0	Output value for port-pin PE0

5.4.6 Settings for Pin Function Controller (PFC)

1. Port E Control Register L2 (PECRL2)
   Specifies the function of the multiplex pin on the port E. Sets the SCK3, TXD3, and RXD3 pins of the SCIF.

   Setting: H' 0222

Bit	Bit Name	Setting	Description
15	—	0	Reserved
14 to 12	PE7MD2 to PE7MD0	000	000: PE7 I/O (port)
11	—	0	Reserved
10 to 8	PE6MD2 to PE6MD0	010	000: PE6 is set as the I/O pin for SCK3 (SCIF clock)
7	—	0	Reserved
6 to 4	PE5MD2 to PE5MD0	010	010: PE5 is set as the output pin for TXD3 (SCIF clock)
3	—	0	Reserved
2 to 0	PE4MD2 to PE4MD0	010	000: PE4 is set as the input pin for RXD3 (SCIF clock)

2. Port E I/O Registers L (PEIORL)
   Sets the pins on port E as inputs or outputs. Sets the SCK3, TXD3, and RXD3 pins of the SCIF.

   Setting: H' 0060

Bit	Bit Name	Setting	Description
15	PE15IOR	0	0: PE15 input
14	PE14IOR	0	0: PE14 input
13	PE13IOR	0	0: PE13 input
12	PE12IOR	0	0: PE12 input
11	PE11IOR	0	0: PE11 input
10	PE10IOR	0	0: PE10 input
9	PE9IOR	0	0: PE9 input
8	PE8IOR	0	0: PE8 input
7	PE7IOR	0	0: PE7 input
6	PE6IOR	1	0: PE6 output (SCK3 output)
5	PE5IOR	1	1: PE5 output (TXD3 output)
4	PE4IOR	0	0: PE4 input (RXD3 input)
3	PE3IOR	0	0: PE3 input
2	PE2IOR	0	0: PE2 input
1	PE1IOR	0	0: PE1 input
0	PE0IOR	0	0: PE0 input

5.4.7 Settings for Interrupt Controller (INTC)

1. Interrupt Priority Register L (IPRL)
   Sets priority levels for corresponding interrupt requests.

   Setting: H' 000F

Bit	Bit Name	Setting	Description
15 to 12	IPR15 to IPR12	0000	Priority level 0
11 to 8	IPR11 to IPR8	0000	Priority level 0
7 to 4	IPR7 to IPR4	0000	Priority level 0
3 to 0	IPR3 to IPR0	1111	Priority level 15 for SCIF (ERIF, RXIF, BRIF, and TXIF) interrupts

6. Flowcharts

6.1 Main Function

The flowchart of the main function is shown in figure 5.

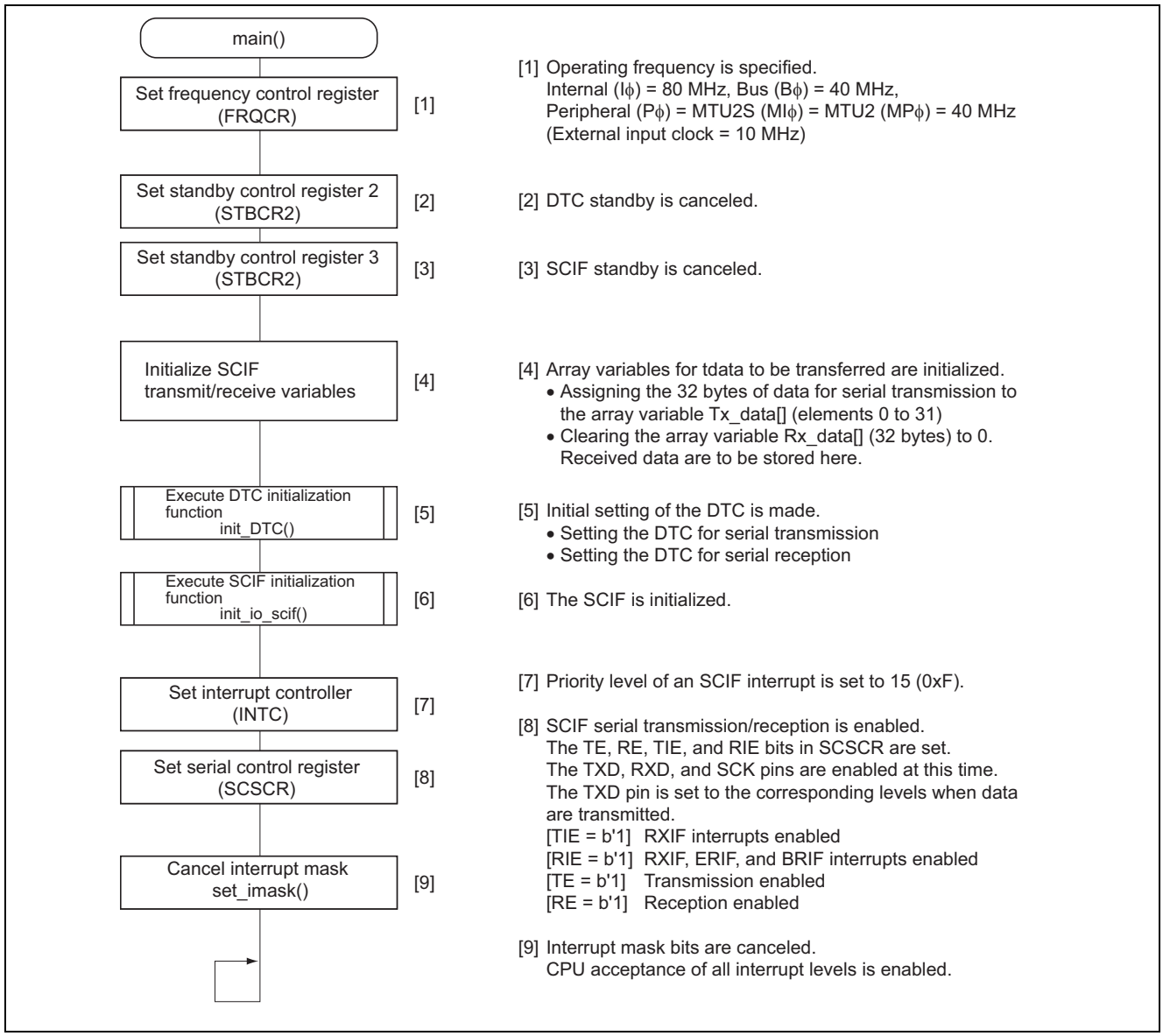
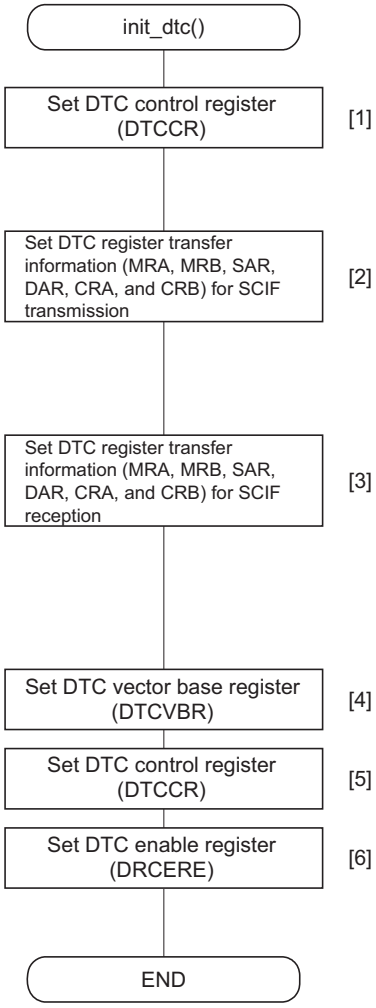


Figure 5 Processing of Main Function

6.2 DTC Initialization

The flowchart of initializing the DTC is shown in figure 6.



[1] The DTC is initialized.
Skipping of DTC transfer-control information reading is disabled.
[RRS = b'0] Read skip not performed

[2] DTC registers for SCIF transmission are set.
- [MRA] Normal mode, byte-size transfer, SAR incremented after each transfer
- [MRB] Chained transfer disabled, interrupts enabled after a data transfer, DAR fixed after each transfer
- [SAR] The SAR indicates the RAM area where data for transmission are stored (Tx_data[]) as the DTC transfer source
- [DAR] The DAR indicates the SCIF transmit register SCFTDR as the DTC transfer destination
- [CAR] Number of unit transfers: 32

[3] DTC registers for SCIF reception are set.
- [MAR] Normal mode, byte-size transfer, SAR fixed after each transfer
- [MRB] Chained transfer disabled, interrupts enabled after a data transfer, DAR incremented after each transfer
- [SAR] The transfer source indicates the SCIF receive register SCRFDR
- [DAR] The transfer source indicates the RAM area where received data are stored (Rx_data[]) as the DTC transfer source
- [CAR] Number of unit transfers: 32

[4] The base address for vector table address calculation by the DTC is set to 0xFFFFB000 within the on-chip RAM

[5] Skipping of DTC transfer-control information reading is is enabled.
[RRS = b'1] Read skip performed

[6] Settings for DTC activation are made.
[DTCERE9 = b'1] DTC activation due to SCIF RXIF interrupts enabled
[DTCERE8 = b'1] DTC activation due to SCIF TXIF interrupts enabled

Figure 6 DTC Initialization

6.3 SCIF Initialization

The flowchart of initializing the SCIF is shown in figure 7.

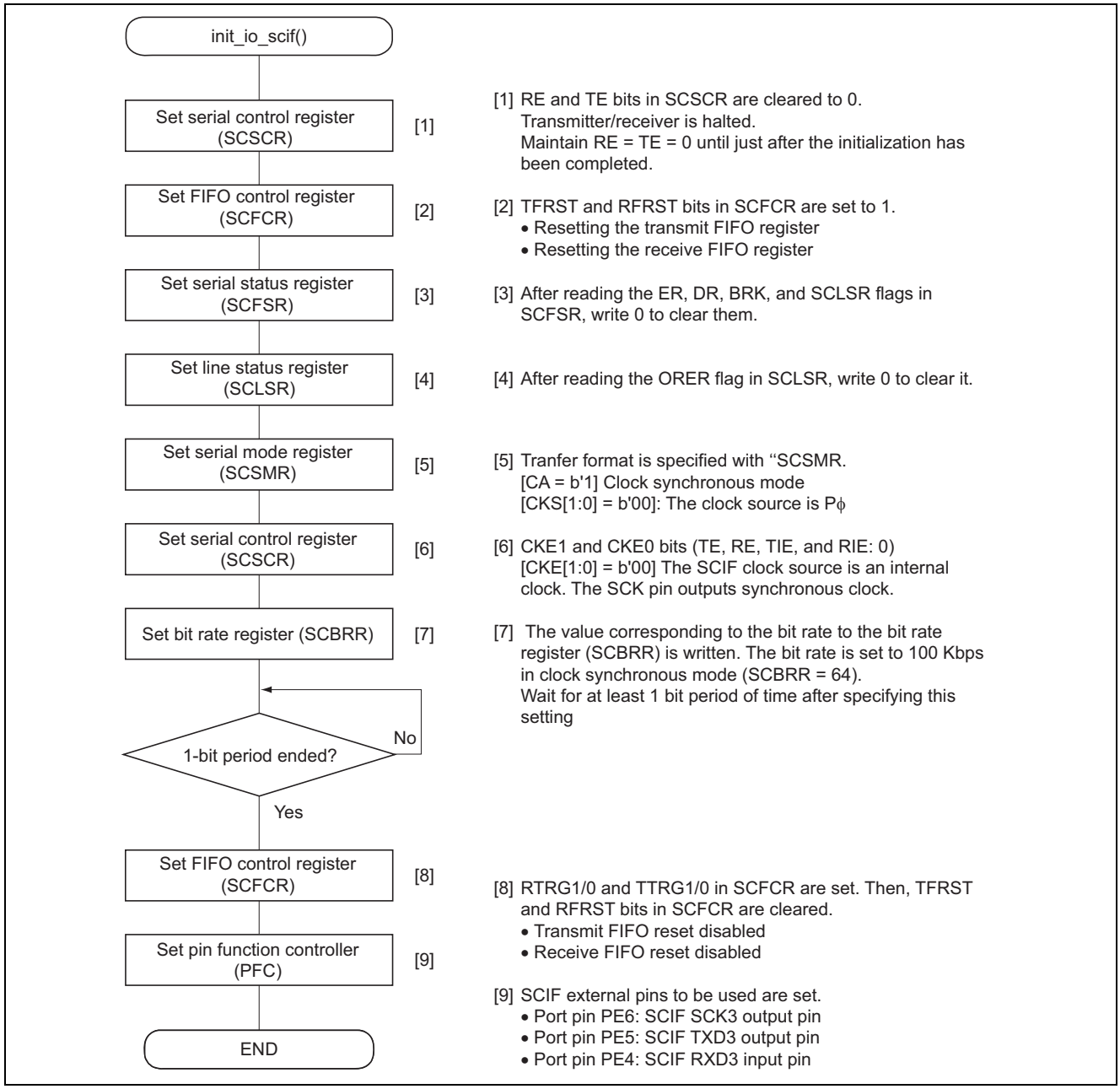


Figure 7 SCIF Initialization

6.4 Interrupt Processing

The processing of the SCIF receive interrupt (interrupt after a DTC transfer), SCIF transmit interrupt (interrupt after a DTC transfer) and SCIF error interrupt is illustrated in figure 8.

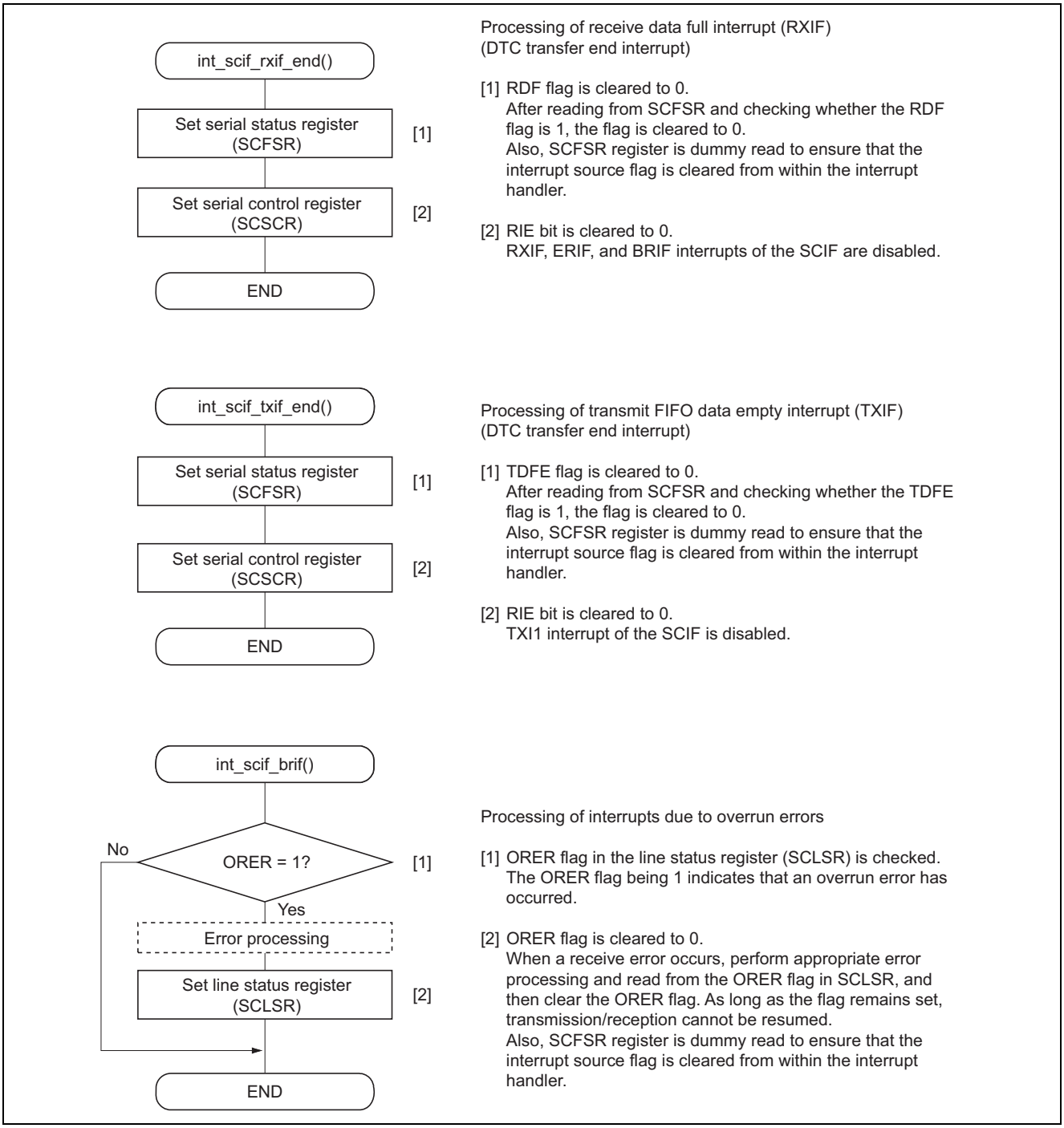


Figure 8 Interrupt Processing

7. Documents for Reference

- Software Manual
  SH-1/SH-2/SH-DSP Software Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.
- Hardware Manual
  SH7080 Series Hardware Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.

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