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SH7280 Group

Using the DTC in the Asynchronous-Mode Transfer of Serial Data by the SCIF

Introduction

This application note describes the transfer of serial data in asynchronous mode by the serial communications interface with FIFO (SCIF) with the aid of the data-transfer controller (DTC). This application note is a summary for quick reference of information required in the design of user software.

Target Device

SH7285

Contents

1. Preface

1.1 Specifications

In this sample task, serial transfer is conducted with the data-transfer controller (DTC) used to transfer data between the serial communications interface with FIFO (SCIF) and on-chip RAM.

Figure 1 shows an example of connection for transmission and reception by the SCIF in asynchronous mode.

- SCIF3 and DTC are used.
- The communications format has a fixed 8-bit data length.
- The data-transfer controller (DTC) is activated by the transmit-FIFO-data-empty-interrupt request and the receive-FIFO-data-full-interrupt request to transfer data to the desired transfer destination. In the transmitting and receiving sections of the SCIF, interrupt processing is activated by the transmit-FIFO-data-empty interrupt on the transmitting side and by the receive-FIFO-data-full-interrupt on the receiving side.
- Once 32 bytes of data have been transmitted and received, each operation is halted.

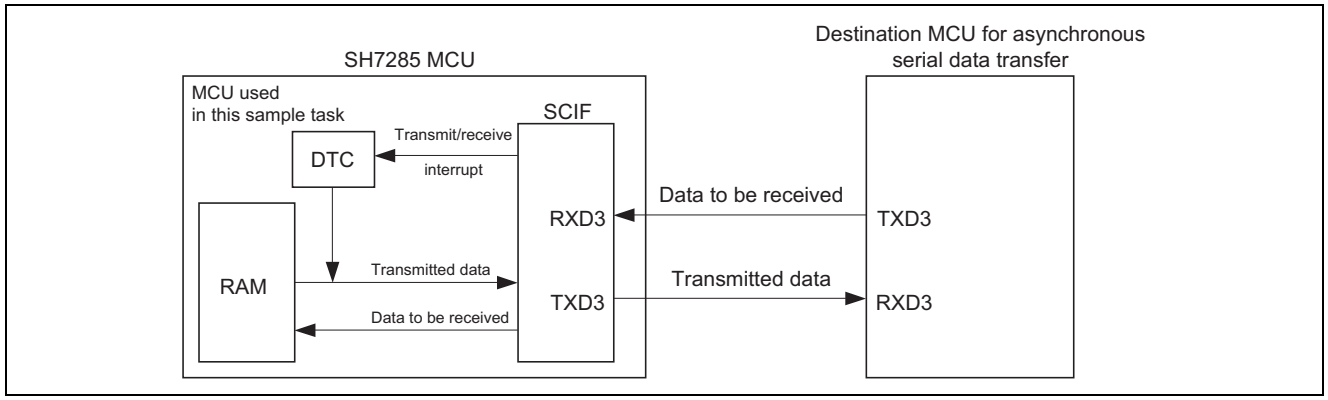


Figure 1 Example of Connection for Using the DTC in Transmission and Reception of Serial Data in Asynchronous Mode

1.2 Modules Used

- Data transfer controller (DTC)
- Serial communications interface with FIFO (SCIF3)

1.3 Applicable Conditions

MCU:	SH7285	
Operating frequency:	Internal clock	100 MHz
	Bus clock	50 MHz
	Peripheral clock	50 MHz
C compiler:	SuperH RISC engine Family C/C++ Compiler Package Ver.9.1.1	
	(from Renesas Technology Corp.)	

2. Description of the Sample Application

The transmit-FIFO-data-empty interrupt (TXI) and receive- FIFO-data-full interrupt (RXI) from the SCIF are used as DTC-activating interrupt sources in the sample program. Normal transfer mode is employed for asynchronous serial data transfer.

2.1 Operational Overview of Modules Used

2.1.1 Serial Communications Interface with FIFO (SCIF)

In asynchronous mode, each transmitted or received character begins with a start bit and ends with a stop bit. Serial communications is synchronized one character at a time. The transmitting and receiving sections of the SCIF are independent, so full duplex communications is possible. The transmitter and receiver are 16-byte FIFO buffered, so data can be written and read while transmitting and receiving are in progress, enabling continuous transmitting and receiving.
In asynchronous serial communications, the communications line is normally held in the mark (high) state. The SCIF monitors the line and starts serial communications when the line goes to the space (low) state, indicating a start bit. One serial character consists of a start bit (low), data (LSB first), parity bit (high or low), and stop bit (high), in that order.
For details on the SCIF, please refer to the section on serial communications interface in the *SH7280 Group Hardware Manual* (REJ09B0393).

Table 1 gives an overview of serial communications in asynchronous mode. Figure 2 is a block diagram of the SCIF.

Table 1 Overview of Serial Data Communications in Asynchronous Mode

Item	Description
Number of interfaces	1 (SCIF3)
Clock sources	For internal clock: Pϕ, Pϕ/4, Pϕ/16, Pϕ/64 (Pϕ: peripheral clock) For external clock: input clock on the SCK3 pin
Data format	Transfer data length: Selectable from 7 or 8 bits Order: LSB first and MSB first are selectable
Baud rate	For internal clock: from 110 bps (Pϕ = 50 MHz) For external clock: up to 781,250 bps (Pϕ = 50 MHz, external input clock of 12.5000 MHz)
Error detection	Framing, parity and overrun errors Breaks can also be detected.
Interrupt requests	Transmit-FIFO-data-empty interrupt (TXI) Receive-FIFO-data-full interrupt (RXI) Break interrupt (BRI) Receive-error interrupt (ERI)
Clock sources	Internal and external clocks are selectable • Internal clock When the internal clock has been selected, the SCIF operates using the clock from the baud-rate generator and a clock signal at 16 times the frequency of the bit rate can be output. • External clock When the external clock has been selected, input of a clock signal at 16 times the frequency of the bit rate is required, not using the on-chip baud rate generator.
Loop-back test function	Internal connection of the transmit output pin (TXD) and receive input pin (RXD) enables loop-back testing.

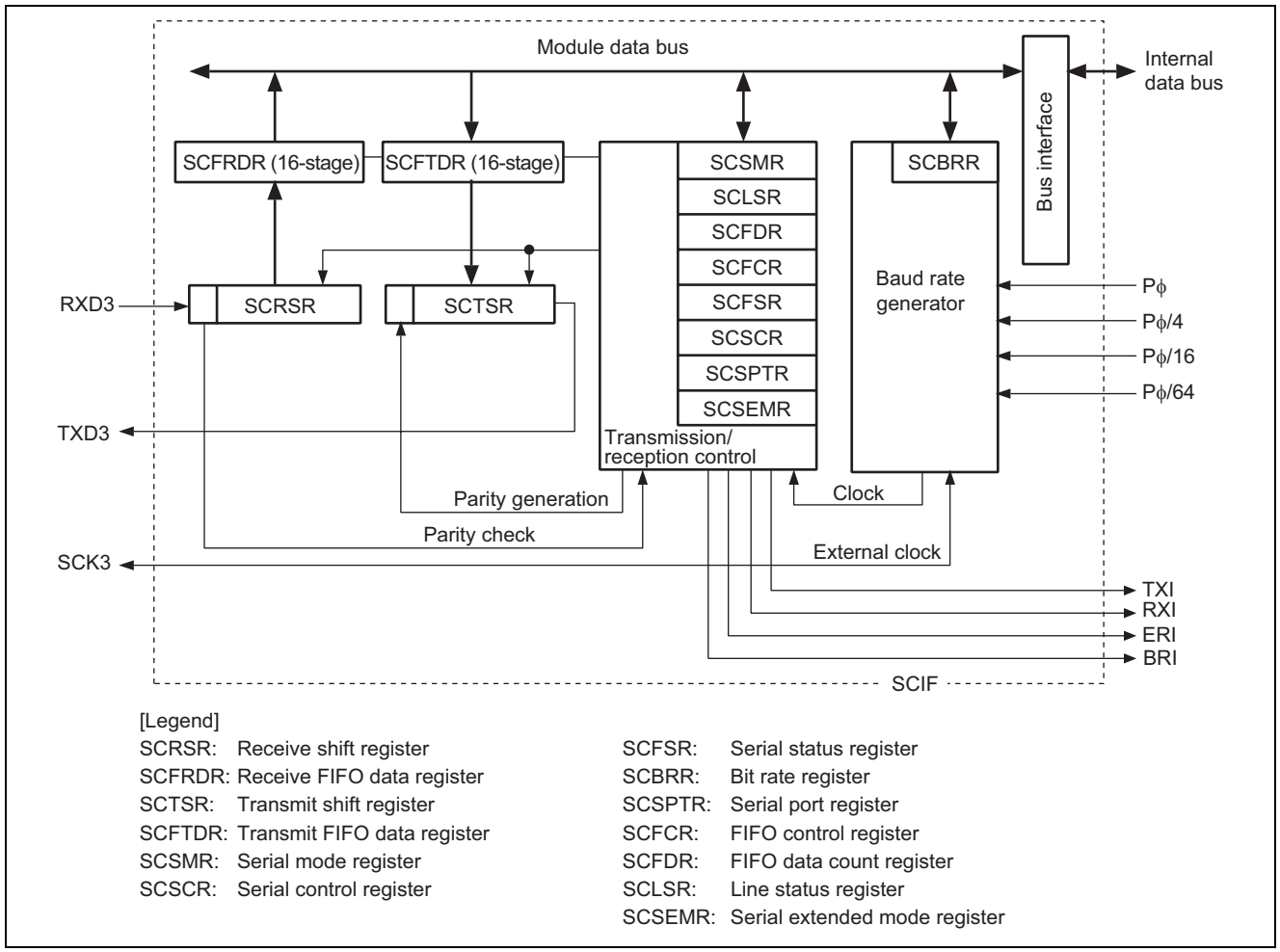


Figure 2 Block Diagram of the SCIF

2.1.2 Data-Transfer Controller (DTC)

There are three transfer modes: normal, repeat, and block transfer modes. Since transfer information is in the data area, it is possible to transfer data over any required number of channels. When activated, the DTC reads transfer information stored in the data area and transfers data according to the transfer information. After the data transfer is complete, it writes updated transfer information back to the data area.

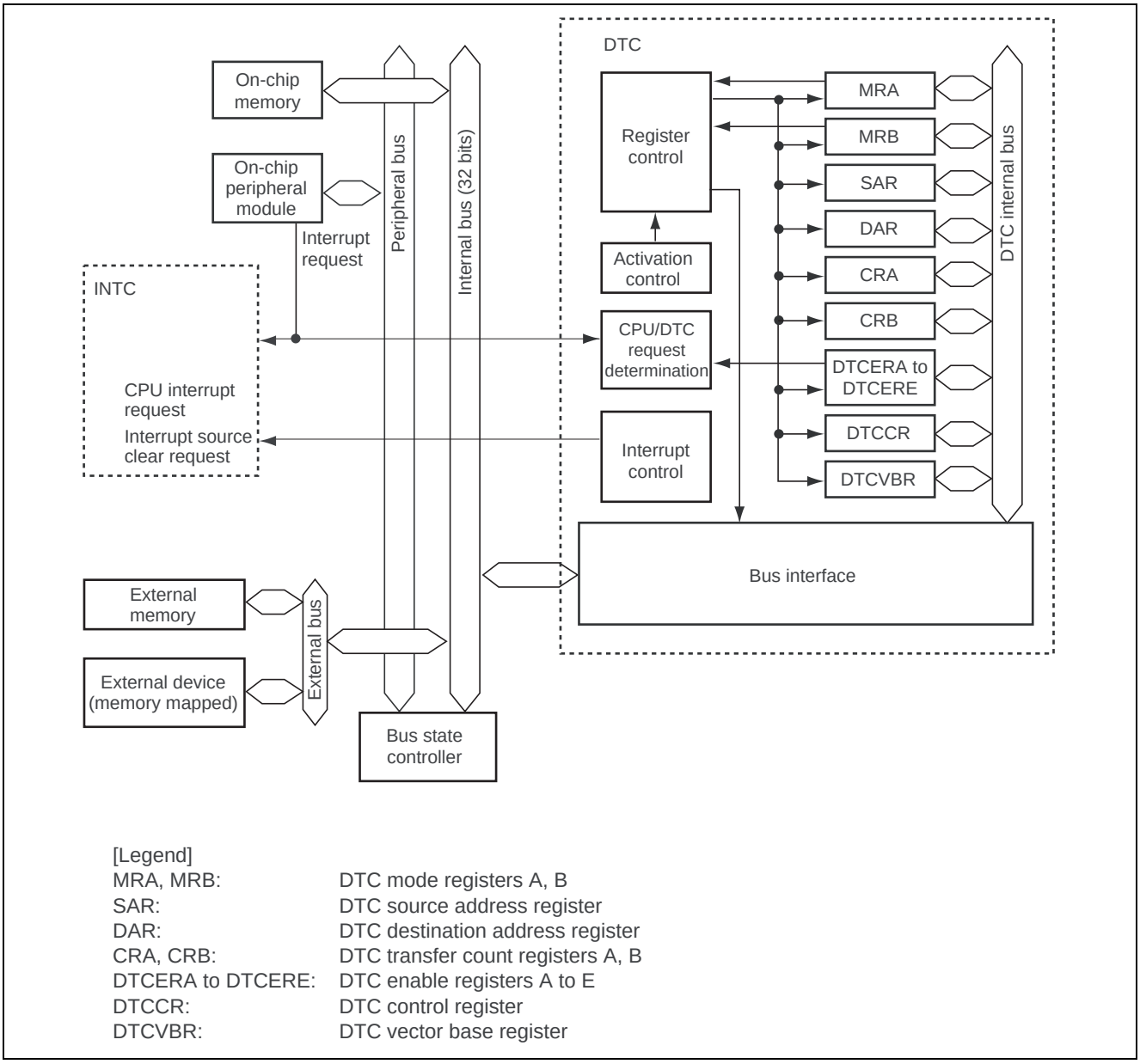
The transfer information is located in the data area. For details on the DTC, see the section on data transfer controller in the *SH7280 Group Hardware Manual* (REJ09B0393).

Table 2 gives an overview of the DTC and figure 3 is a block diagram of the DTC.

Table 2 Overview of DTC

Item	Description
Transfer modes	Normal/repeat/block transfer modes are selectable
Rounds of transfer	Normal transfer mode: 1 to 65,536 Repeat transfer mode: 1 to 256 Block transfer mode: 1 to 65,536
Data size	Size of data for data transfer can be specified as byte, word, or longword
CPU interrupt request	A CPU interrupt can be requested after completion of one data transfer A CPU interrupt can be requested after completion of the specified data transfer
Activation sources	External pins, ADC, CMT, USB, MTU2, MTU2S, IIC3, SSU, SCI, SCIF
Others	Chained transfer (multiple rounds of data transfer performed in response to a single activation source) is available A read-skip mode is specifiable for the DTC's transfer-control information Module stop mode is specifiable Short address mode is specifiable Bus release timing is selectable from three types Priority of the DTC activation can be selected from two types

Note: Note that at least either the source or destination must be an on-chip peripheral module; transfer cannot be done among an external memory, a memory-mapped external device, and an on-chip memory.



[Legend]

MRA, MRB:	DTC mode registers A, B
SAR:	DTC source address register
DAR:	DTC destination address register
CRA, CRB:	DTC transfer count registers A, B
DTCERA to DTCERE:	DTC enable registers A to E
DTCCR:	DTC control register
DTCVBR:	DTC vector base register

Figure 3 Block Diagram of the DTC

(a) Configuration of transfer information

Figure 4 shows how transfer information for the DTC is configured in the data area. Figure 5 shows the correspondence between the DTC vector table and transfer information.

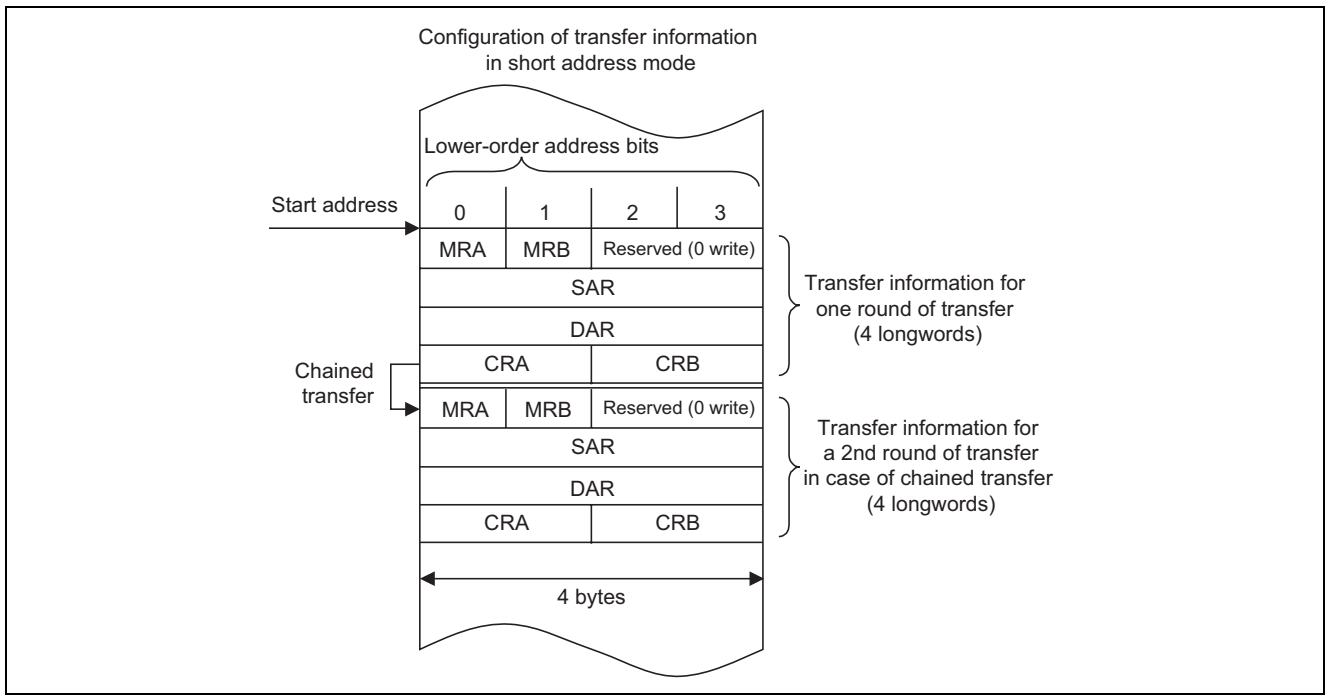


Figure 4 Transfer Information in Data Area

(b) Procedure for setting the address of the vector table for the DTC

1. The vector base address is set in the DTC vector base address register (DTCVBR) to allocate the DTC vector table in RAM.
2. Destination addresses indicated by DTC vector table address offsets are the addresses where sets of transfer-control information start.

For details on the vector table address offsets, see the section on the data transfer controller in the *SH7280 Group Hardware Manual* (REJ09B0393).

The DTC reads the start address of transfer information from the vector table according to the activation source, and then reads the transfer information from the first address.

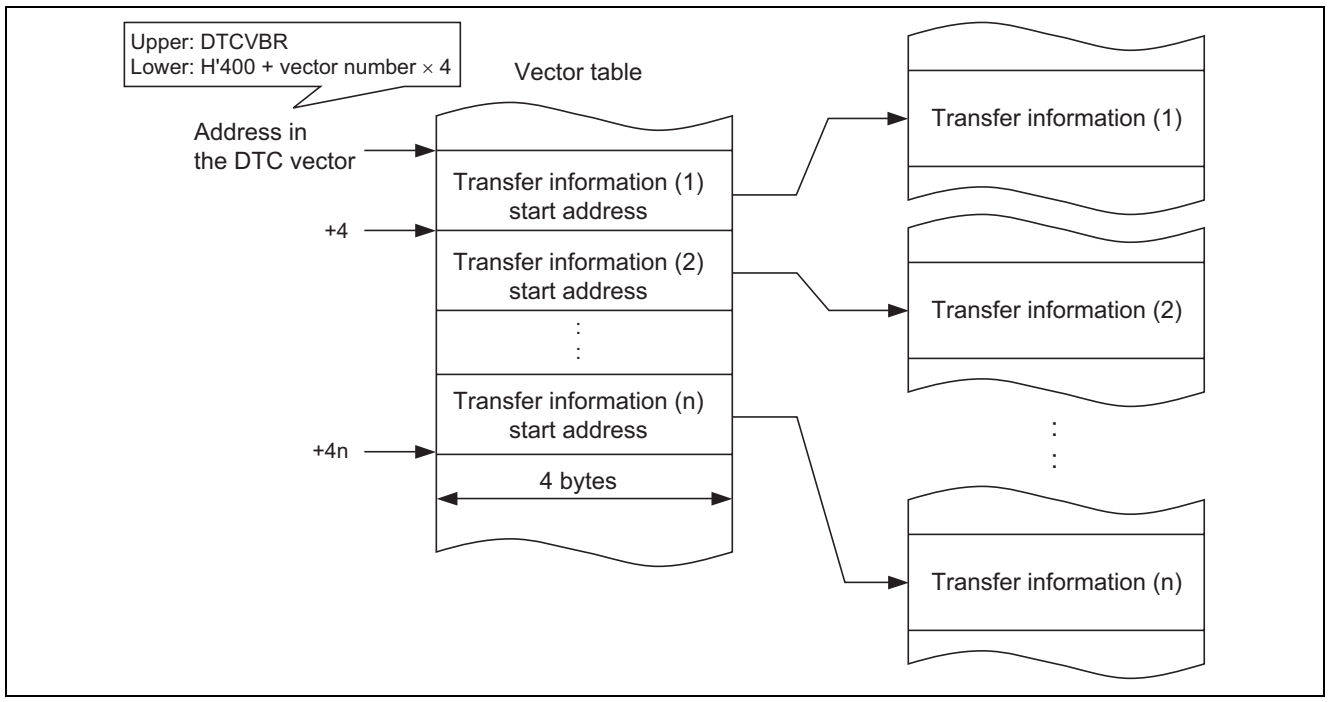


Figure 5 Correspondence between DTC Vector Addresses and Transfer Information

2.1.3 Operation of the Sample Program

Tables 3 and 4 give a list of DTC transfer conditions and an outline of settings for the communications function, respectively. Figures 6 and 7 are images of the allocation of transfer information in memory and the timing of operations, respectively.

Table 3 DTC Transfer Conditions

Item	Settings of DTC Transfer for SCIF Transmission (TXI3)	Settings of DTC Transfer for SCIF Reception (RXI3)
Transfer mode	Normal mode	Normal mode
Number of unit transfers	32	32
Transfer size	Byte transfer	Byte transfer
Transfer source	Internal RAM	Receive-FIFO-data register (SCFRDR_3)
Transfer destination	Transmit-FIFO-data register (SCFTDR_3)	Internal RAM
Transfer source address	The transfer source address is incremented after transfer.	Fixed transfer source
Transfer destination address	Fixed transfer destination	The transfer destination address is incremented after transfer.
Activation source	SCIF transmit-FIFO-data-empty interrupt	SCIF receive-FIFO-data-full interrupt
Interrupt processing	After completion of the specified data transfer, interrupts for the CPU are enabled.	After completion of the specified data transfer, interrupts for the CPU are enabled.

Table 4 Settings for Communications Function in the Sample Program

Item	Description
Module	SCIF3
Communications mode	Asynchronous mode
Interrupts	Transmit-FIFO-data-empty interrupt (TXI) Receive-FIFO-data-full interrupt (RXI) Break interrupt (BRI)
Transfer rate	38,400 bps
Number of data to be transmitted and received	32 bytes
Data length	8-bit data
Stop bit	1 stop bit
Parity	None
Bit order	LSB-first
Number of FIFO data triggers	Receive FIFO data trigger: 1 Transmit FIFO data trigger: 8

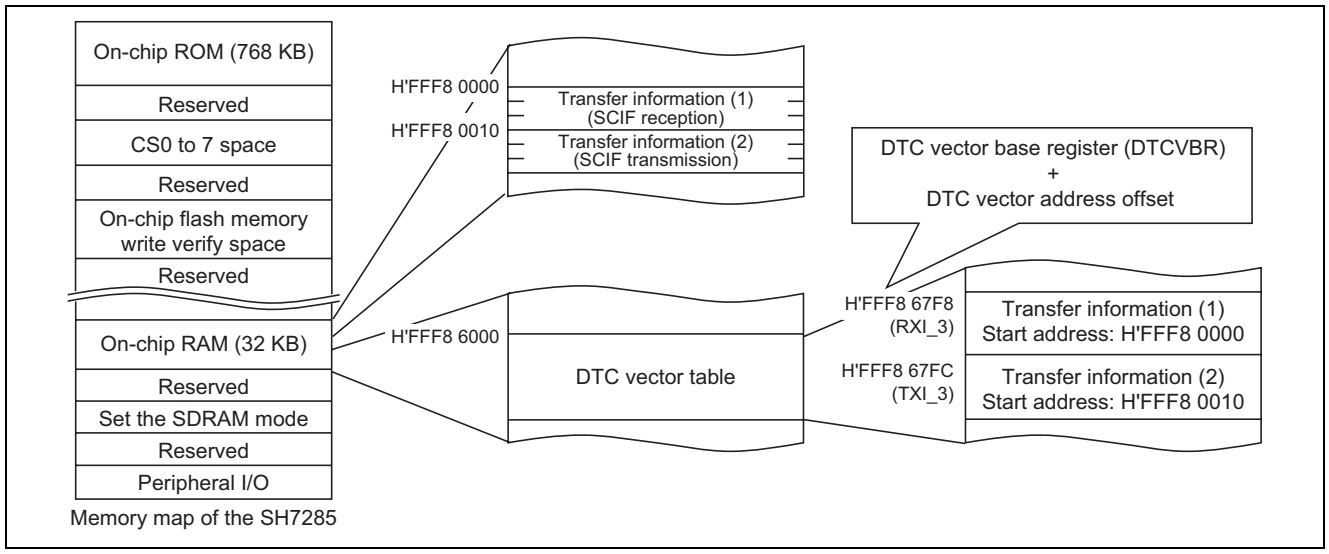


Figure 6 Image of Arrangement of Transfer Information in Memory

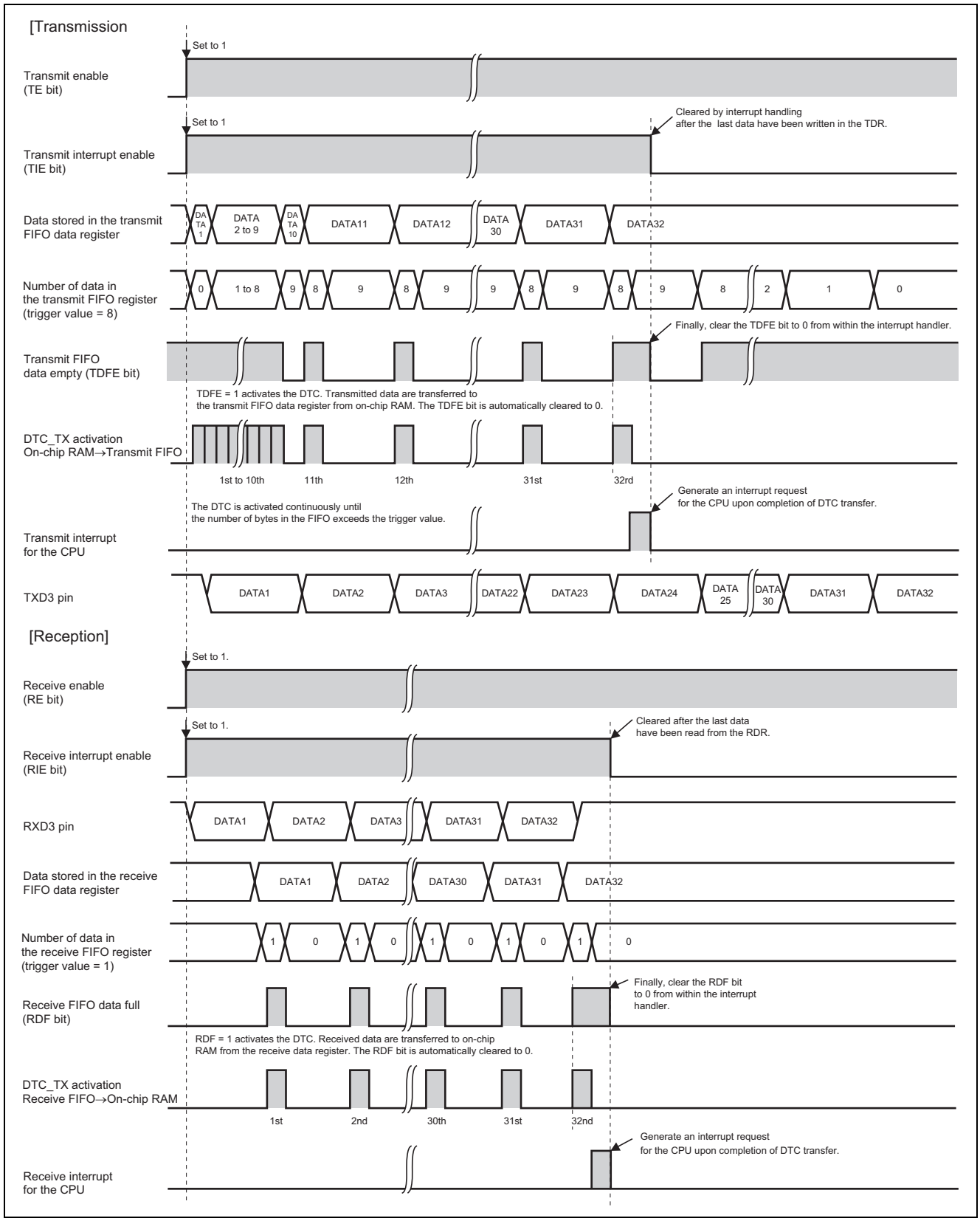


Figure 7 Principles of Operation

2.2 Procedure for Setting Modules Used

This section describes the procedure for setting up SCIF3 for asynchronous mode operations using the DTC.

Figure 8 shows the flow of processing by the sample program, figure 9 shows the flow of settings for release from module-standby mode, figure 10 shows flow 1 of DTC initialization (for transmission), figure 11 shows flow 2 of DTC initialization (fore receive operation), figure 12 shows the flow for initialization of data transmission and reception in asynchronous mode, and figure 13 shows the flow for setting up the pin function controller. Furthermore, figure 14 shows the flow for handling transmit interrupts in asynchronous mode, figure 15 shows the flow for handling receive interrupts in asynchronous mode, and figure 16 shows the flow for handling receive error interrupts. For details on the settings of individual registers, see the *SH7280 Group Hardware Manual* (REJ09B0393).

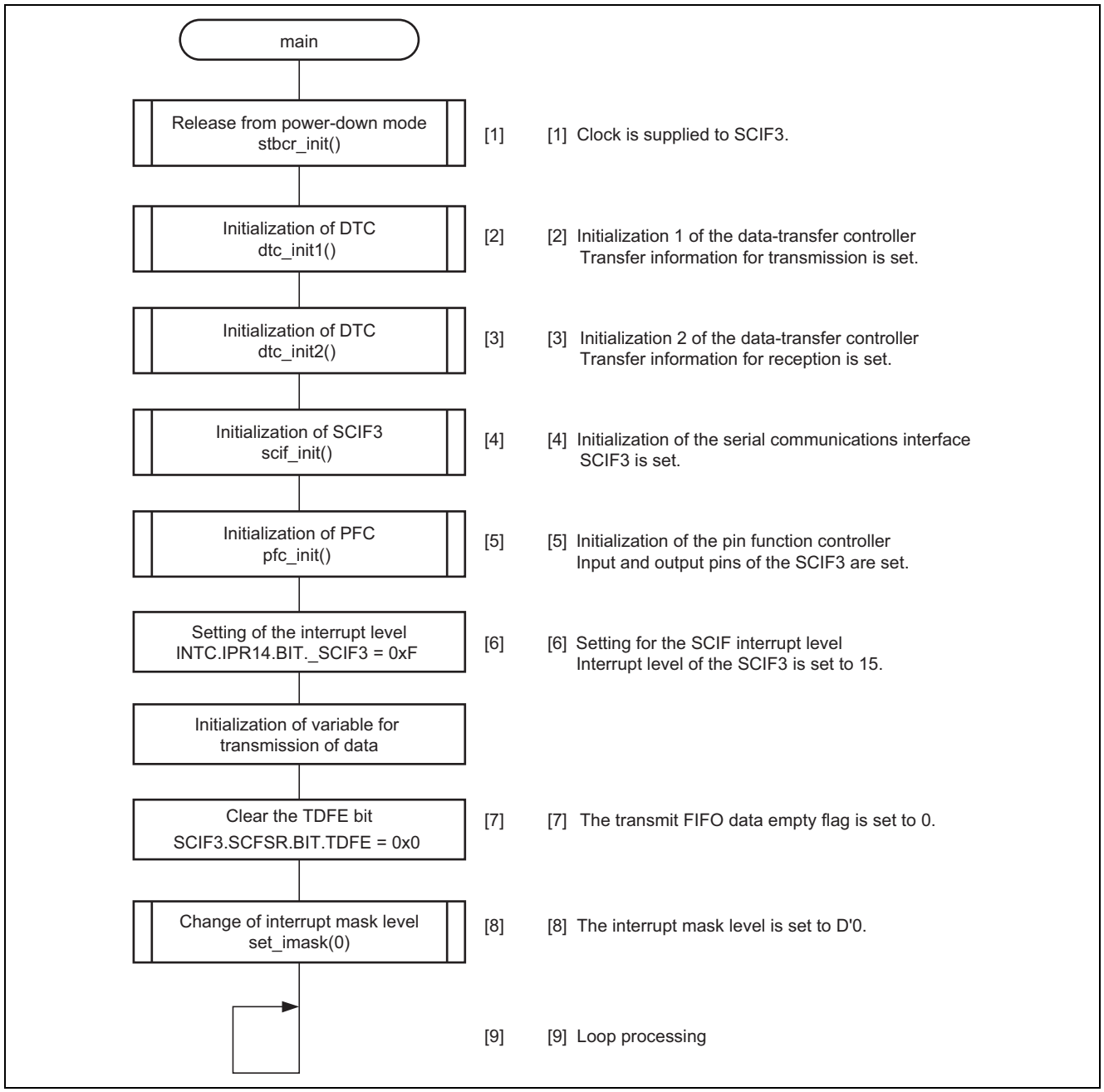


Figure 8 Flow of Processing by the Sample Program

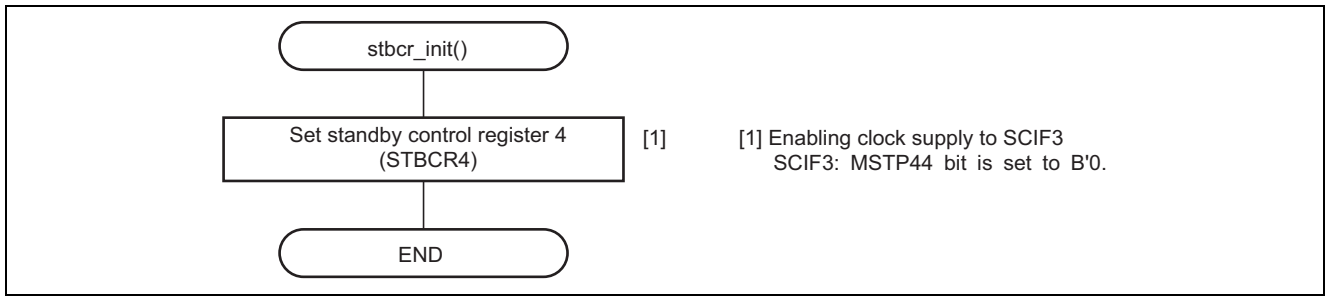


Figure 9 Flow of Setting for Release from Module-Standby Mode

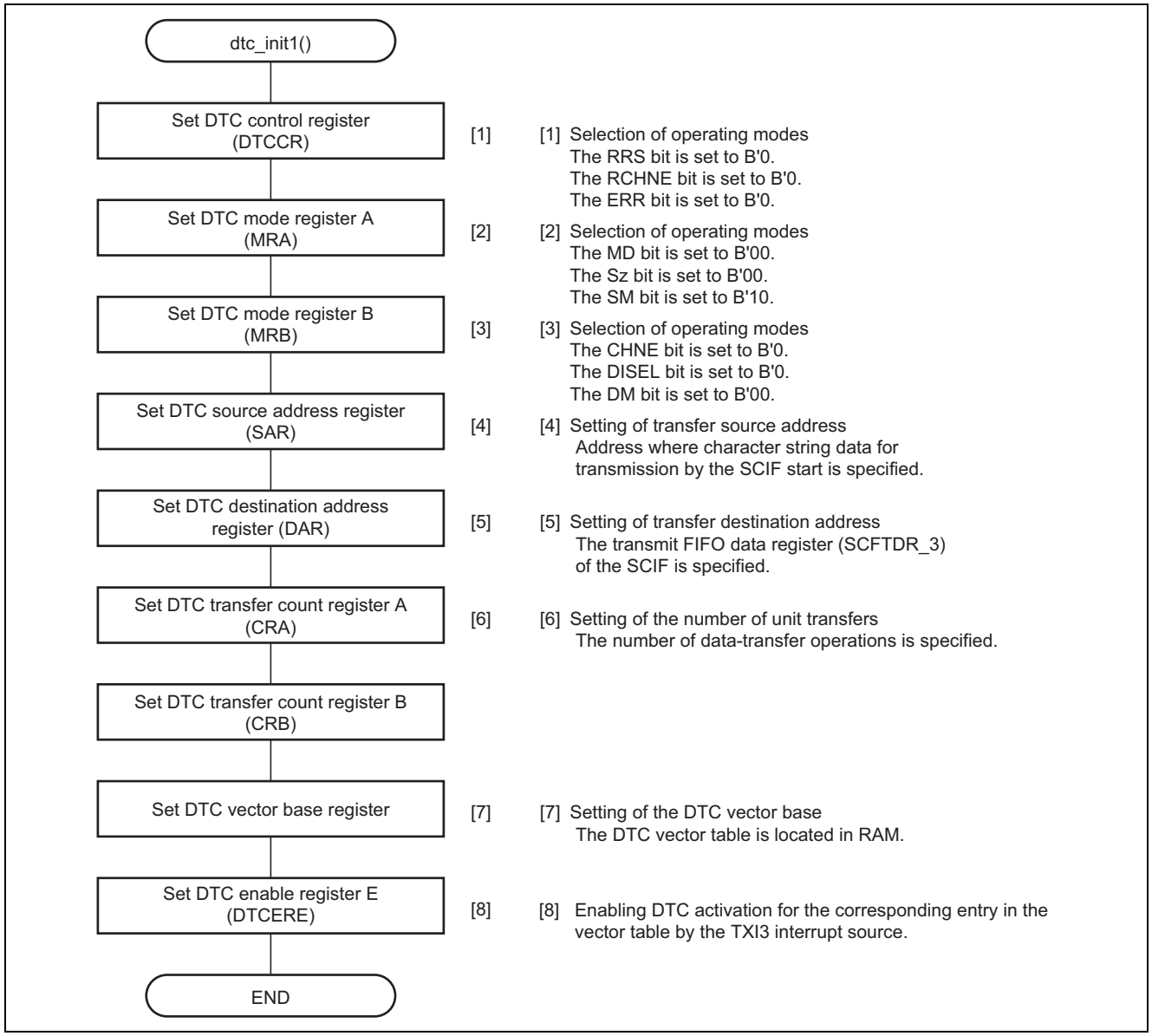


Figure 10 Flow 1 of DTC Initialization (before Transmission)

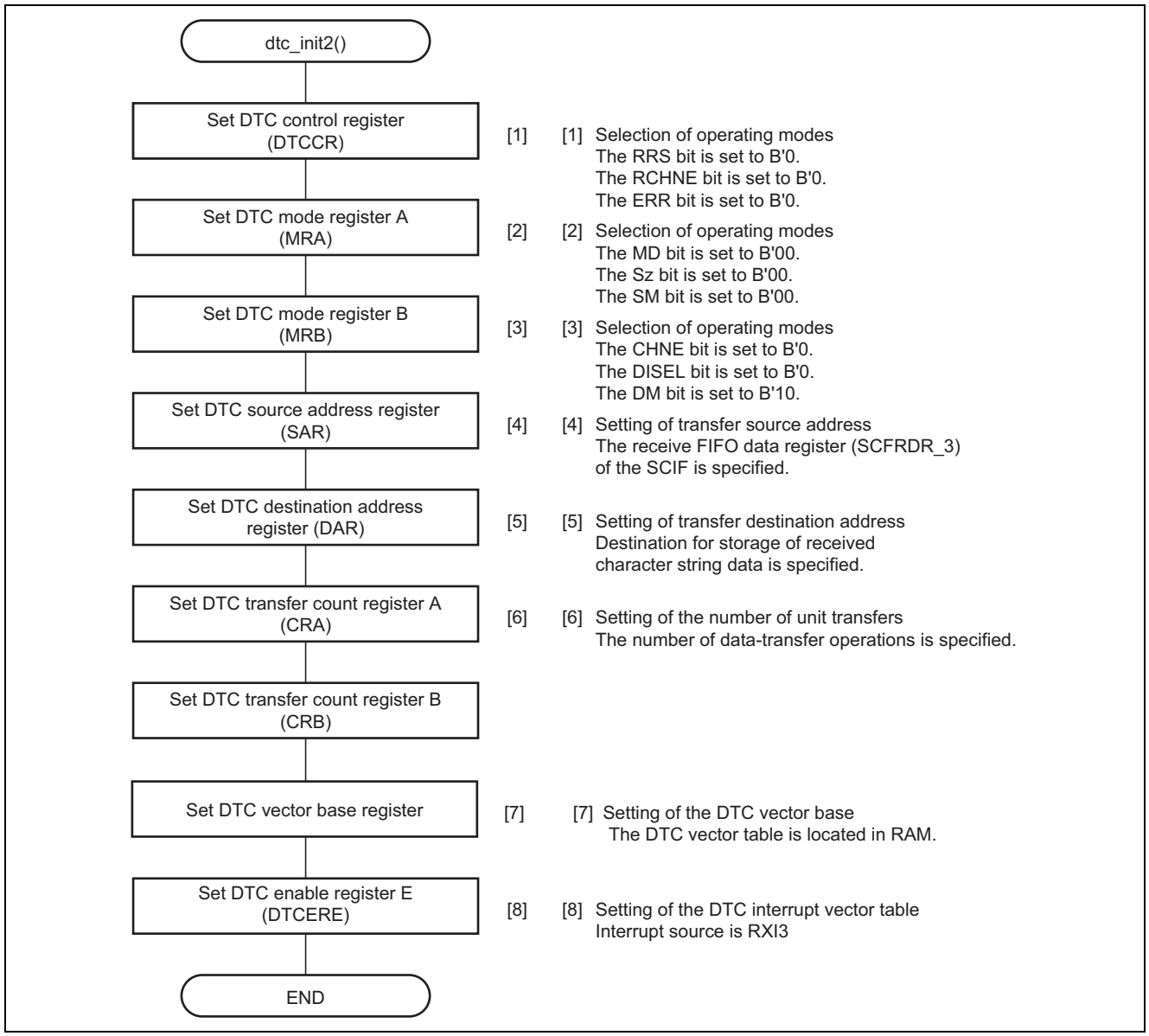


Figure 11 Flow 2 of DTC Initialization (before Receive Operation)

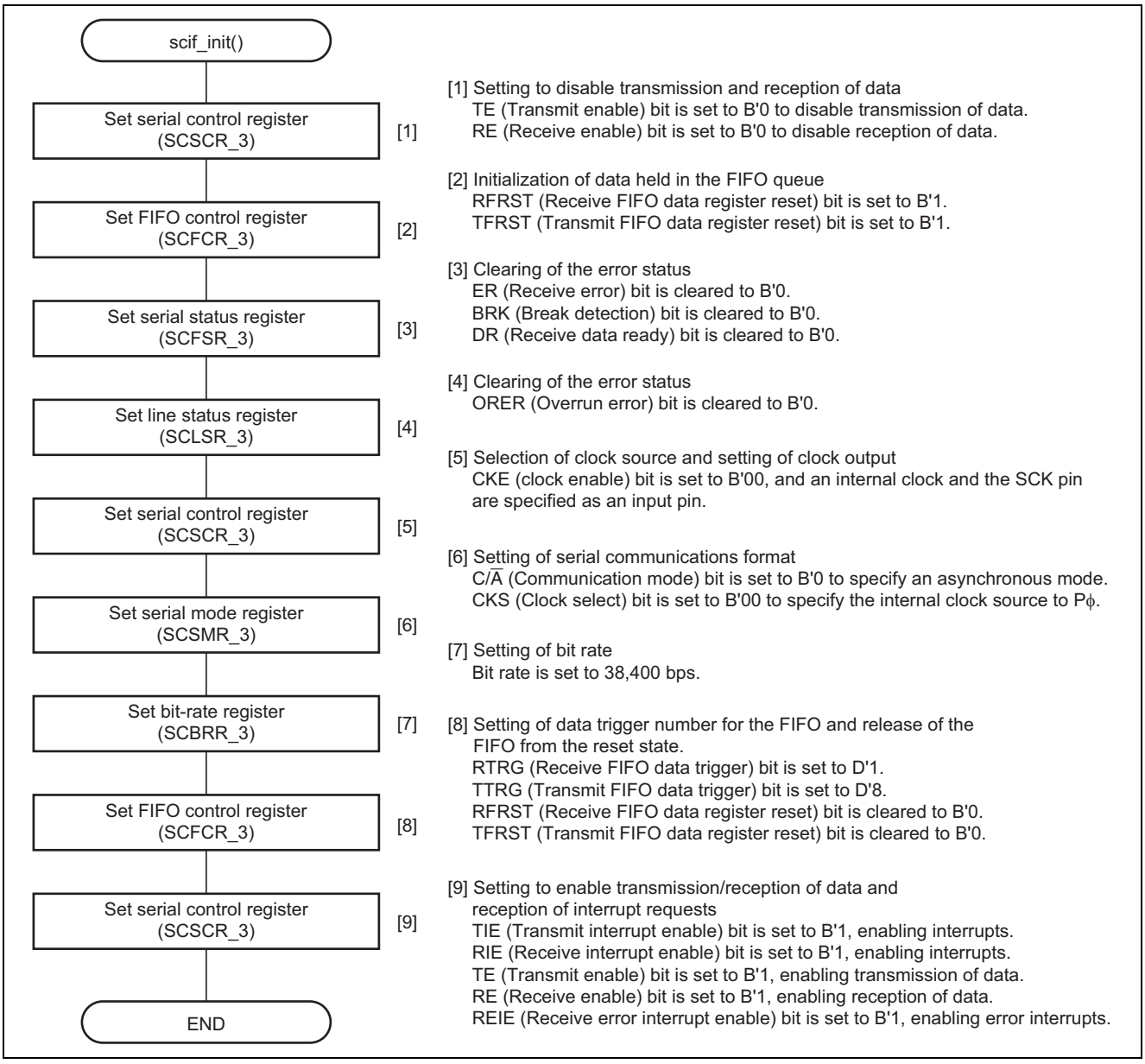


Figure 12 Flow for Initialization of Data Transmission and Reception in Asynchronous Mode

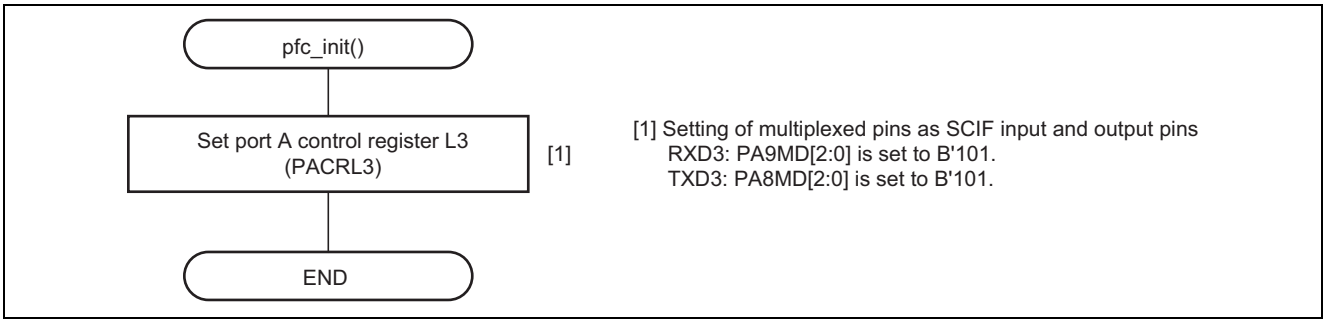


Figure 13 Flow for Setting Up the Pin Function Controller

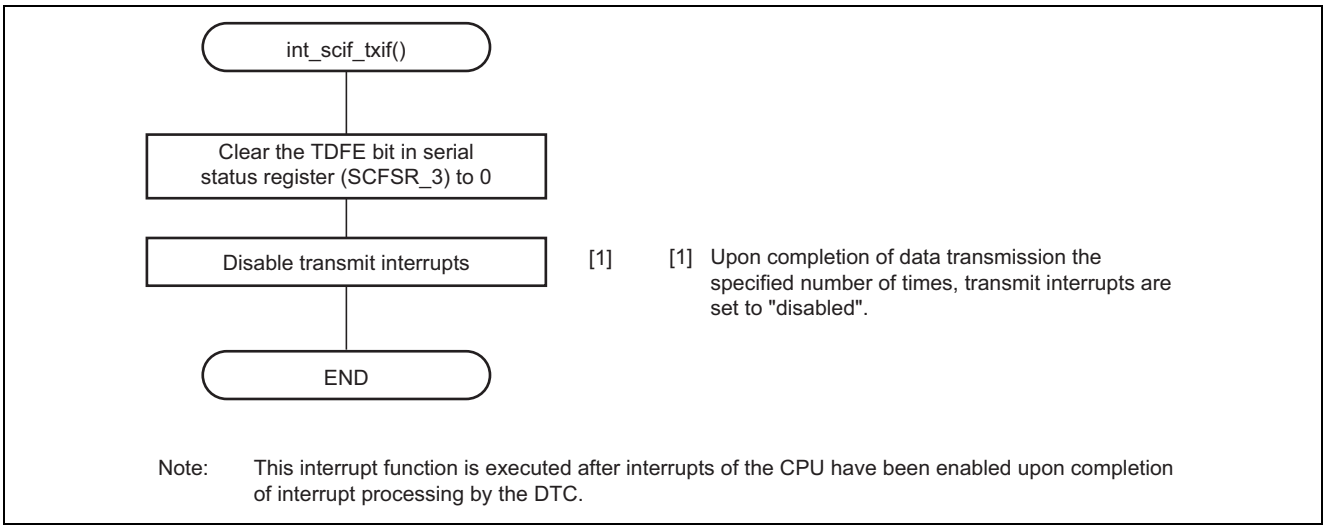


Figure 14 Flow for Handling Transmit Interrupts in Asynchronous Mode

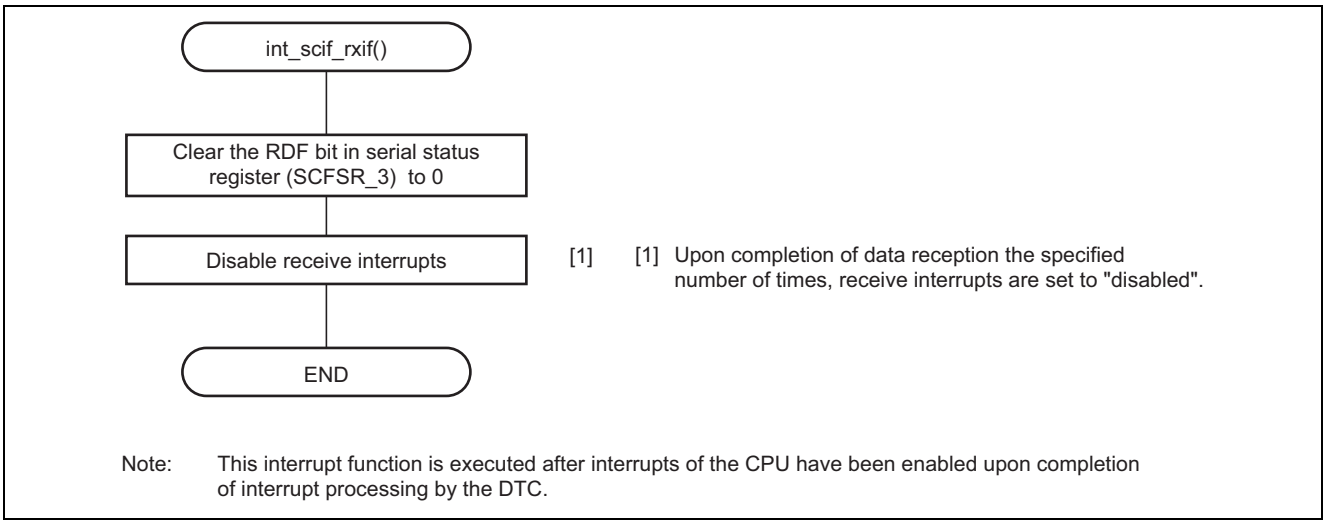


Figure 15 Flow for Handling Receive Interrupts in Asynchronous Mode

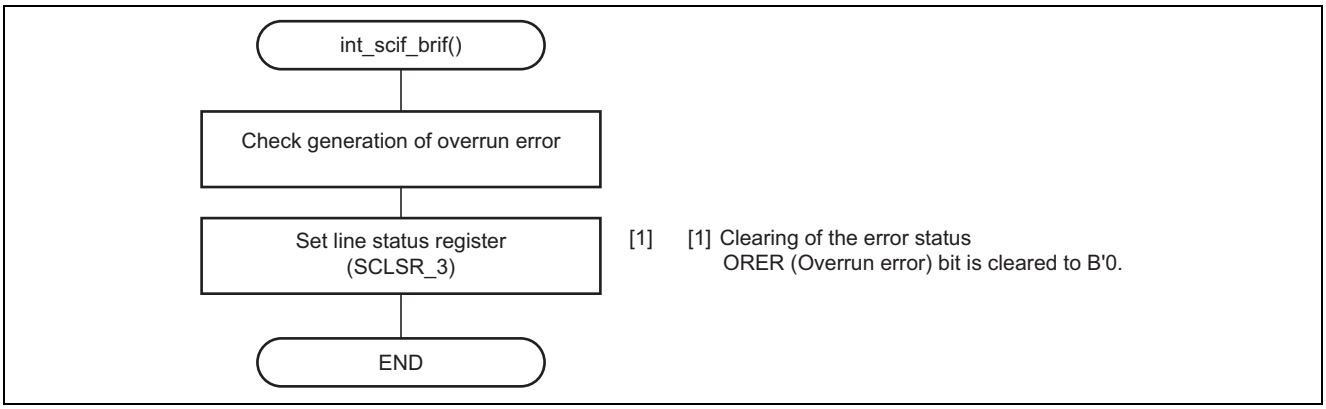


Figure 16 Flow for Handling Receive Error Interrupts in Asynchronous Mode

2.3 Processing Sequence of the Sample Program

2.3.1 Clock Pulse Generator (CPG)

Table 5 gives settings for the register of the clock pulse generator in the sample program.

Table 5 Settings for Register in Clock Pulse Generator

Register Name	Address	Setting	Description
Frequency control register (FRQCR)	H'FFFE 0010	H'0101	STC [2:0] = B'001: × 1/2 (Bϕ) IFC [2:0] = B'000: × 1 (Iϕ) PFC [2:0] = B'001: × 1/2 (Pϕ)
MTU2S clock frequency control register (MCLKCR)	H'FFFE 0410	H'41	MSSCS[1:0] = B'01: PLL output clock MSDIVS[1:0] = B'01: × 1/2 (Mϕ)
AD clock frequency control register (ACLKCR)	H'FFFE 0414	H'41	ASSCS[1:0] = B'01: PLL output clock ASDIVS[1:0] = B'01: × 1/2 (Aϕ)

2.3.2 Power-Down Modes

Table 6 gives settings for the standby control register in the sample program.

Table 6 Settings for Standby Control Register

Register Name	Address	Setting	Description
Standby control register 2 (STBCR2)	H'FFFE 0018	H'00	MSTP4 = B'0: DTC operates
Standby control register 4 (STBCR4)	H'FFFE 040C	H'E4	MSTP44 = B'0: SCIF3 operates

2.3.3 Interrupt Controller (INTC)

Table 7 gives settings for the register of the interrupt controller in the sample program.

Table 7 Settings for Register of the Interrupt Controller

Register Name	Address	Setting	Description
Interrupt priority register 14 (IPR14)	H'FFFE 0C10	H'000F	IPR14[3:0] = B'F: SCIF3 is at a level 15

Note: The order of priority for RXI3 and TXI3 is determined by the order of the offset addresses of the corresponding interrupt vectors. For details of the interrupt priority levels, refer to the description of the interrupt exception handling vector table and priority in the interrupt controller section of the *SH7280 Group Hardware Manual* (REJ09B0393).

2.3.4 Pin Function Controller (PFC)

Table 8 gives settings for the registers of the pin function controller in the sample program.

Table 8 Settings for Register of Pin Function Controller

Register Name	Address	Setting	Description
Port A control register L3 (PACRL3)	H'FFFE 3812	H'0055	PA8MD[2:0] = B'101: TXD3 output PA9MD[2:0] = B'101: RXD3 input

2.3.5 Data Transfer Controller (DTC)

Table 9 gives settings for the registers of the DTC in the sample program.

Table 9 Settings for Data Transfer Controller

Register Name	Address	Setting	Description
DTC control register (DTCCR)	H'FFFE 6010	H'10	RRS = B'0: Read skip is not performed RCHNE = B'0: Disables the chained transfer ERR = B'0: No interrupt request occurs
DTC vector base register (DTCVBR)	H'FFFE 6014	H'FFF8 6000	Setting for the DTC vector base address

- SCIF3 transmission: Setting transfer information (MRA, MRB, SAR, DAR, CRA, and CRB)

Register Name	Address	Setting	Description
DTC mode register A (MRA)	H'FFF8 0000 (On-chip RAM)*[1]	H'08	MD[1:0] = B'00: Normal transfer mode Sz[1:0] = B'00: Byte-size transfer SM[1:0] = B'10: Increments SAR
DTC mode register B (MRB)	H'FFF8 0001 (On-chip RAM)*[1]	H'00	CHNE = B'0: Disables chained transfer CHNS = B'0: Chained transfer every time DISEL = B'0: Generates CPU interrupt request DTS = B'0: Specifies the destination as repeat or block area DM[1:0] = B'00: DAR is fixed
DTC source address register (SAR)	H'FFF8 0004 (On-chip RAM)*[1]	—	Specifies transfer source address Buffer for transmission (&SndData[0])
DTC destination address register (DAR)	H'FFF8 0008 (On-chip RAM)*[1]	SCFTDR_3	Specifies transfer destination address Transmit FIFO data register (SCFTDR)
DTC transfer count register A (CRA)	H'FFF8 000C (On-chip RAM)*[1]	H'20	Specifies the number of unit transfers as 32
DTC enable register E (DTCERE)	H'FFFE 6008	H'0400	Selects interrupt source to activate the DTC TXI_3

- SCIF3 reception: Setting transfer information (MRA, MRB, SAR, DAR, CRA, and CRB)

Register Name	Address	Setting	Description
DTC mode register A (MRA)	H'FFF8 0010 (On-chip RAM)*[1]	H'00	MD[1:0] = B'00: Normal transfer mode Sz[1:0] = B'00: Byte-size transfer SM[1:0] = B'00: SAR is fixed
DTC mode register B (MRB)	H'FFF8 0011 (On-chip RAM)*[1]	H'08	CHNE = B'0: Disables chained transfer CHNS = B'0: Chained transfer every time DISEL = B'0: Generates CPU interrupt request DTS = B'0: Specifies the destination as repeat or block area DM [1:0] = B'10: Increments DAR
DTC source address register (SAR)	H'FFF8 0014 (On-chip RAM)*[1]	SCFRDR_3	Specifies transfer source address Receive data register (SCFRDR)
DTC destination address register (DAR)	H'FFF8 0018 (On-chip RAM)*[1]	—	Specifies transfer destination address Buffer for reception (&RcvData[0])
DTC transfer count register A (CRA)	H'FFF8 001C (On-chip RAM)*[1]	H'20	Specifies the number of unit transfers as 32
DTC enable register E (DTCERE)	H'FFFE 6008	H'0800	Selects interrupt source to activate the DTC RXI_3

Note: 1. The allocation of transfer information depends on the memory allocation of the compiler. Accordingly, when the setting is changed, the allocation address may also be changed.

2.3.6 Serial Communications Interface with FIFO

Table 10 gives settings for the registers of the SCIF in the sample program.

Table 10 Settings for SCIF Register

Register Name	Address	Setting	Description
Serial mode register_3 (SCSMR_3)	H'FFFE 9800	H'0000	C/$\overline{A}$ = B'0: Asynchronous mode CHR = B'0: 8-bit data PE = B'0: Disables appending and checking of parity bits STOP = B'0: 1 stop bit CKS[1:0] = B'00: Pϕ clock
Bit rate register_3 (SCBRR_3)	H'FFFE 9804	D'124	Asynchronous mode Bit rate: 38,400 (bit/s) *[1]
Serial control register_3 (SCSCR_3)	H'FFFE 9808	H'0000	Initialization TIE = B'0: Disables transmit-FIFO-data-empty-interrupt (TXI) request RIE = B'0: Disables receive-FIFO-data-full-interrupt (RXI) and receive-error-interrupt (ERI) requests TE = B'0: Disables transmission of data RE = B'0: Disables reception of data
			At the time of setting Asynchronous mode CKE[1:0] = B'00: Internal clock, SCK pin is used as an input pin
		H'00F0	Enabling transmission and reception of data TIE = B'1: Enables transmit-FIFO-data-empty interrupt (TXI) request RIE = B'1: Enables receive-FIFO-data-full interrupt (RXI) request TE = B'1: Enables transmission of data RE = B'1: Enables reception of data
Serial status register_3 (SCSSR_3)	H'FFFE 9810	H'0060	Initial value TDFE = B'1: Transmit FIFO data empty flag TEND = B'1: Transmit end flag
		H'0000	At the time of setting All flags are cleared to 0.

Note: 1. For details on bit rate settings, see the table of bit rates and SCBRR settings in the section on the serial communications interface with FIFO of the *SH7280 Group Hardware Manual* (REJ09B0393).

3. Documents for Reference

- Software Manual
  SH-2A, SH2A-FPU Software Manual (REJ09B0051)
  The most up-to-date version of this document is available on the Renesas Technology Website.

- Hardware Manual
  SH7280 Group Hardware Manual (REJ09B0393)
  The most up-to-date version of this document is available on the Renesas Technology Website.

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