R32C/100 Series

Using DMAC II to Transfer Calculated Immediate Data + Data in Memory

Abstract

This document describes a method of transferring the result of immediate data and data in memory added together to any memory location using DMAC II in the R32C/100 Series.

Products

MCUs: R32C/116 Group, R32C/117 Group, and R32C/118 Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

When an INT0 interrupt request is generated, an immediate data + data in memory calculation transfer is performed.

Table 1.1 lists the Peripheral Functions and Their Applications. Figure 1.1 and Figure 1.2 show the Block Diagram and Bus Timing, respectively.

Table 1.1   Peripheral Functions and Their Applications

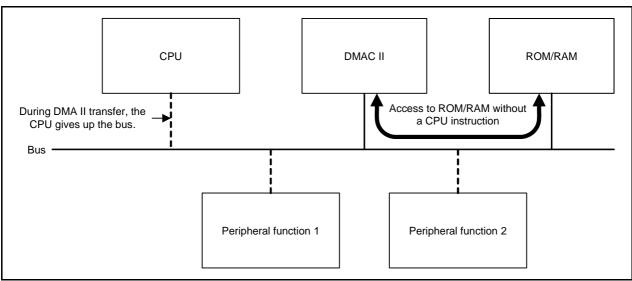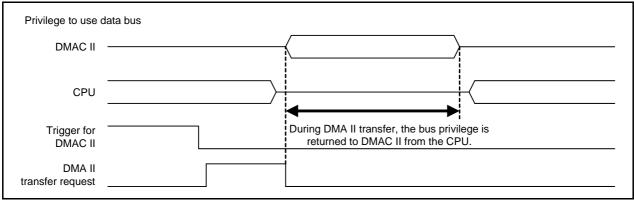| Peripheral Function	Application
DMAC II	Immediate data + data in memory is transferred to memory (calculation transfer)
INT0 interrupt	Trigger for DMAC II

Figure 1.1   Block Diagram

Figure 1.2   Bus Timing

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1   Operation Confirmation Conditions

Item	Contents
MCU used	R5F64189DFD (R32C/118 Group)
Operating frequencies	Main clock: 16 MHz PLL clock: 100 MHz Base clock: 50 MHz CPU clock: 50 MHz Peripheral bus clock: 25 MHz Peripheral function clock source: 25 MHz
Operating voltage	5 V
Integrated development environment	Renesas Electronics Corporation High-performance Embedded Workshop Version 4.07
C compiler	Renesas Electronics Corporation R32C/100 Series C Compiler V.1.02 Release 01
	Compile options -D__STACKSIZE__=0X300 -D__ISTACKSIZE__=0X300 -DVECTOR_ADR=0x0FFFFFBDC -c -finfo -dir "$(CONFIGDIR)" (Default setting is used in the integrated development environment.)
Operating mode	Single-chip mode
Sample code version	Version 1.00
Board used	Renesas Starter Kit for R32C/118 (product name: R0K564189S000BE)

3. Reference Application Note

The application note associated with this application note is listed below. Refer to the following application note for additional information.

- R32C/100 Series Configuring PLL Mode (REJ05B1221-0100)

4. Hardware

4.1 Pin Used

Table 4.1 lists the Pin Used and Its Function.

Table 4.1   Pin Used and Its Function

Pin Name	I/O	Function
P8_2/INT0	Input	DMAC II trigger (INT0 interrupt) input

5. Software

5.1 Operation Overview

When an interrupt request is generated with interrupt request level 7, an immediate data + a data in memory calculation transfer is performed. In this application note, the INT0 interrupt is set to interrupt request level 7.

(1) DMAC II initial settings:
  Set the DMAC II index and DMAC II trigger. Also, set the $\overline{INT0}$ pin and INT0 interrupt control register to use the INT0 interrupt as a trigger for DMAC II.

  Settings for the DMAC II index are as follows:
  • Transfer size: 8 bits
  • Transfer type: Immediate data
  • Source addressing: Increment
  • Destination addressing: Fixed
  • Calculation transfer: Used
  • Transfer mode: Single transfer
  • Transfer complete interrupt: Not used
  • Chained transfer: Not used
  • Transfer counter (COUNT): Five times
  • Source address (SADR): Immediate data (20h)
  • Operation address (OADR): Operation address (400h)
  • Destination address (DADR): Destination address (1000h)

(2) When the INT0 interrupt is generated:
  When the INT0 interrupt is generated, an immediate data set in the source address (SADR) of the DMAC II index and data in the memory specified by the operation address (OADR) are added, and DMAC II transfers the calculated result to the address specified in the destination address (DADR). After the data is transferred, 1 is subtracted from the transfer counter (COUNT) and 1 is added to OADR. [1]
  When COUNT becomes 0, even if the INT0 interrupt is generated, DMA II transfer is not performed.

Note:
  1. When the transfer size is 8 bits. When the transfer size is 16 bits, 2 is added.

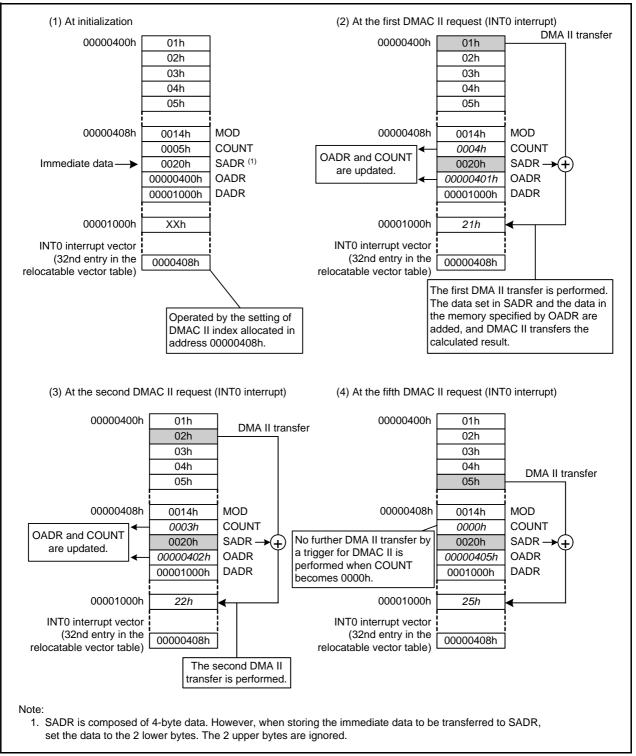Figure 5.1 shows a DMA II Transfer Operation Example.

Figure 5.1   DMA II Transfer Operation Example

5.2   Invariable Table

Table 5.1 lists the Invariables Used in the Sample Code.

Table 5.1   Invariables Used in the Sample Code

Invariable Name	Setting Value	Contents
DEST_ADDRESS	1000h	DMA II destination address
TRANS_COUNT	5	Number of DMA II transfers
IMM_DATA	0020h	Immediate data

5.3   Structure/Union List

Figure 5.2 shows the Structure/Union Used in the Sample Code.

```
// DMAC II index

struct{
  union {
    struct{
      char   size:1;                  // Transfer size select bit
      char   imm:1;                   // Transfer source select bit
      char   upds:1;                  // Source addressing select bit
      char   updd:1;                  // Destination addressing select bit
      char   oper:1;                  // Calculation transfer select bit
      char   brst:1;                  // Burst transfer select bit
      char   inte:1;                  // Transfer complete interrupt select bit
      char   chain:1;                 // Chained transfer select bit
      char   reserve:7;               //
      char   mult:1;                  // Multiple transfer select bit
    }mod_bit;
    unsigned short mod_word;
  }mod;
  unsigned short count;               // transfer counter
  unsigned long sadr;                 // source address
  unsigned char far *oadr;            // operation address
  unsigned char far *dadr;            // destination address
}dm_index;
```

Figure 5.2   Structure/Union Used in the Sample Code

Set the starting address of the DMAC II index to the interrupt vector for the DMAC II triggerable peripheral interrupt source.
In this application note, the INT0 interrupt is used as a trigger for DMAC II.
Figure 5.3 shows a setting example of the asm function in a C language program.

```
asm( "   .rvector 31, _dm_index" );      // Define DMAC II Index (Software Interrupt Number 31)
```

Figure 5.3   Setting Example for the Starting Address of the DMAC II Index to the Interrupt Vector

5.4 Variable Table

Table 5.2 lists the Global Variables.

Table 5.2 Global Variables

Type	Variable Name	Contents	Function Used
unsigned char	cal_data[]	Data to be calculated for DMA II transfer (01h, 02h, 03h, 04h, and 05h)	DMACII_init
struct	dm_index	DMAC II index	DMACII_init

5.5 Flowcharts

5.5.1 Main Processing

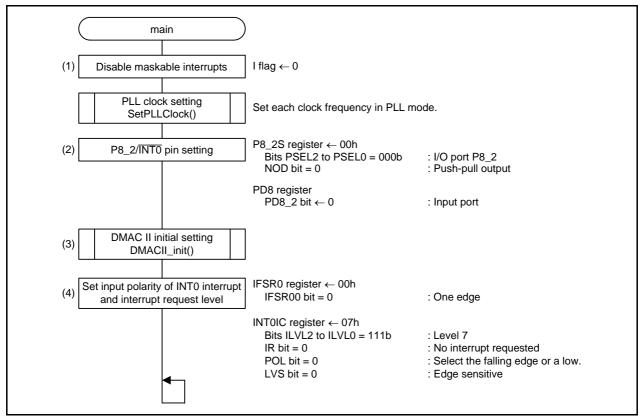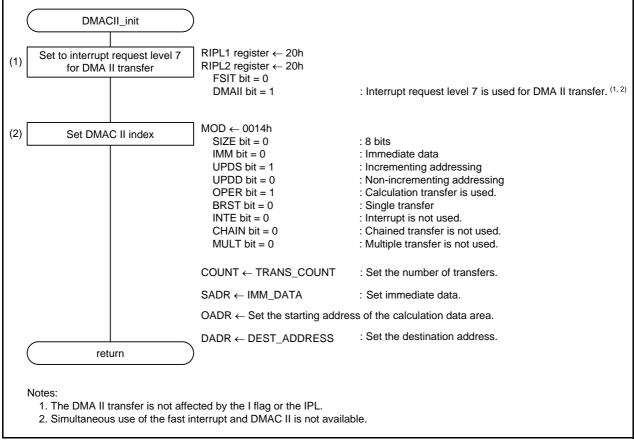Figure 5.4 shows the Main Processing.

Figure 5.4 Main Processing

5.5.2   DMAC II Initial Setting

Figure 5.5 shows the DMAC II Initial Setting.


```
                    ┌──────────────────────┐
                    │     DMACII_init      │
                    └──────────────────────┘
                                │
        ┌──────────────────────────────────┐   RIPL1 register ← 20h
 (1)    │  Set to interrupt request level 7│   RIPL2 register ← 20h
        │       for DMA II transfer        │     FSIT bit = 0
        └──────────────────────────────────┘     DMAII bit = 1              : Interrupt request level 7 is used for DMA II transfer. (1, 2)
                                │
                                │                MOD ← 0014h
 (2)    ┌──────────────────────────────────┐     SIZE bit = 0              : 8 bits
        │         Set DMAC II index        │     IMM bit = 0               : Immediate data
        └──────────────────────────────────┘     UPDS bit = 1              : Incrementing addressing
                                │                UPDD bit = 0              : Non-incrementing addressing
                                │                OPER bit = 1              : Calculation transfer is used.
                                │                BRST bit = 0              : Single transfer
                                │                INTE bit = 0              : Interrupt is not used.
                                │                CHAIN bit = 0             : Chained transfer is not used.
                                │                MULT bit = 0              : Multiple transfer is not used.
                                │
                                │                COUNT ← TRANS_COUNT        : Set the number of transfers.
                                │
                                │                SADR ← IMM_DATA           : Set immediate data.
                                │
                                │                OADR ← Set the starting address of the calculation data area.
                                │
        ┌──────────────────────┐                DADR ← DEST_ADDRESS        : Set the destination address.
        │        return        │
        └──────────────────────┘
```

Notes:
   1. The DMA II transfer is not affected by the I flag or the IPL.
   2. Simultaneous use of the fast interrupt and DMAC II is not available.

Figure 5.5   DMAC II Initial Setting

6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents

R32C/116 Group User's Manual: Hardware Rev.1.10
R32C/117 Group User's Manual: Hardware Rev.1.10
R32C/118 Group User's Manual: Hardware Rev.1.10
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual
R32C/100 Series C Compiler Package V.1.02
C Compiler User's Manual Rev.2.00
The latest version can be downloaded from the Renesas Electronics website.

8. Website and Support

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Revision History	R32C/100 Series Using DMAC II to Transfer Calculated Immediate Data + Data in Memory		

Rev.	Date	Description	
		Page	Summary
1.00	Dec. 28, 2010	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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