

APPLICATION NOTE

R01AN0851EJ0100

Rev.1.00 Feb. 15, 2012

SH7231 Group

Using CMT2 Output Compare Function

Abstract

This application note describes an example to use the output compare function with the compare match timer 2 (hereinafter called CMT2).

Products

SH7231

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.



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1. Specifications

In this application note, the dedicated pins (TOC0 and TOC1) output two square waves (carrier cycle: 200ms, duty ratio: 50%) using the CMT2 output compare function.

Table 1.1 lists the peripheral functions used and their applications. Figure 1.1 shows the block diagram of the peripheral functions.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Function	Application
Compare match timer 2 (CMT2)	Sets the output compare function (square wave output).
Pin function controller (PFC)	Sets the pin function at port H, PH15 and PH14 to output compare output 0 (TOC0) and output compare output 1 (TOC1) respectively.

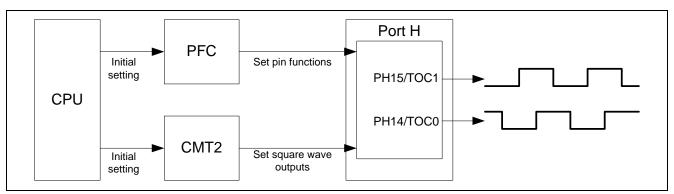


Figure 1.1 Block Diagram of Peripheral Functions for Use



2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Item	Contents
MCU used	SH7231
Operating frequency	Internal clock: 100MHz
	Bus clock: 50MHz
	Peripheral clock: 50MHz
Operating voltage	Vcc: 3.3V
Integrated development	Renesas Electronics Corporation
environment	High-performance Embedded Workshop Ver.4.08.00
C compiler	Renesas Electronics Corporation
	SuperH RISC engine family C/C++ compiler package V.9.04 Release 00
	Compile options:
	-cpu=sh2afpu -fpu=single -include="\$(WORKSPDIR)\inc"
	-object="\$(CONFIGDIR)\\$(FILELEAF).obj" -debug -gbr=auto -chgincpath
	-errorpath -global_volatile=0 -opt_range=all -infinite_loop=0
	-del_vacant_loop=0 -struct_alloc=1 -nologo
Operating mode	Single chip mode
Sample code version	1.00
Board used	R0K572310C000BR

Table 2.1 Operation Confirmation Conditions

3. Reference Application Note

For additional information associated with this document, refer to the following application note.

• SH7231 Group Example of Initialization (R01AN0322EJ)



4. Peripheral Function

This chapter provides information on compare match timer 2 (hereinafter called CMT2). Refer to the "SH7231 Group User's Manual: Hardware" for basic information.

4.1 Compare Match Timer 2 (CMT2)

CMT2 has the function to output square waves in addition to the normal compare match function. The follows are its features.

- Includes one channel of upcounter (16-bit/32-bit selectable).
- Up to two input capture input signals available.
- Up to two output compare output signals available.
- Selectable among four counter input clocks: $P\phi/8$, $P\phi/32$, $P\phi/128$, and $P\phi/512$
- Allows the counter to be cleared by input capture inputs and upon compare match.
- Five types of interrupts are available for input capture and compare match. The interrupts can be requested independently.
- Data transfer is enabled by activating data transfer controller (DTC) or the direct memory access controller (DMAC).
- Module standby mode can be set.



5. Hardware

5.1 Pins Used

Table 5.1 lists the pins used and their functions.

Table 5.1 Pins Used and Their Functions

Pin Name	I/O	Function
TOC0	Output	Output compare output 0
TOC1	Output	Output compare output 1



6. Software

6.1 Operation Overview

This section describes the square wave output operation with the CMT2 output compare function in this software. In the initialization after starting a reset, the initial data 1 (High) is output from the TOC0 pin. When the value of the timer counter (CM2CNT) and the output compare register (CM2OCR0) match, namely a compare match is generated between them, toggle output is provided. Meanwhile, TOC1 pin outputs the initial data 0 (Low), and provides toggle output upon compare match with the output compare register 1 (CM2OCR1). The CM2CNT is cleared to 0 upon compare match with the CM2OCR1.

The toggle period both at TOC0 and TOC1 are 100ms (carrier cycle: 200ms., duty ratio: 50%). The pins provide square waves with time difference of 50ms in each other. Figure 6.1 shows the operation overview.

Figure 6.3 shows the setting procedure to output the square waves shown in the Figure 6.1. For details on each register, refer to the "SH7231 Group User's Manual: Hardware".

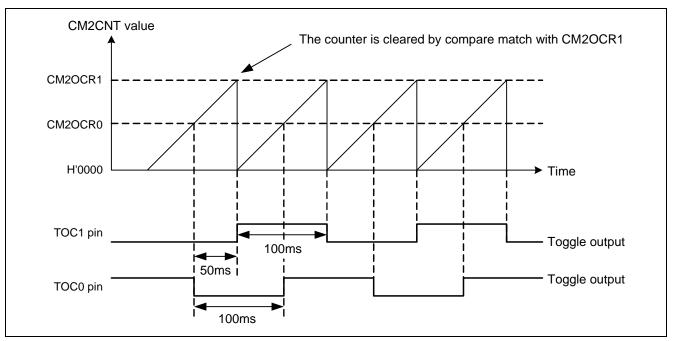


Figure 6.1 Relation between Operation and Data Transfer



6.2 File Composition

Table 6.1 lists the file used in the sample code. The files generated automatically in the integrated development environment are excluded in this table.

Table 6.1 File Used in the Sample Code

File	Outline	Remarks
main.c	Main module	Main processing, PFC setting, and CMT2 setting

6.3 Functions

Table 6.2 lists the functions.

Table 6.2 Functions

Function Name	Outline	
void main(void)	Main processing	
void io_init_pfc(void)	PFC setting	
<pre>void io_init_cmt2(void)</pre>	CMT2 setting	



6.4 Function Specifications

The following tables list the function specifications in the sample code.

Main	
Outline	Main processing
Header	
Declaration	void main(void)
Description	Sets the CMT2 output compare function to output square wave with toggle period of 100ms (carrier cycle: 200ms, duty ratio: 50%) from TOC0 and TOC1 pin.
Arguments	None
Return Value	None

io_init_pfc	
Outline	PFC setting
Header	
Declaration	void io_init_pfc(void)
Description	Sets pin functions PH15 and PH14 to TOC1 and TOC0 (output) respectively.
Arguments	None
Return Value	None

io_init_cmt2	
Outline	CMT2 setting
Header	
Declaration	void io_init_cmt2(void)
Description	After clearing CMT2 module standby, starts the timer count operation along with the CMT2 setting below.
	Timer counter size: 16 bits
	 Clock divided ratio: P
	 Enables a compare match operation with CM2OCR1 and CM2OCR0 (toggle period: 100ms, counter clear upon compare match with CM2OCR1)
	 CM2OCR1: initial output (TOC1) is 0-output, toggle output upon compare match
	— CM2OCR0: initial output (TOC0) is 1-output, toggle output upon compare match
Arguments	None
Return Value	None



6.5 Flowcharts

6.5.1 Main Processing and PFC Setting

Figure 6.2 shows the procedure of main processing and PFC setting.

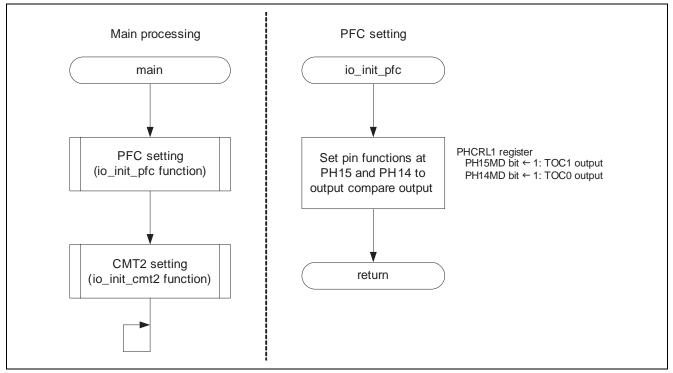


Figure 6.2 Procedure of Main Processing (main function) and PFC Setting (io_init_pfc function)



6.5.2 CMT2 Setting

Figure 6.3 shows the procedure of CMT2 setting.

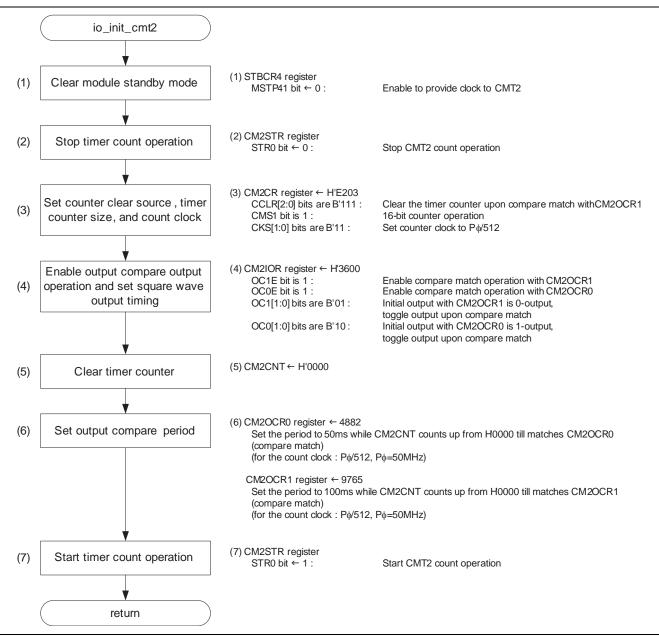


Figure 6.3 Procedure of CMT2 Setting (io_init_cmt2 function)



7. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

8. Reference Documents

User's Manual: Hardware SH7231 Group User's Manual: Hardware Rev.1.00 (R01UH0073EJ) The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News The latest information can be downloaded from the Renesas Electronics website.

User's Manual: Development Tools

SuperH C/C++ Compiler Package V.9.04 User's Manual Rev.1.01 (R20UT0704EJ) The latest version can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website http://www.renesas.com

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Devision History	SH7231 Group Application Note Using CMT2 Output Compare
Revision History	Function

Rev.	Date	Description	1
Nev.	Date	Page	Summary
1.00	Feb. 15, 2012	—	First edition issued

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

- 1. Handling of Unused Pins
 - Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
 - The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flow internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
- 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

 The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

- 3. Prohibition of Access to Reserved Addresses
 - Access to reserved addresses is prohibited.

The reserved addresses are provided for the possible future expansion of functions. Do not access
these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
- 5. Differences between Products

Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.

— The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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