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SH7080/SH7146/SH7125/SH7200 Series

Skipping the Activation of A/D Converter Using MTU2

Introduction

This application note discusses how to implement skipping of the A/D converter activation when three-phase complementary PWM waveforms are output.

Target Device

- Microcomputer: SH7085 (R5F7085)
- Operating frequency: Internal clock 80 MHz
  Bus clock 40 MHz
  Peripheral clock 40 MHz
  MTU2 clock 40 MHz
  MTU2S clock 80 MHz
- C compiler: Ver. 7.1.04 of Renesas C compiler.

Contents

1. Specifications

In this task sample, the A/D converter is activated while three-phase complementary PWM waveforms are being output from channels 3 and 4 (ch3 and ch4) of the MTU2. Activation of the A/D converter is skipped specified number of times. The basic specifications of this sample task are as follows.

- Three-phase complementary PWM waveforms including dead time are output from ch3 and ch4 of the MTU2, and a toggle output synchronized with the PWM period is output from the TIOC3A pin.
- The A/D converter is activated on compare-match between TCNT_4 and TADCORA_4 while TCNT_4 is counting upward.
- The A/D converter activation is skipped twice in linked operation with the skipping of compare-match interrupts on ch3 (TGIA3).
- The A/D converter operates in single mode.
- The result of A/D conversion is stored to the on-chip RAM at each A/D conversion end interrupt.

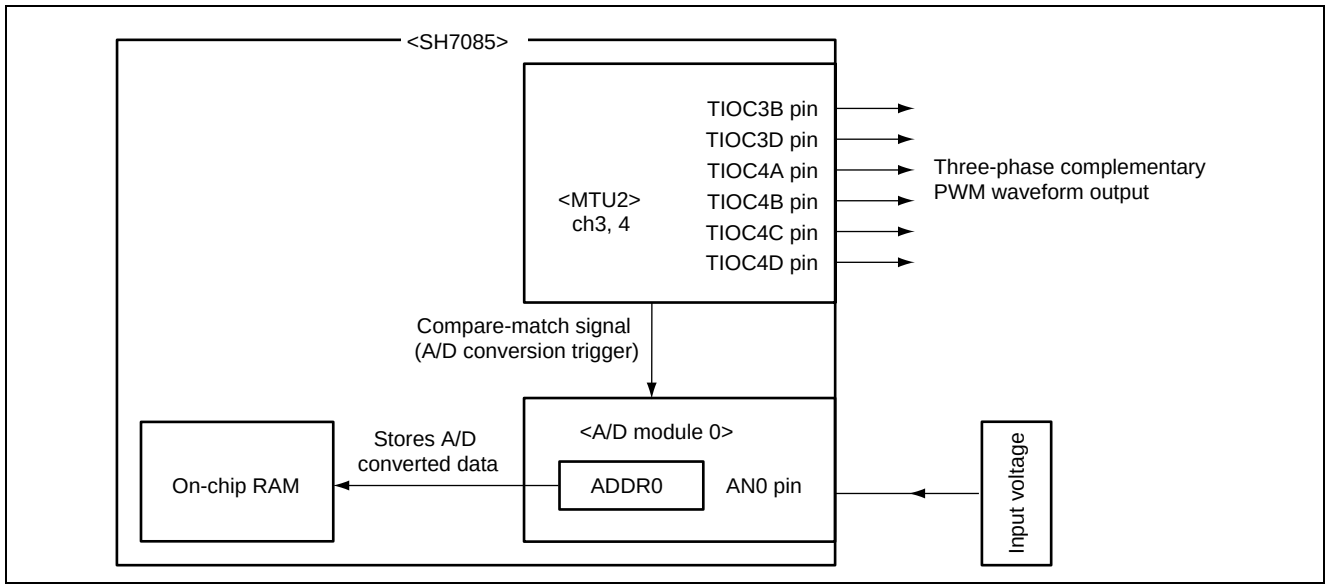


Figure 1 Block Diagram of A/D Conversion Controlled by MTU2

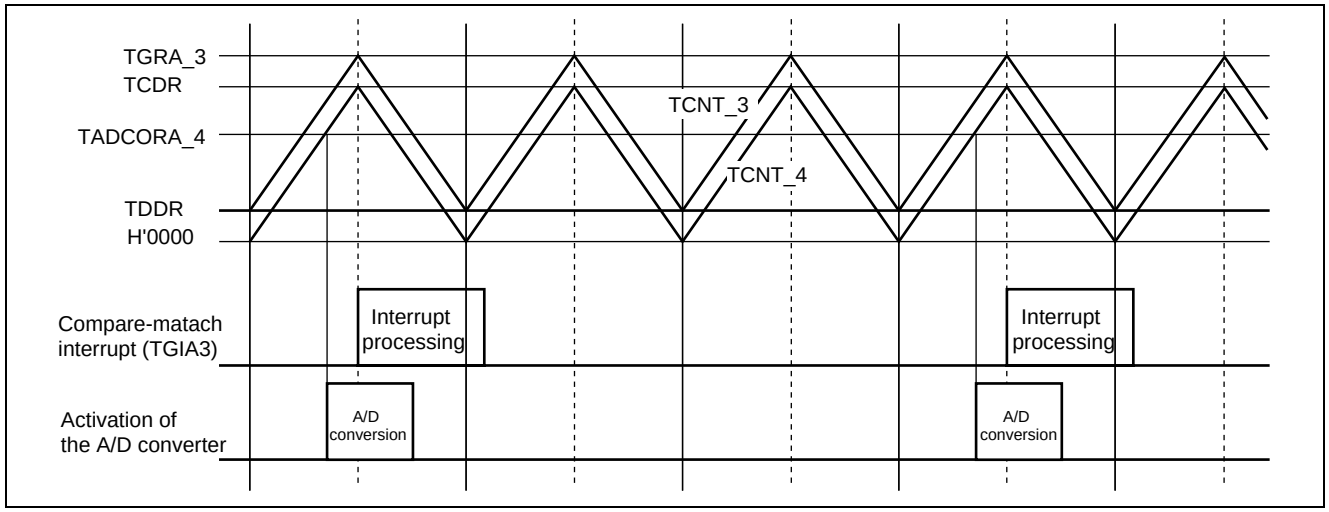


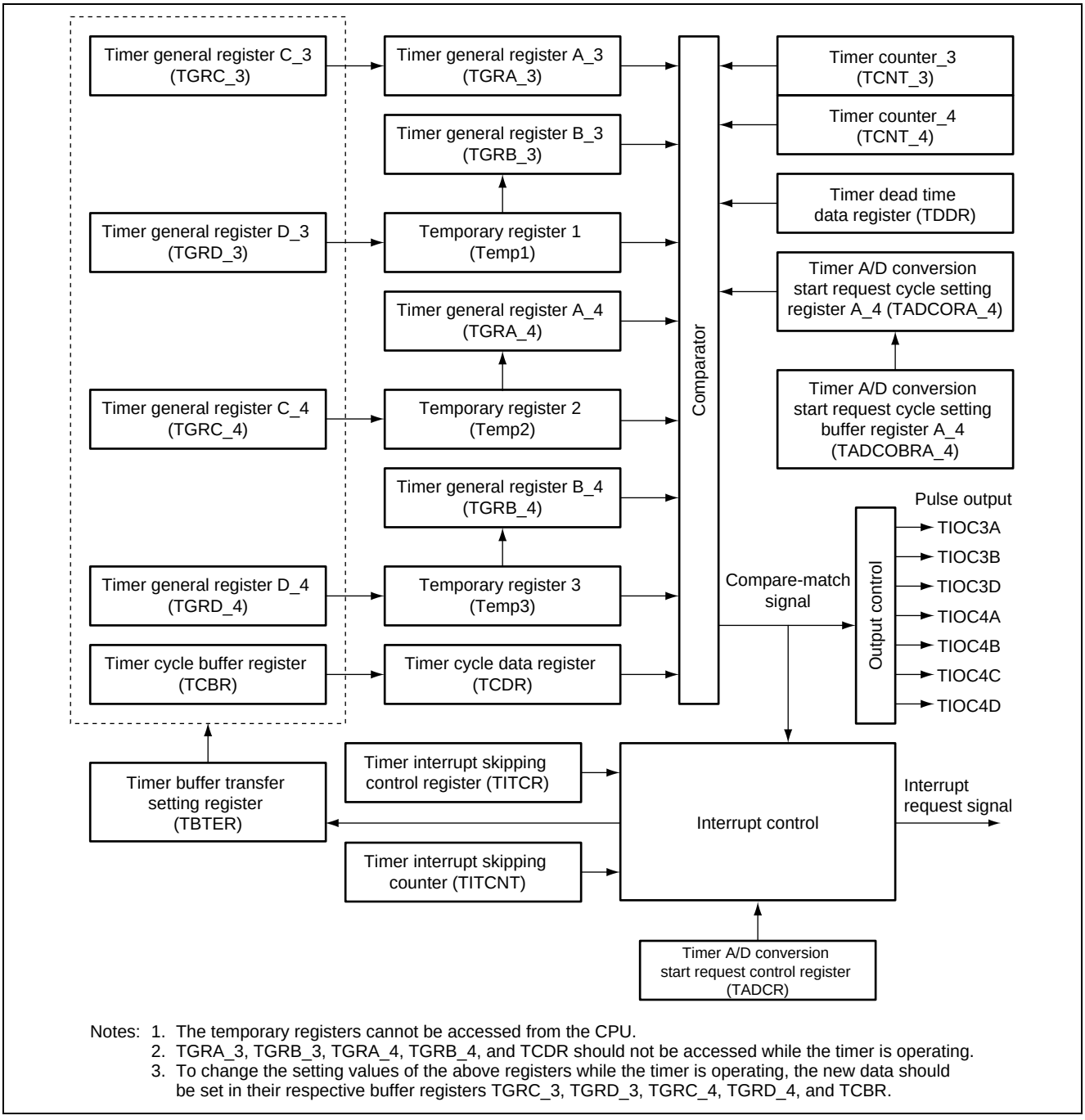
Figure 2 A/D Conversion Linked with TGIA3 Interrupt Skipping

2. Description of Functions

In this sample task, the A/D converter is activated by linked operation of the MTU2's A/D conversion start request delaying function and interrupt skipping function.

2.1 MTU2 (Multi-Function Timer Pulse Unit 2)

Figure 3 shows a block diagram of the MTU2 (ch3 and ch4) when the interrupt skipping function is used, with an explanation of the function noted below.



Notes: 1. The temporary registers cannot be accessed from the CPU.
2. TGRA_3, TGRB_3, TGRA_4, TGRB_4, and TCDR should not be accessed while the timer is operating.
3. To change the setting values of the above registers while the timer is operating, the new data should be set in their respective buffer registers TGRC_3, TGRD_3, TGRC_4, TGRD_4, and TCBR.

Figure 3 Block Diagram of MTU2 (ch3 and ch4) When Interrupt Skipping is Used

- The timer general register A_3 (TGRA_3) operates as a compare register. A value that corresponds to half the PWM pulse period should be set in TGRA_3. To change the setting value during timer operation, a new value should be set in the timer general register C_3 (TRGC_3).
- The timer general register B_3 (TGRB_3) operates as a compare register. The duty cycle of the PWM waveforms output from the TIOC3B and TIOC3D pins should be set in TGRB_3. To change the setting value during timer operation, a new value should be set to the timer general register D_3 (TRGD_3).
- The timer general register C_3 (TGRC_3) operates as the buffer register for TGRA_3. While the timer is operating, the TGRC_3 value is reflected to TGRA_3.
- The timer general register D_3 (TGRD_3) operates as the buffer register for TGRB_3. If the value of TGRD_3 is changed during timer operation, a new value will be transferred to the temporary register 1 (TEMP1) and reflected to TGRB_3.
- The timer general register A_4 (TGRA_4) operates as a compare register. The duty cycle of the PWM waveforms output from the TIOC4A and TIOC4C pins should be set in TGRA_4. To change the setting value during timer operation, a new value should be set in the timer general register C_4 (TRGC_4).
- The timer general register B_4 (TGRB_4) operates as a compare register. The duty cycle of the PWM waveforms output from the TIOC4B and TIOC4D pins should be set in TGRB_4. To change the setting value during timer operation, a new value should be set in the timer general register D_4 (TRGD_4).
- The timer general register C_4 (TGRC_4) operates as the buffer register for TGRA_4. While the timer is operating, the TGRC_4 value is reflected to TGRA_4.
- The timer general register D_4 (TGRD_4) operates as the buffer register for TGRB_4. While the timer is operating, the TGRD_4 value is reflected to TGRB_4.
- The temporary registers 1 to 3 (TEMP1 to TEMP3) are located between the buffer registers and compare registers. Data written to the buffer register is transferred to the corresponding temporary register, and then transferred to the compare register. The temporary registers cannot be accessed from the CPU.
- The timer counter_3 (TCNT_3) is a 16-bit readable/writable counter. TCNT_3 counts downward after a compare-match with TGRA_3, and counts upward after a compare-match with the timer dead time data register (TDDR).
- The timer counter_4 (TCNT_4) is a 16-bit readable/writable counter. TCNT_4 counts downward after a compare-match with the timer cycle data register (TCDR), and counts upward after it reaches H'0000.

- The timer dead time data register (TDDR) is a 16-bit readable/writable register. Dead time of PWM waveforms should be set in TDDR.
- The timer cycle data register (TCDR) is a 16-bit readable/writable register. A value that corresponds to half the PWM carrier period should be set in TCDR.
- The timer cycle buffer register (TCBR) operates as the buffer register for TCDR. While the timer is operating, the TCBR value is reflected to TCDR.
- The timer interrupt skipping control register (TITCR) enables/disables skipping of interrupts. The number of times interrupts will be skipped is set in TITCR. TCNT_3 compare-match interrupts (TGIA_3) and TCNT_4 underflow interrupts (TCIV_4) can be skipped up to seven times in complementary PWM mode.
- The timer interrupt skipping counter (TITCNT) counts the number of times compare-match interrupts are skipped. TITCNT is cleared when its value matches the TITCR setting value.
- The timer buffer transfer setting register (TBTER) specifies whether or not data transfer from a buffer register to a temporary register is suppressed. When transfer is not suppressed, it also sets whether or not transfer operation is linked with the interrupt skipping function.
- The timer A/D conversion start request control register (TADCR) is a 16-bit readable/writable register. TADCR enables/disables generation of A/D conversion start requests and specifies whether or not request generation is linked with the interrupt skipping function.
- The timer A/D conversion start request cycle setting register A_4 (TADCORA_4) is a 16-bit readable/writable register. A corresponding A/D conversion start request is generated when the setting value matches the TCNT_4 setting value.
- The timer A/D conversion start request cycle setting buffer register A_4 (TADCOBRA_4) operates as a buffer register for TADCORA_4. During timer operation, the TADCOBRA_4 value is reflected to TADCORA_4.

2.2 A/D Converter

In this sample task, the A/D module 0 is activated by an A/D conversion trigger (TRG4AN) generated by the MTU2, and performs A/D conversion in single mode. Figure 4 shows a block diagram of the A/D 0 module, with a description of the functions noted below.

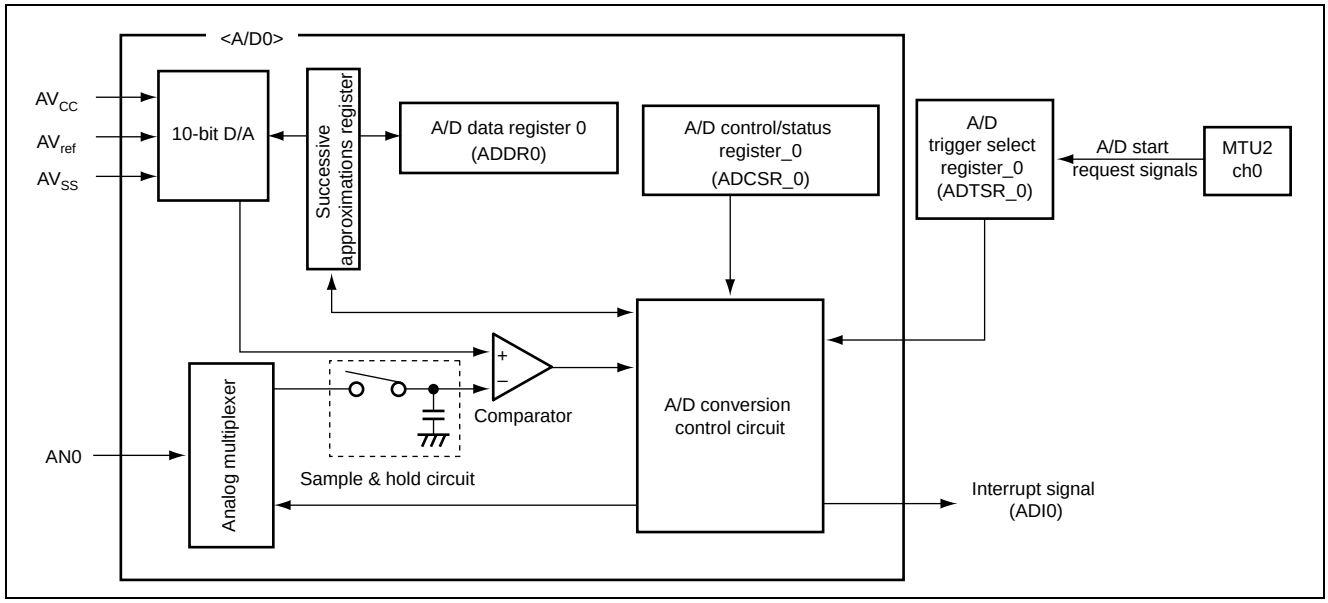
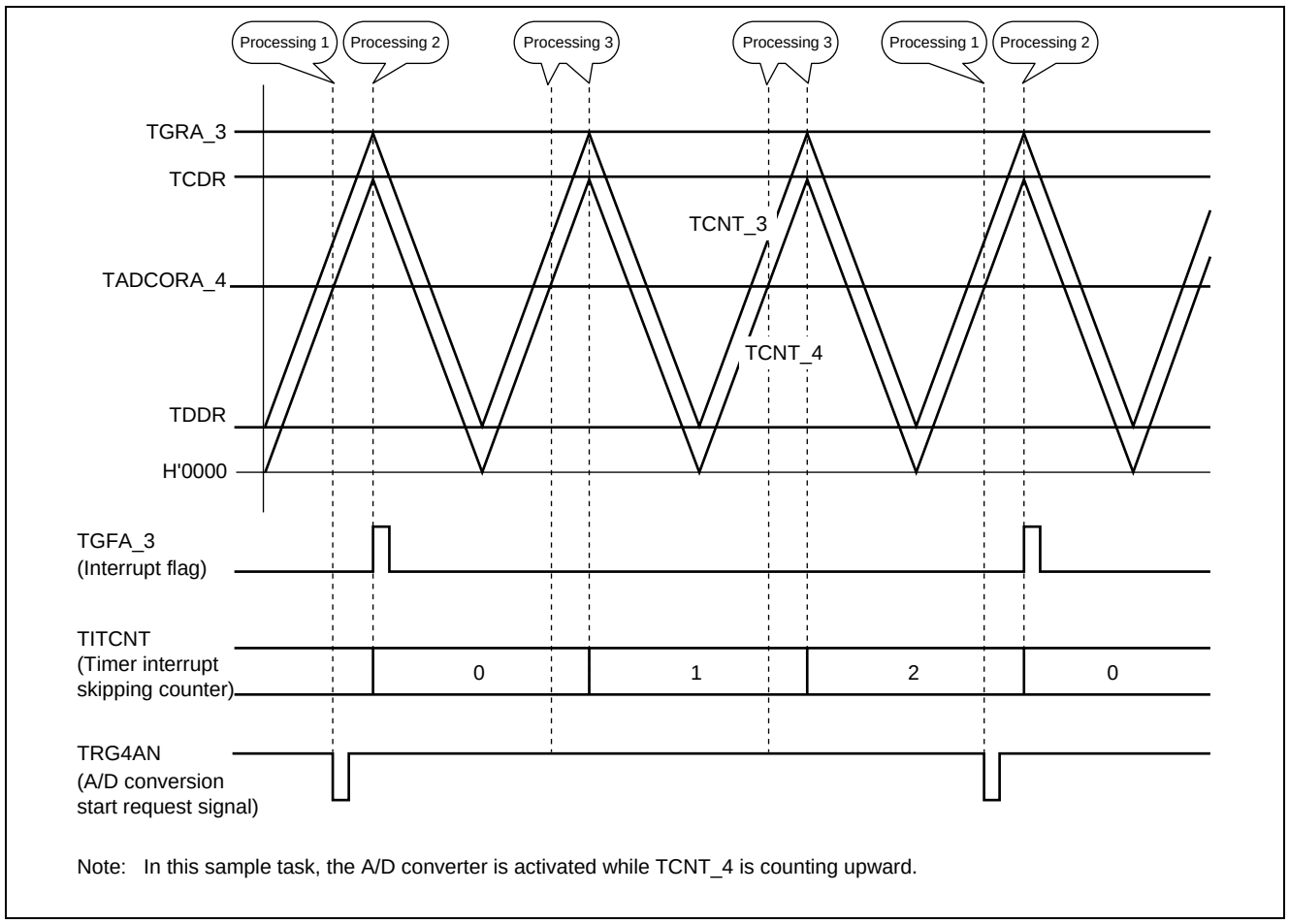


Figure 4 Block Diagram of A/D Module 0

- The A/D data register 0 (ADDR0) is a 16-bit read only register that is used to store the A/D-converted result of the data input from the analog input channel (AN0). The converted data is stored to the upper 10 bits (bits 15 to 6), and the lower 6 bits are always 0.
- The A/D control/status register_0 (ADCSR_0) controls A/D conversion operation.
- The A/D trigger select register_0 (ADTSR_0) selects an external trigger to start A/D conversion.

3. Description of Operation

Figure 5 illustrates the operation of this sample task, and table 1 describes the operation in terms of software and hardware processing.



Note: In this sample task, the A/D converter is activated while TCNT_4 is counting upward.

Figure 5 Principles of Operation

Table 1 Software and Hardware Processing

	Software Processing	Hardware Processing
Processing 1	—	• Generate compare-match between TCNT_4 and TADCORA_4. • Output an A/D conversion start request signal (TRG4AN) to the A/D converter. • Start A/D conversion.
Processing 2	• Clear the compare-match interrupt flag (TGFA_3). • Update the duty cycle.	• Generate a TGRA_3 compare-match interrupt. • Clears TITCNT.
Processing 3	—	• Cancel the A/D conversion start request signal and TGRA_3 compare-match interrupt request signal. • Increment TITCNT.

4. Description of Software

4.1 Modules

Table 2 describes the modules of this sample task.

Table 2 Description of Modules

Module Name	Label Name	Functions
Main routine	main()	Makes initial settings of MTU2 and starts the timer counters.
TGRA_3 compare-match interrupt routine	int_tgia3()	Changes the duty cycle and updates the timing of A/D conversion.
A/D conversion end interrupt routine	int_ad0()	Stores the result of A/D conversion to the on-chip RAM.

4.2 Internal Registers

Table 3 shows the registers used in this sample task. Note that the settings in the tables are the values used in this sample task, and are different from their initial values.

Table 3 Description of Internal Registers

Register	Bit	Bit Name	Function	Setting
FRQCR			Frequency Control Register Specifies the ratios for dividing the output frequency of the PLL circuit to generate operating clocks. FRQCR = H'0241 sets the division ratios as follows. Internal clock: ×1 Bus clock: ×1/2 Peripheral clock: ×1/2 MTU2S clock: ×1 MTU2 clock: ×1/2	H'0241
STBCR4			Standby Control Register 4	H'BE
	6	MSTP22	Module Stop 22 Clock is supplied to MTU2 when MSTP22 = b'0.	0
	0	MSTP16	Module Stop 16 Clock is supplied to AD_0 when MSTP16 = b'0.	0
PECRL3			Port E Control Register L3	H'1011
	15	—	Reserved	0
	14	PE11MD2	PE11 Mode	0
	13	PE11MD1	Select TIOC3D as the pin function when PE11MD2 to	0
	12	PE11MD0	PE11MD0 = b'001.	1
	11	—	Reserved	0
	10	PE10MD2	PE10 Mode	0
	9	PE10MD1	Select PE10 (general I/O) as the pin function when	0
	8	PE10MD0	PE10MD2 to PE10MD0 = b'000	0

Register	Bit	Bit Name	Function	Setting
PECRL3	7	—	Reserved	0
	6	PE9MD2	PE9 Mode	0
	5	PE9MD1	Select TIOC3B as the pin function when PE9MD2 to	0
	4	PE9MD0	PE9MD0 = b'001.	1
	3	—	Reserved	0
	2	PE8MD2	PE8 Mode	0
	1	PE8MD1	Select TIOC3A as the pin function when PE8MD2 to	0
	0	PE8MD0	PE8MD0 = b'001.	1
PECRL4			Port E Control Register L4	H'1111
	15	—	Reserved	0
	14	PE15MD2	PE15 Mode	0
	13	PE15MD1	Selects TIOC4D as the pin function when PE15MD2 to	0
	12	PE15MD0	PE15MD0 = b'001.	1
	11	—	Reserved	0
	10	PE14MD2	PE14 Mode	0
	9	PE14MD1	Selects TIOC4C as the pin function when PE14MD2 to	0
	8	PE14MD0	PE14MD0 = b'001.	1
	7	—	Reserved	0
	6	—	Reserved	0
	6	PE13MD2	PE13 Mode	0
	5	PE13MD1	Selects TIOC4B as the pin function when PE13MD1 and	1
	4	PE13MD0	PE13MD0 = b'01.	
	3	—	Reserved	0
	2	PE12MD2	PE12 Mode	0
	1	PE12MD1	Selects TIOC4A as the pin function when PE12MD2 to	0
	0	PE12MD0	PE12MD0 = b'001.	1
PEIORL			Port E I/O Register L Sets the PWM output pins (TIOC3A, TIOC3B, TIOC3D, TIOC4A, TIOC4B, TIOC4C and TIOC4D pins) to function as output pins.	H'FB00
IPRE			Interrupt Priority Register E Sets the TGIA_3 interrupt level of the MTU2 to 10.	H'00A0
IPRK			Interrupt Priority Register K Sets the ADI_0 interrupt level of the A/D converter to10.	H'A000
TCR_3			Timer Control Register_3	H'01
	7	CCLR2	Counter Clear 2,1,0	0
	6	CCLR1	Disables clearing of TCNT_3 when CCLR2 to CCLR0 =	0
	5	CCLR0	b'000.	0
	4	CKEG1	Clock Edge 1,0	0
	3	CKEG0	When CKEG1 and CKEG0 = b'00, TCNT_3 counts rising edges of the internal clock.	0
	2	TPSC2	Timer Prescaler 2,1,0	0
	1	TPSC1	When TPSC2 to TPSC0 = b'001, the clock source for	0
	0	TPSC0	TCNT_3 is MPϕ/4.	1

Register	Bit	Bit Name	Function	Setting
TCR_4			Timer Control Register_4	H'01
	7	CCLR2	Counter Clear 2, 1, 0	0
	6	CCLR1	Disables clearing of TCNT_4 when CCLR2 to CCLR0 =	0
	5	CCLR0	b'000.	0
	4	CKEG1	Clock Edge 1,0	0
	3	CKEG0	When CKEG1 and CKEG0 = b'00, TCNT_4 counts rising edges of the internal clock.	0
	2	TPSC2	Timer Prescaler 2, 1, 0	0
	1	TPSC1	When TPSC2 to TPSC0 = b'001, the clock source for	0
	0	TPSC0	TCNT_4 is MPϕ/4.	1
TCNT_3			Timer Counter_3 The timer counter for channel 3 The same value as the timer dead time data register (TDDR) value is set.	Dead_time
TCNT_4			Timer Counter_4 The timer counter for channel 4 H'0000 is set.	H'0000
TGRA_3			Timer General Register A_3 TCNT_3 starts counting downward on compare-match with TGRA_3. Used to set carrier period / 2 + dead time.	Pul_cycle
TGRB_3			Timer General Register B_3 Used to set the duty cycle of PWM waveforms output from the TIOC3B and TIOC3D pins.	Pul_duty3d
TGRC_3			Timer General Register C_3 Buffer register for TGRA_3 To change the TGRA_3 value during timer operation, a new value should be set in this register. The same value as TGRA_3 is set as the initial value.	Pul_cycle
TGRD_3			Timer General Register D_3 Buffer register for TGRB_3 To change the TGRB_3 value during timer operation, a new value should be set in this register. The same value as TGRB_3 is set as the initial value.	Pul_duty3d
TGRA_4			Timer General Register A_4 Used to set the duty cycle of PWM waveforms output from the TIOC4A and TIOC4C pins.	Pul_duty4c
TGRB_4			Timer General Register B_4 Used to set the duty cycle of PWM waveforms output from the TIOC4B and TIOC4D pins.	Pul_duty4d
TGRC_4			Timer General Register C_4 Buffer register for TGRA_4 To change the TGRA_4 value during timer operation, a new value should be set in this register. The same value as TGRA_4 is set as the initial value.	Pul_duty4c

Register	Bit	Bit Name	Function	Setting
TGRD_4			Timer General Register D_4 Buffer register for TGRB_4 To change the TGRB_4 value during timer operation, a new value should be set in this register. The same value as TGRB_4 is set as the initial value.	Pul_duty4d
TDDR			Timer Dead Time Data Register Sets the dead time.	Dead_time
TCDR			Timer Cycle Data Register Sets half the carrier period.	C_cycle
TCBR			Timer Cycle Buffer Register Buffer register for the timer cycle data register To change the TCDR value during timer operation, a new value must be set in this register.	C_cycle
TOCR1			Timer Output Control Register 1	H'40
	7	—	Reserved	0
	6	PSYE	PWM Synchronous Output Enable Enables toggle output synchronized with the PWM period of the PWM pulses on the TIOC3A pin when PSYE = b'1.	1
	5	—	Reserved	0
	4	—	Reserved	0
	3	TOCL	TOC Register Write Protect Enables writing to the TOCS, OLSN and OLSP bits in TOCR1 when TOCL = b'0.	0
	2	TOCS	TOC Select Validates TOCR1 setting when TOCS = b'0.	0
	1	OLSN	Output Level Select N Selects output level of the negative phase.	0
	0	OLSP	Output Level Select P Selects output level of the positive phase.	0
TMDR_3			Timer Mode Register_3	H'3F
	7	—	Reserved	0
	6	BFR	Buffer Operation E Reserved with channel 3.	0
	5	BFB	Buffer Operation B Selects buffer operation of TGRB_3 and TGRD_3 when BFB = b'1.	1
	4	BFA	Buffer Operation A Selects buffer operation of TGRA_3 and TGRC_3 when BFA = b'1.	1
	3	MD3	Mode 3, 2, 1, 0 Sets the timer operating mode. When MD3 to MD0 = b'1111, the timer operates in complementary PWM mode 3.	1
	2	MD2		1
	1	MD1		1
	0	MD0		1

Register	Bit	Bit Name	Function	Setting
TOER			Timer Output Enable Register	H'FF
	7	—	Reserved	1
	6	—	Reserved	1
	5	OE4D	Timer Enable TIOC4D Enables output from the TIOC4D pin when OE4D = b'1.	1
	4	OE4C	Timer Enable TIOC4C Enables output from the TIOC4C pin when OE4C = b'1.	1
	3	OE3D	Timer Enable TIOC3D Enables output from the TIOC3D pin when OE3D = b'1.	1
	2	OE4B	Timer Enable TIOC4B Enables output from the TIOC4B pin when OE4B = b'1.	1
	1	OE4A	Timer Enable TIOC4A Enables output from the TIOC4A pin when OE4A = b'1.	1
	0	OE3B	Timer Enable TIOC3B Enables output from the TIOC3B pin when OE3B = b'1.	1
TITCR			Timer Interrupt Skipping Setting Register	H'A0
	7	T3AEN	Enables/disables skipping of TGIA_3 interrupts. Enables skipping of TGIA_3 interrupts when T3AEN = b'1.	1
	6	3ACOR2	Sets the number of times TGIA_3 interrupts will be skipped (0 to 7). The TGIA_3 interrupt will be skipped twice when 3ACOR2 to 3ACOR0 = b'010.	0
	5	3ACOR1		1
	4	3ACOR0		0
	3	T4VEN	Enables/disables skipping of TCIV_4 interrupts Disables skipping of TCIV_4 interrupts when T4VEN = b'0.	0
	2	4VCOR2	Sets the number of times TCIV_4 interrupts will be skipped. In this sample task, these bits are invalid because T4VEN = 0.	0
	1	4VCOR1		0
	0	4VCOR0		0
TBTER			Timer Buffer Transfer Setting Register	H'02
	7	—	Reserved	0
	6	—		0
	5	—		0
	4	—		0
	3	—		0
	2	—		0
	1	BTE1	When BTE1 and BTE0 = b'10, data transfers from the buffer register to the temporary register are linked with interrupt skipping.	1
	0	BTE0		0

Register	Bit	Bit Name	Function	Setting
TITCNT			Timer Interrupt Skipping Counter	H'00
	7	—	Reserved	0
	6	3ACNT2	TGIA_3 interrupt counter for interrupt skipping	0
	5	3ACNT1	TGIA_3 interrupt generating condition is satisfied.	0
	4	3ACNT0	Incremented by 1 every time TGIA_3 interrupt generating condition is satisfied.	0
	3	—	Reserved	0
	2	4VCNT2	TCIV_4 interrupt counter for interrupt skipping	0
	1	4VCNT1	This counter value remains unchanged because the	0
	0	4VCNT0	T4VEN bit of the TITCR register is 0.	0
TADCOBRA_4			Timer A/D Conversion Start Request Cycle Setting Buffer Register_4 Buffer register for TADCORA	Ad_timing
TADCORA_4			Timer A/D Conversion Start Request Cycle Setting Register_4 Sets the A/D converter activation timing.	Ad_timing
TADCR			Timer A/D Conversion Start Request Control Register	H'8088
	15	BF1	TADCOBRA/B_4 Transfer Timing Select	1
	14	BF0	Specifies that the data in TADCOBRA_4 is transferred to TADCORA_4 at troughs of TCNT_4, when BF1 and BF0 = b'10.	0
	13	—	Reserved	0
	12	—		0
	11	—		0
	10	—		0
	9	—		0
	8	—		0
	7	UT4AE	Up-Count TRG4AN Enable Enables triggering by TRG4AN* while TCNT_4 is counting upward when UT4AE = b'1.	1
	6	DT4AE	Down-Count TRG4AN Enable Disables triggering by TRG4AN* while TCNT_4 is counting downward when DT4AE = b'0.	0
	5	UT4BE	Up-Count TRG4BN Enable Disables triggering by TRG4BN* while TCNT_4 is counting upward when UT4BE = b'0.	0
	4	DT4BE	Down-Count TRG4BN Enable Disables triggering by TRG4BN* while TCNT_4 is counting downward when DT4BE = b'0.	0
	3	ITA3AE	TGI3A Interrupt skipping Linkage Enable Enables triggering by TRG4AN* linked with the TGIA_3 interrupt skipping when ITA3AE = b'1.	1
	2	ITA4VE	TCI4V Interrupt skipping Linkage Enable Disables triggering by TRG4AN* linked with the TCIV_4 interrupt skipping when ITA4VE = b'0.	0

Note*: TRG4AN and TRG4BN are A/D conversion start requests generated by the A/D conversion start request delaying function.

Register	Bit	Bit Name	Function	Setting
TADCR	1	ITB3AE	TGI3A Interrupt skipping Linkage Enable Disables triggering by TRG4BN* linked with the TGIA_3 interrupt skipping when ITB3AE = b'0.	0
	0	ITB4VE	TCI4V Interrupt skipping Linkage Enable Disables triggering by TRG4BN* linked with the TCIV_4 interrupt skipping when ITB4VE = b'0.	0
ADTSR_0			A/D Trigger Select Register_0 Sets that A/D conversion in the A/D module 0 is triggered by the delayed A/D conversion start request (TRG4AN) of the MTU2.	H'0003
ADCSR_0			A/D Control/Status Register_0	H'5880
	15	ADF	A/D End Flag	0
	14	ADIE	A/D Interrupt Enable Enables ADI interrupts when ADIE = b'1.	1
	13	—	Reserved	0
	12	OPON	Operational Amplifier ON Enables the operational amplifier when OPON = b'1.	1
	11	TRGE	Trigger Enable Specifies to start A/D conversion by an external trigger or MTU2 (MTU2S) trigger when TRGE = b'1.	1
	10	—	Reserved	0
	9	CONADF	ADF Control The setting of this bit is invalid because single mode is used in this sample task.	0
	8	STC	State Control Sets the A/D conversion time to 50 states when STC = b'0.	0
	7	CKSL1	Clock Select 1,0	1
	6	CKSL0	Selects Pϕ/2 as the clock for A/D conversion when CKSL1 and CKSL0 = b'10.	0
	5	ADM1	A/D Mode 1,0	0
	4	ADM0	Selects single mode operation when ADM1 and ADM0 = b'00.	0
	3	ADCS	A/D Continuous Scanning Specifies single-cycle scanning when ADCS = b'0.	0
	2	CH2	Channel Select 2,1,0	0
	1	CH1	Selects AN0 as the analog input channel for A/D	0
	0	CH0	conversion when CH2 to CH0 = b'000.	0

Note: * TRG4AN and TRG4BN are A/D conversion start requests generated by the A/D conversion start request delaying function.

Register	Bit	Bit Name	Function	Setting
TIER_3			Timer Interrupt Enable register_3	H'01
	7	TTGE	A/D Conversion Start Request Enable Disables A/D conversion start request generation by TGRA when TTGE = b'0.	0
	6	TTGE2	A/D Conversion Start Request Enable 2 Reserved with channel 3.	0
	5	TCIEU	Underflow Interrupt Enable Reserved with channel 3.	0
	4	TCIEV	Overflow Interrupt Enable Disables interrupt requests by the TCFV flag when TCIEV = b'0.	0
	3	TGIED	TGR Interrupt Enable D Disables interrupt requests by the TGFD bit when TGIED = b'0.	0
	2	TGIEC	TGR Interrupt Enable C Disables interrupt requests by the TGFC bit when TGIEC = b'0.	0
	1	TGIEB	TGR Interrupt Enable B Disables interrupt requests by the TGFB bit when TGIEB = b'0.	0
	0	TGIEA	TGR Interrupt Enable A Enables interrupt requests by the TGFA bit when TGIEA = b'1.	1
TSTR			Timer Start Register	H'C0
	7	CTS4	Count Start 4 TCNT_4 starts counting when CTS4 = b'1.	1
	6	CTS3	Count Start 3 TCNT_3 starts counting when CTS3 = b'1.	1
	5	—	Reserved	0
	4	—		0
	3	—		0
	2	CTS2	Count Start 2 TCNT_2 stops counting when CTS2 = b'0.	0
	1	CTS1	Count Start 1 TCNT_1 stops counting when CTS1 = b'0.	0
	0	CTS0	Count Start 0 TCNT_0 stops counting when CTS0 = b'0.	0

4.3 Arguments

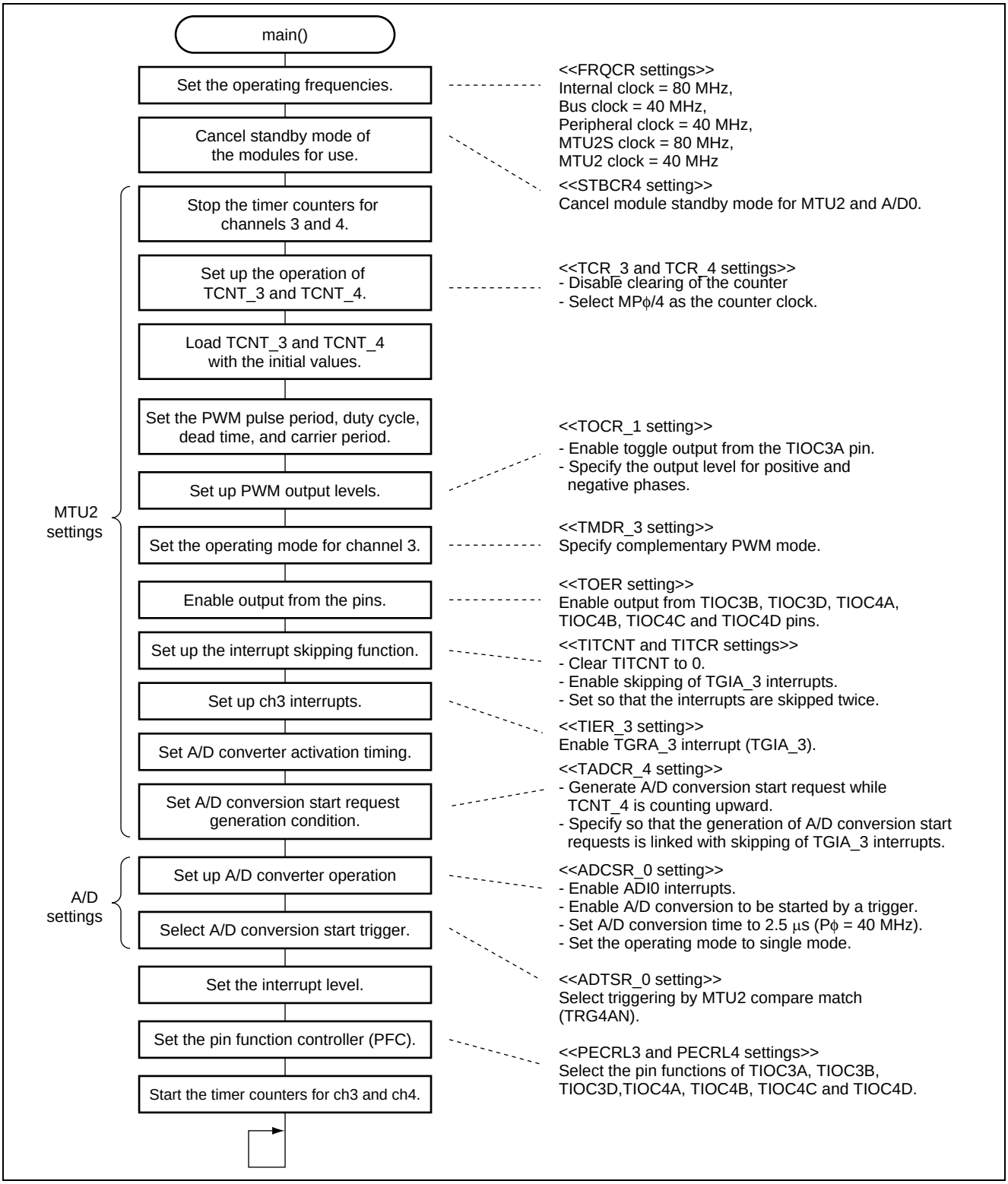
Table 4 describes the arguments used in this sample task.

Table 4 Description of Arguments

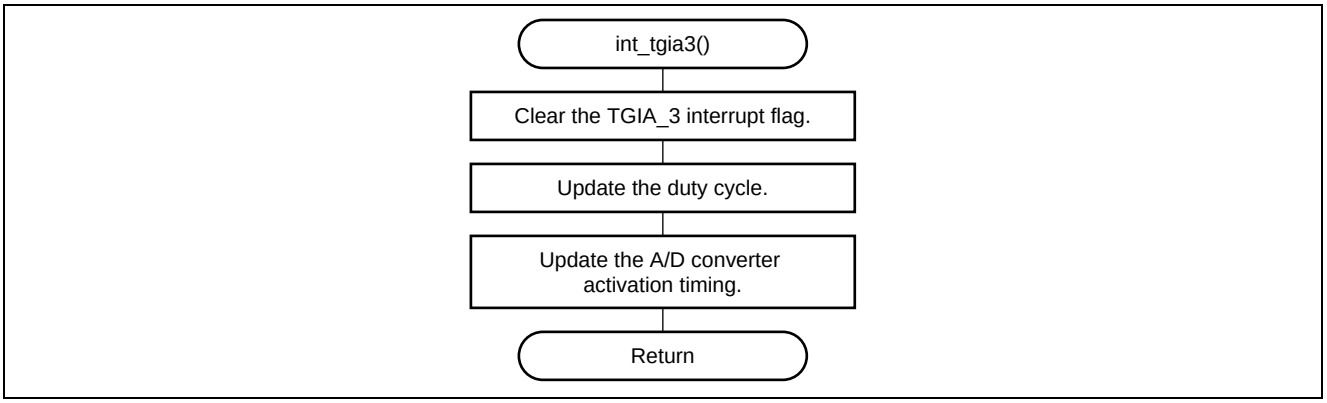
Label	Description	Used in
Pul_duty3d	Duty cycle of the PWM waveforms output from the TIOC3D pin (set in TGRD_3)	Main routine, TGRA_3 compare-match interrupt routine
Pul_duty4c	Duty cycle of the PWM waveforms output from the TIOC4C pin (set in TGRC_4)	
Pul_duty4d	Duty cycle of the PWM waveforms output from the TIOC4D pin (set in TGRD_4)	
Ad_start	A/D conversion start timing (set in TADCOBRA_4)	
Dead_time	Dead time (set in TDDR)	Main routine
C_cycle	PWM carrier period / 2 (set in TCBR)	
Pul_cycle	Pulse period / 2 + dead time (set in TGRC_3)	
Ad_data	Storage of A/D conversion results	A/D conversion end interrupt routine

5. Flowchart

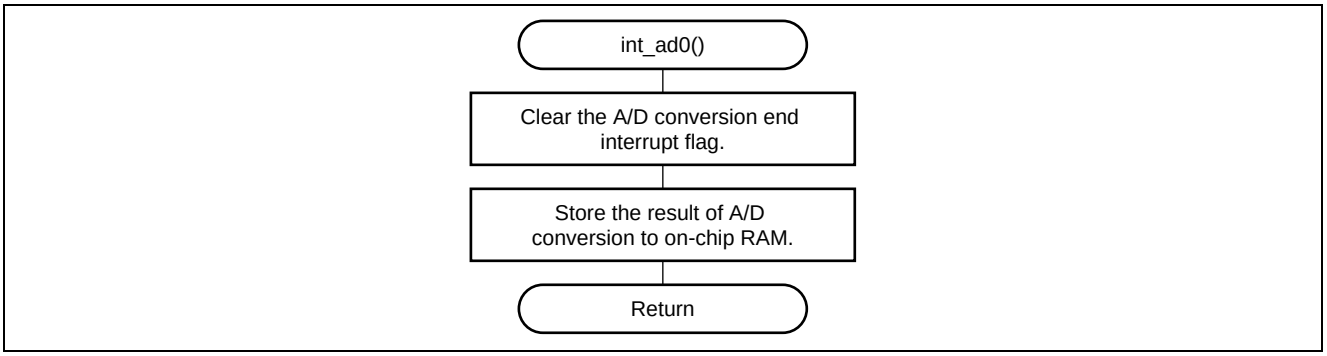
5.1 Main Routine



5.2 TGRA_0 Compare Match Interrupt Routine



5.3 A/D Conversion End Interrupt Routine



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1.00	Mar.04.05	—	First edition issued

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