R32C/100 Series

Serial Interface Operation When Receiving Data in Synchronous Serial Interface Mode

R01AN0178EJ0100
Rev.1.00
Nov. 26, 2010

1. Abstract

This document describes a method for receiving data from an external device synchronized with the internal clock using synchronous serial interface mode.

2. Introduction

The application example described in this document applies to the following microcomputers (MCUs):

MCUs: R32C/116 Group, R32C/117 Group, and R32C/118 Group

This application note can be used with other R32C/100 Series MCUs which have the same special function registers (SFRs) as the above groups. Check the manuals for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Application Example

This document describes the setting procedure for receiving data using synchronous serial interface mode (UART3). Table 3.1 and Table 3.2 list the Clock Frequency Settings and Setting Conditions for Data Reception Using Synchronous Serial Interface Mode, respectively.

Table 3.1 Clock Frequency Settings

Clock	Frequency
Main clock	16 MHz
PLL clock	100 MHz
Base clock	50 MHz
CPU clock	50 MHz
Peripheral bus clock	25 MHz
Peripheral function clock source	25 MHz

Table 3.2 Setting Conditions for Data Reception Using Synchronous Serial Interface Mode

Item	Setting Condition
Character length	8-bit
Transmit/receive clock	Internal
Transmit control	CTS
Bit order	LSB first
Continuous receive mode	Not used
CLK polarity	Output transmit data on the falling edge of the transmit/receive clock and input receive data on the rising edge
TXD/RXD I/O polarity switch bit	Non inverted
Bit rate	500 kbps (1)

Note:

1. The bit rate is calculated by the formula below.
   fx: Count source for transmit/receive clock (f1, f8, and f2n)
   m: Setting value (00h to FFh) in the UiBRG register (i = 0 to 6)

   Bit rate: $\frac{fx}{2(m+1)}$

When data is received from an external device, the transmit/receive clock is output from the MCU. To output the transmit/receive clock, set the port direction bit and the function select register for the port corresponding to the CLK pin.
Table 3.3 lists the CLK Pin, Port Direction Bits, and Function Select Register Settings.

Table 3.3 CLK Pin, Port Direction Bits, and Function Select Register Settings

CLK Pin	Port	Port Direction Bit	Setting Value	Function Select Register	Setting Value
CLK0	P6_1	PD6_1	1	P6_1S	03h
CLK1	P6_5	PD6_5	1	P6_5S	03h
CLK2	P7_2	PD7_2	1	P7_2S	03h
CLK3	P4_1	PD4_1	1	P4_1S	03h
CLK4	P9_5	PD9_5 (1)	1	P9_5S (1)	03h
CLK5	P7_7	PD7_7	1	P7_7S	03h
CLK6	P4_5	PD4_5	1	P4_5S	03h

Note:
1. The instruction to set these registers should be written immediately after the instruction to set the PRC2 bit to 1 (write enabled). Any interrupt or DMA transfer should not be generated between these two instructions.

3.1 Data Reception In Synchronous Serial Interface Mode

(1) In the U3C1 register, set the TE bit to 1 (transmission enabled) and set the RE bit to 1 (reception enabled).
(2) When dummy data is set in the U3TB register, the MCU switches to wait status.
(3) When the input signal to the $\overline{\text{CTS3}}$ pin becomes low, the transmit/receive clock is output. (1) The MCU receives the first bit of the RXD3 pin synchronized with the initial rising edge of transmit/receive clock. Then, data from the second bit on is received synchronized with the rising edge of transmit/receive clock.
(4) When 1-byte data accumulates in the UART3 receive register, the value in the UART3 receive register is transferred to the U3RB register. Simultaneously, the RI bit in the U3C1 register becomes 1 (data held in the U3RB register), indicating that data reception is completed. Also, the IR bit in the S3RIC register becomes 1 (interrupt requested).
(5) When the lower byte in the U3RB register is read, the RI bit becomes 0 (no data held in the U3RB register).

Note:
1. The input signal to the $\overline{\text{CTS3}}$ pin is controlled by the transmit device.

Figure 3.1 and Figure 3.2 show the Connection Example and Receive Operation, respectively.

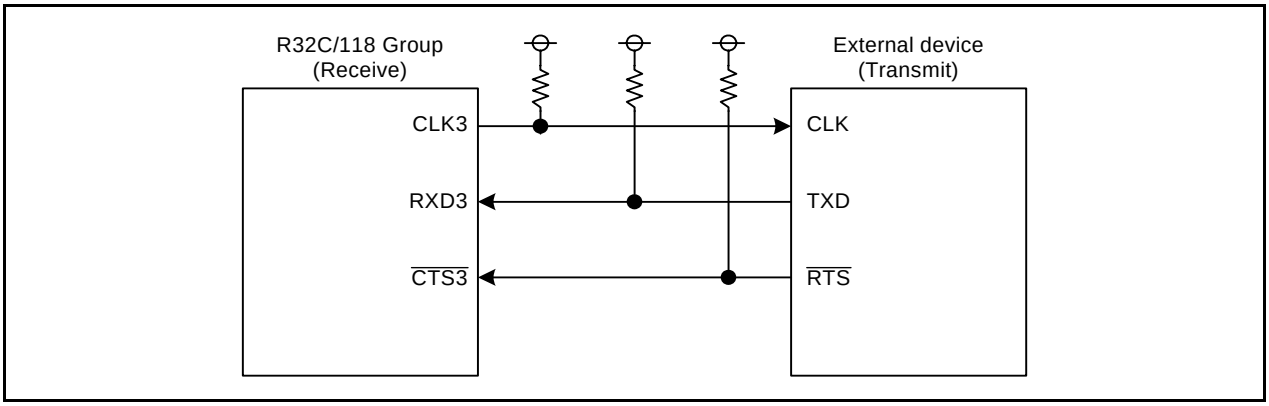
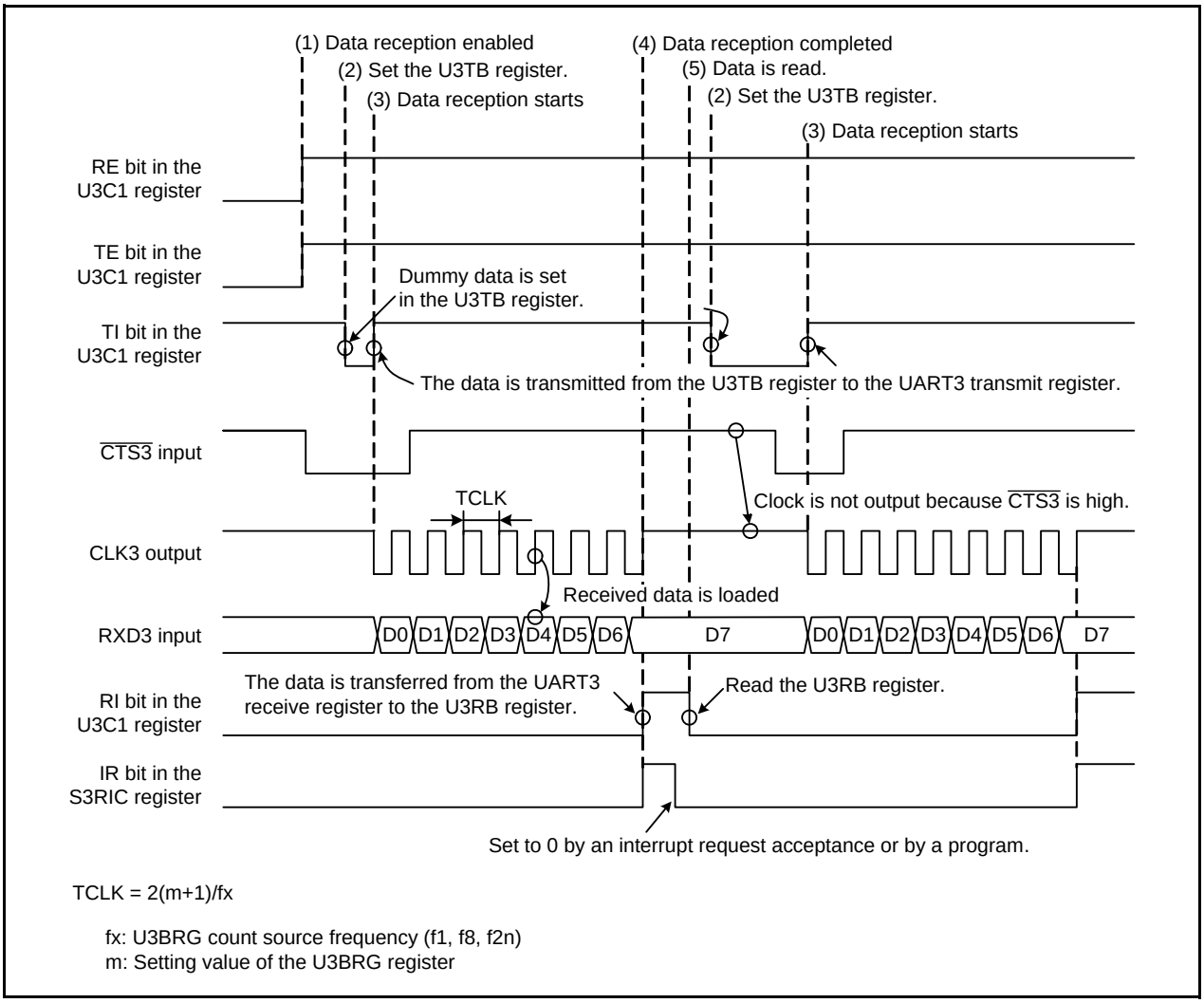


Figure 3.1 Connection Example



TCLK = 2(m+1)/fx

fx: U3BRG count source frequency (f1, f8, f2n)
m: Setting value of the U3BRG register

Figure 3.2 Receive Operation

3.2 Settings

This section describes the setting procedures and values for “3.1 Data Reception In Synchronous Serial Interface Mode”. Refer to the hardware user's manual for details of each register.
Figure 3.3 and Figure 3.4 show the Main Function Flowchart and UART3 Initialization Flowchart, respectively.

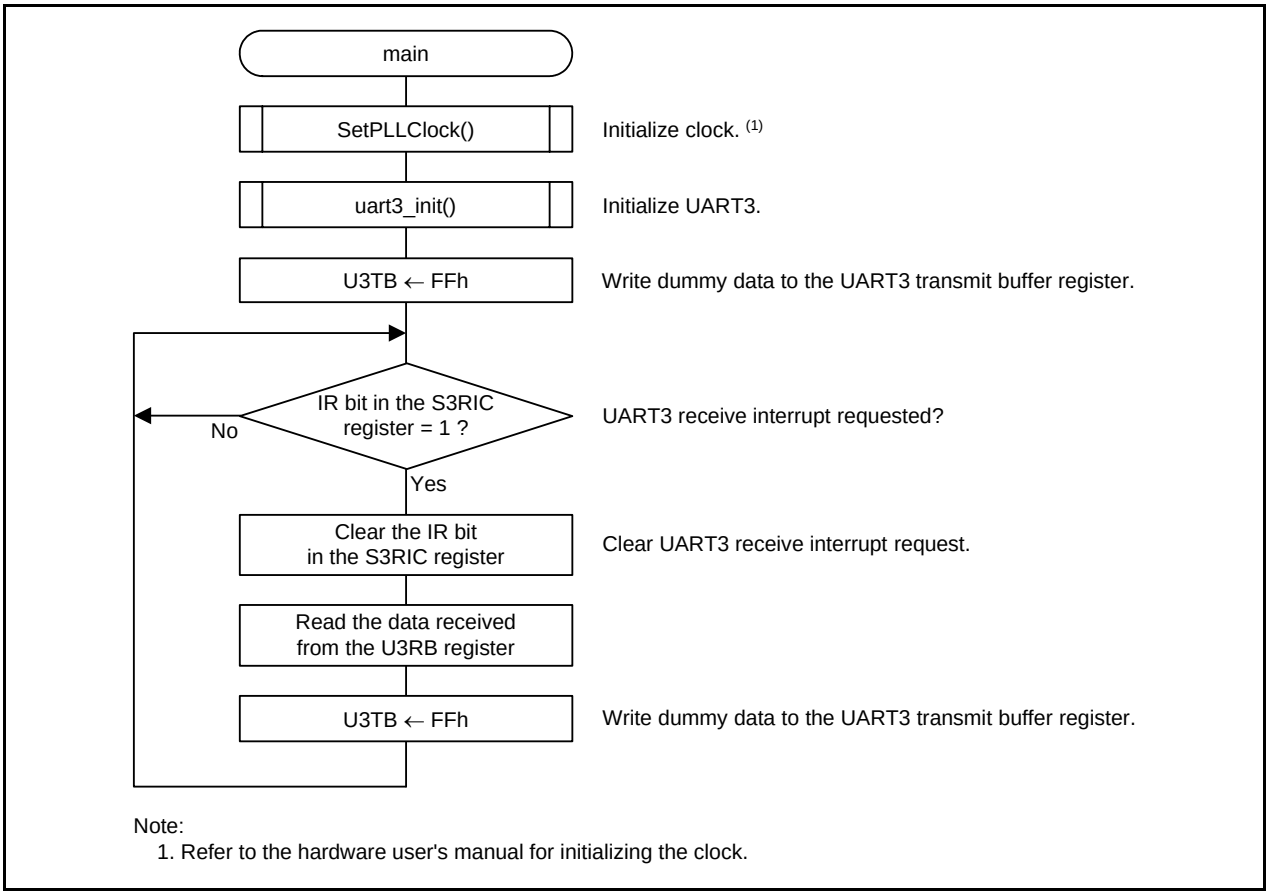


Figure 3.3 Main Function Flowchart

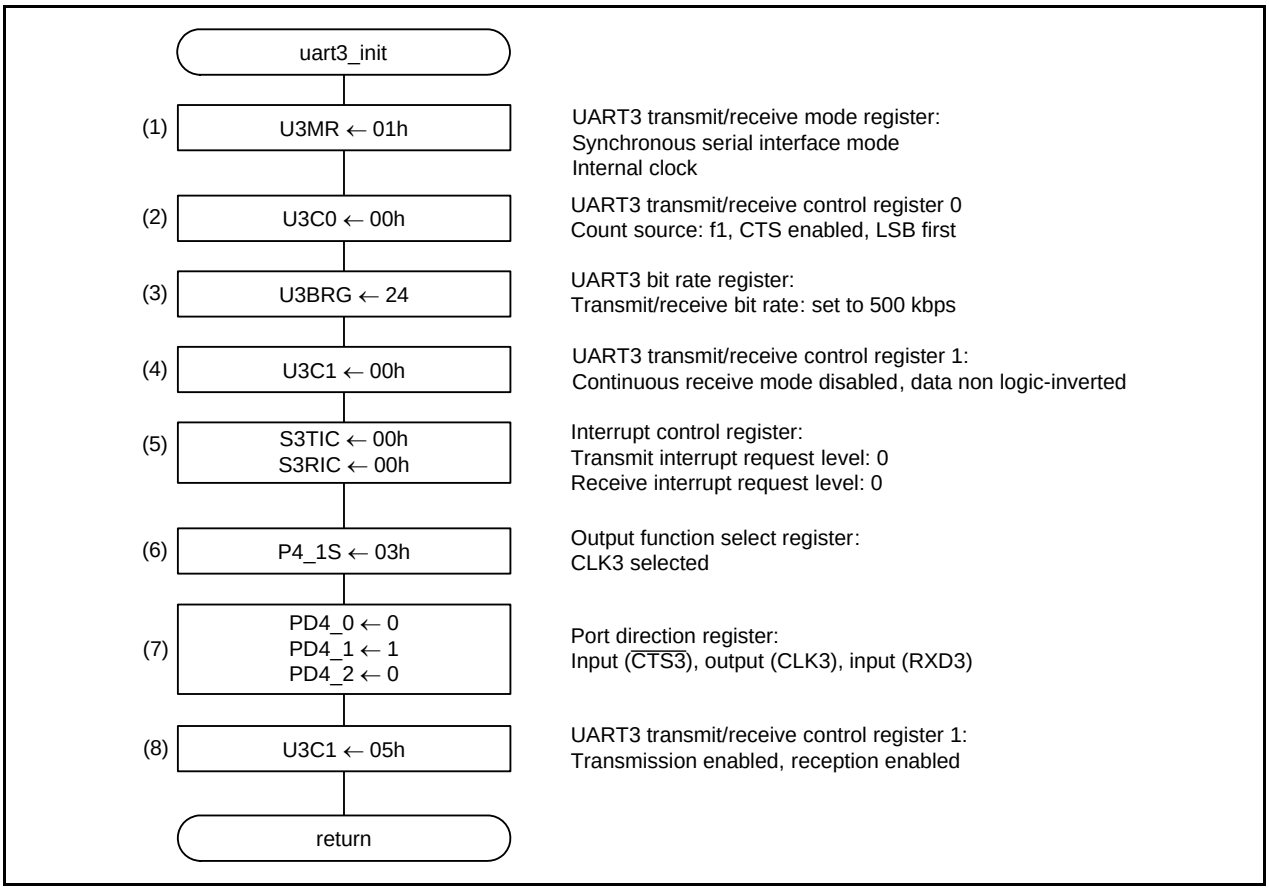


Figure 3.4 UART3 Initialization Flowchart

4. Sample Program

A sample program can be downloaded from the Renesas Electronics website.

5. Reference Documents

User's Manuals
R32C/116 Group User's Manual: Hardware Rev.1.10
R32C/117 Group User's Manual: Hardware Rev.1.10
R32C/118 Group User's Manual: Hardware Rev.1.10
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual
R32C/100 Series C Compiler Package V.1.02 C Compiler User's Manual Rev.2.00
The latest version can be downloaded from the Renesas Electronics website.

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REVISION HISTORY	R32C/100 Series Serial Interface Operation When Receiving Data in Synchronous Serial Interface Mode

Rev.	Date	Description	
		Page	Summary
1.00	Nov. 26, 2010	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
7F, No. 363 Fu Shing North Road Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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