

RZ/T1 Group

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EoE Web server function edition

Introduction

This document explains a sample program for adding Web server function using EoE service in the EtherCAT[®] Slave Stack Code environment provided by EtherCAT Technology Group of RZ/T1(with R-IN engine)

Target Device

RZ/T1(with R-IN engine)

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1. Overview

This document explains a sample program for adding Web server function by EoE (Ethernet over EtherCAT) service to EtherCAT slave device.

EtherCAT communication program is created with the EtherCAT Slave Stack Code generation tool (SSC Tool) provided by EtherCAT Technology Group. This sample program provides the SSC Tool project file for using the EoE service, the ESI file, and the patch file for making corrections for this sample program.

Ethernet communication program for EoE uses the Renesas Electronics TCP/IP protocol official version stack (TCP/IP stack) for RZ/T1, and this provides a virtual Ethernet driver for the connection between the EoE service and the TCP/IP stack.

EtherCAT communication program and the Ethernet communication program operate with the Cortex[®]-M3 core.

Cortex[®]-R4 core receives the flashing interval time of the LED from the Ethernet communication program of the Cortex-M3 core and controls the LED at its flashing interval, and the communication between the CPU uses shared memory driver.

Table 1.1. Requirements

Item	Description
Board	RZ/T1 Evaluation Board RTK7910022C00000BR
CPU	RZ/T1 (with R-IN engine) R7S910017
IDE	IAR Systems Embedded Workbench [®] for Arm Version 8.20.2 or later
Emulator	IAR Systems I-jet
SSC Tool	EtherCAT Technology Group Beckhoff Automation Slave Stack Code Tool Version 5.12
Software PLC	Beckhoff Automation TwinCAT [®] 3
TCP/IP stack	TCP / IP stack for the Renesas Electronics RZ/T1

The main functions of the TCP/IP stack for RZ/T1 are shown below.

- Supports IPv4, ARP, ICMP, IGMPv2, UDP, TCP protocol
- DHCP client, DNS client, FTP server, HTTP server function available

For detailed specifications of the TCP/IP stack for RZ/T1, refer to the following user's manual.
RZ/T1 Group User's Manual TCP/IP Stack Edition (R01US01831JJxxxx)

2. Software description

2.1 Software structure

Figure 2.1 shows the software structure of the sample program. The sample program consists of the EtherCAT slave stack part and the TCP/IP stack part.

EoE enables Ethernet-based services and protocols to be used by encapsulating Ethernet communication frames in EtherCAT communication data. The fragmentation of the Ethernet communication frame during assembly and transmission of the segmented Ethernet communication frame at the time of reception due to the encapsulation of the communication data is implemented as the EoE service of the SSC. The virtual Ethernet driver replaces the Ethernet driver on the physical layer of the normal TCP/IP stack and is responsible for passing the Ethernet communication frame between the TCP/IP protocol stack and the EoE service. The HTTP server, which is a network application, sends the contents of the slave to the HTTP client (web browser).

Cortex-R4 core sample program consists of LED flashing process, and the blinking time can change from the web browser, with the inter-CPU communication, the changed blinking time is transmitted from Cortex-M3's HTTP server application to Cortex-R4, and the LED blinking process changes the blinking interval according to the received blinking time.

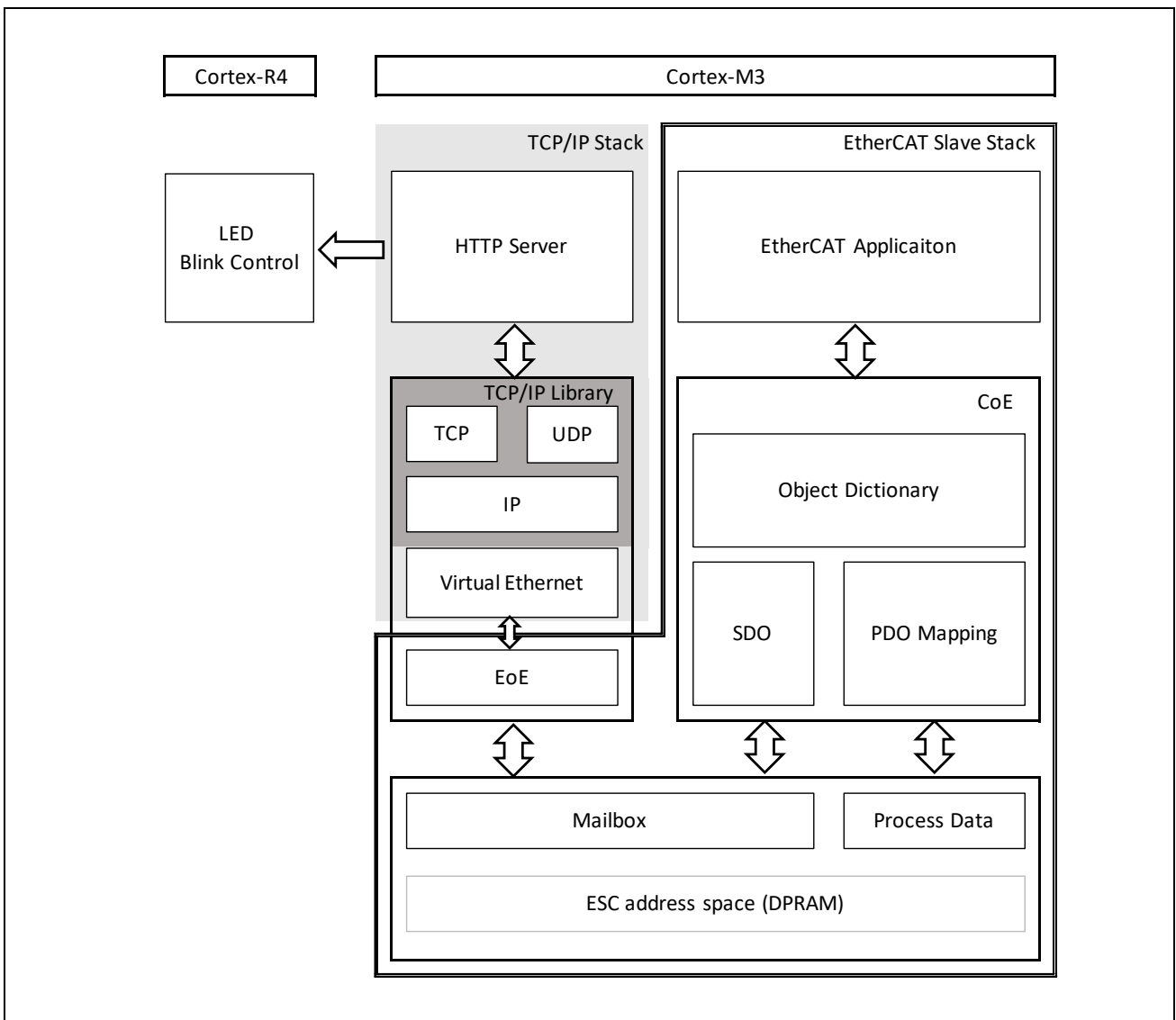


Figure 2.1: Software configuration diagram

2.2 Directory structure

(1) Cortex-M3 sample program

Table 2.1 describes the directories under workspace/iccarm/Cortex-M3/Device/Renesas/RIN_Engine

Table 2.1. Directory structure of Cortex-M3 sample program

Item	Description
/Include	Include file store directory
/Include/ecat_unet3	Virtual Ethernet driver header file store directory
/Library	Library store directory
/Library/IAR	OS Library, TCP/IP Library store directory
/Source/Driver	Peripherals driver source file store directory
/Source/Driver/ecat_unet3	Virtual Ethernet driver source file store directory
/Source/Middleware	Middleware source file store directory
/Source/Middleware/uNet3	Ethernet application protocol store directory such as HTTP
/Source/Project/EtherCAT_EoE	EtherCAT EoE sample program store directory
/Source/Project/EtherCAT_EoE/uNet3_sample	Network application store directory
/Source/Templates	Startup file store directory

(2) Cortex-R4 sample program

Table 2.2 describes the directories under workspace/iccarm/Cortex-R4/RZ_T1_shm

Table 2.2. Directory structure of Cortex-R4 sample program

Item	Description
/Include	Include file store directory
/src/common	Boot related source file storage directory
/src/drv	Peripherals driver source file store directory
/src/sample	Sample program store directory

2.3 List of kernel objects

Table 2.3 describes the kernel objects used in the Cortex-M3 sample program. and the Cortex - R4 sample program does not use the OS.

Table 2.3. Cortex-M3 Sample program kernel object

Object	Object ID	Function
Task	ID_TASK_MAIN	Initialization processing, EtherCAT slave stack task
Task	ID_TASK_TCP_TIM	TCP / IP stack time management task
Task	ID_TASK_ETH_SND	Virtual Ethernet driver transmission task
Task	ID_TASK_HTTPS	HTTP server task
Task	ID_TASK_TCP_APPL	Network application task
Semaphore	ID_SEM_TCP	Protocol stack resource control semaphore
Semaphore	ID_SEM_INTDMA	Virtual Ethernet driver semaphore
Mailbox	ID_MBX_ETH_SND	Virtual Ethernet driver mailbox
Mailbox	ID_MBX_MEMPOL	Memory management mailbox

3. Procedure for creating a sample program

Sample program does not include the source file of the EtherCAT slave stack.

EtherCAT Slave Stack Code Tool (SSC tool) is required to create the source file of the EtherCAT slave stack

Note) Use Ver.5.12 SSC tool.

- (1) Double-click the SSC tool project file of the sample program and start the SSC tool.

workspace/iccarm/Cortex-

M3/Device/Renesas/RIN_Engine/Source/Project_Dual/EtherCAT_EoE/RenasasSDK/RZT1 EtherCAT EoE.esp

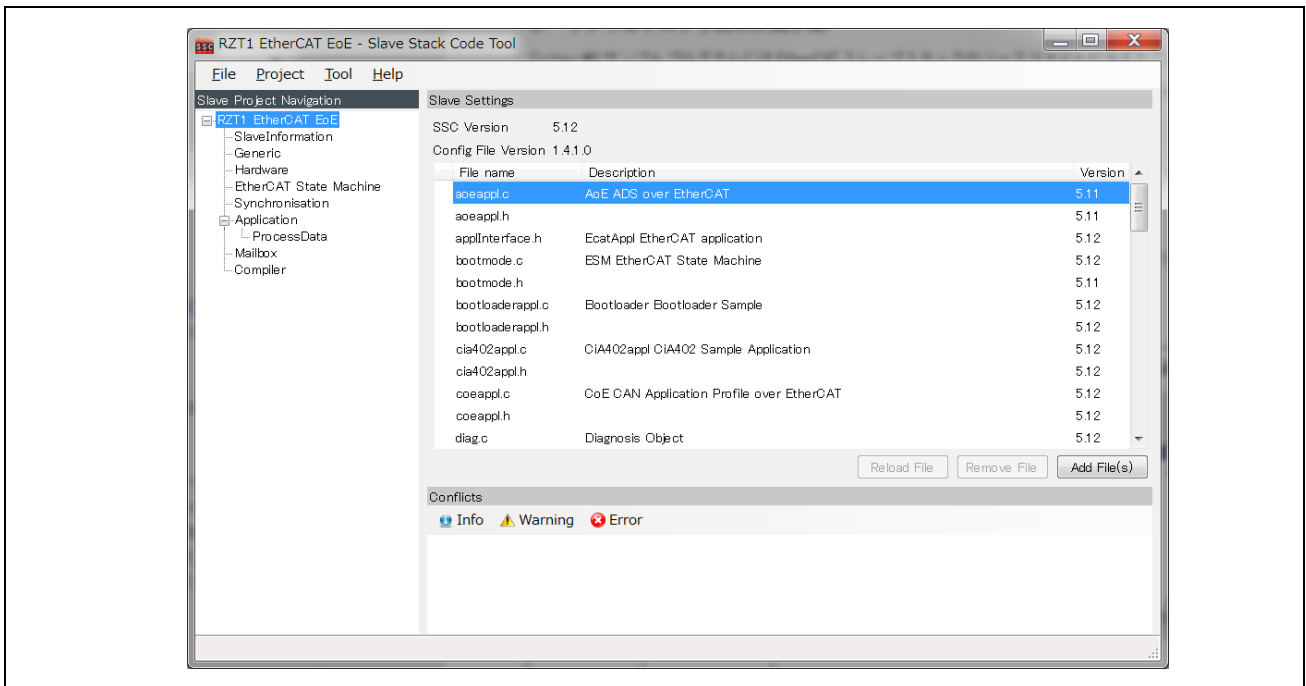


Figure 3.1: SSC Tool startup

- (2) Select [Project] ⇒ [Create new Slave Files]
- (3) Push Start to generate the EtherCAT Slave Stack Code
- (4) Generation is completed when [New files created successfully] is displayed.

workspace/iccarm/Cortex-

M3/Device/Renesas/RIN_Engine/Source/Project_Dual/EtherCAT_EoE/RenasasSDK/Src

- (5) If patch command is not installed GNU Patch Ver 2.5.9 or later is required.

Download the patch command (Ver 2.5.9) from the following website and store "patch.exe" in the folder passed the directory path.

<http://gnuwin32.sourceforge.net/packages/patch.htm>

(6) Applying patches,

Right-click on the apply_patch.bat file and select [Run as administrator] ⇒ [Yes].

Patch file contains fixes for RZ/T1 for SSC source files.

```
workspace/iccarm/Cortex-  
M3/Device/Renesas/RIN_Engine/Source/Project_Dual/EtherCAT_EoE/RenesasSDK/apply_patch.bat
```



```
--- Patching process start ---  
patching file Src/applInterface.h  
patching file Src/ecatappl.c  
patching file Src/ecateoe.c  
patching file Src/ecateoe.h  
patching file Src/mailbox.h  
--- Patching process end ---  
続行するには何かキーを押してください . . . ■
```

Figure 3.2: "Apply_patch.bat" execution screen

4. Build and debug the sample program

In this chapter, explain the procedure to build without executing debugging by building a sample program.

Refer to the following startup manual for the procedure for debugging sample program.

RZ/T1 Group Development Tools Startup Manual

EtherCAT communication procedure (product with R-IN Engine) (R01AN3069JJ ****)

(1) Build the Cortex-M3 sample program

Double-click the IAR project file and start IAR Embedded Workbench for Arm

workspace/iccarm/Cortex-M3/Device/Renesas/RIN_Engine/Source/Project_Dual/EtherCAT_EoE/IAR/main.eww

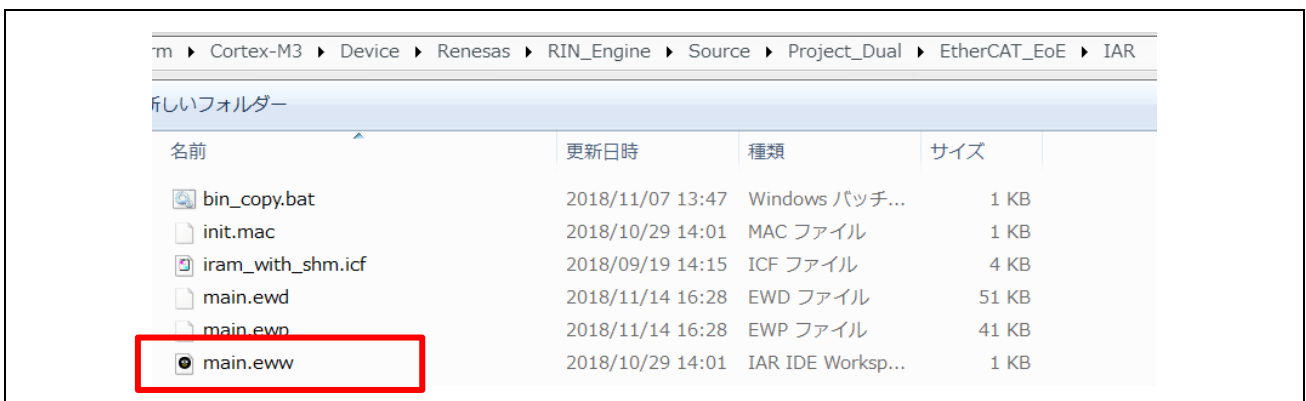


Figure 4.1: Cortex-M3 IAR project · File directory screen

The build configuration included in the Cortex - M3 sample program is "RAM Debug" only.

[Project] → [Rebuild All], build the project. When the build is finished, the binary file "cm3_boot.bin" is created in the following directory.

workspace/iccarm/Cortex-M3/cm3_boot_binary

(2) Build the Cortex-R4 sample program

Double-click the IAR project file and start IAR Embedded Workbench for Arm

workspace/iccarm/Cortex-R4/RZ_T1_shm/RZ_T1_shm_boot.eww

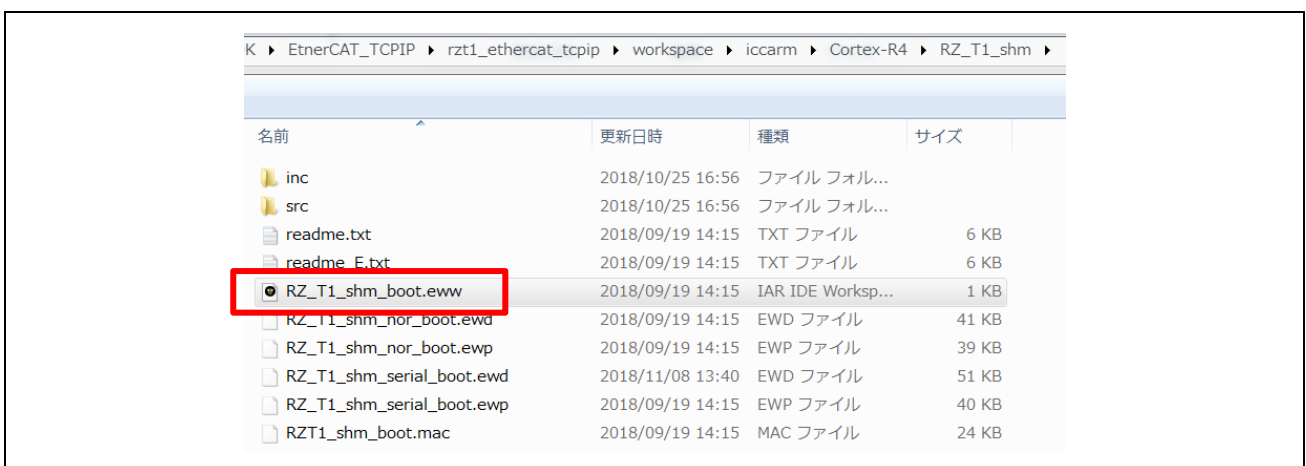


Figure 4.2: Cortex-R4 IAR project · File directory screen

Table 4.1 shows the build configuration included in the sample program.

Select the build configuration according to the operation mode of the evaluation board.

Table 4.1. Build configuration of sample program

Build configuration name	Program code download location
RZ_T1_shm_serial_boot - Debug	Serial flash ROM
RZ_T1_shm_nor_boot - Debug	Parallel flash ROM

[Project] → [Rebuild All], build the project.

(3) Start-up of the Cortex-R4 sample program

Write to flash memory with [Project] → [Download and debug] and clicking the [execute] button.

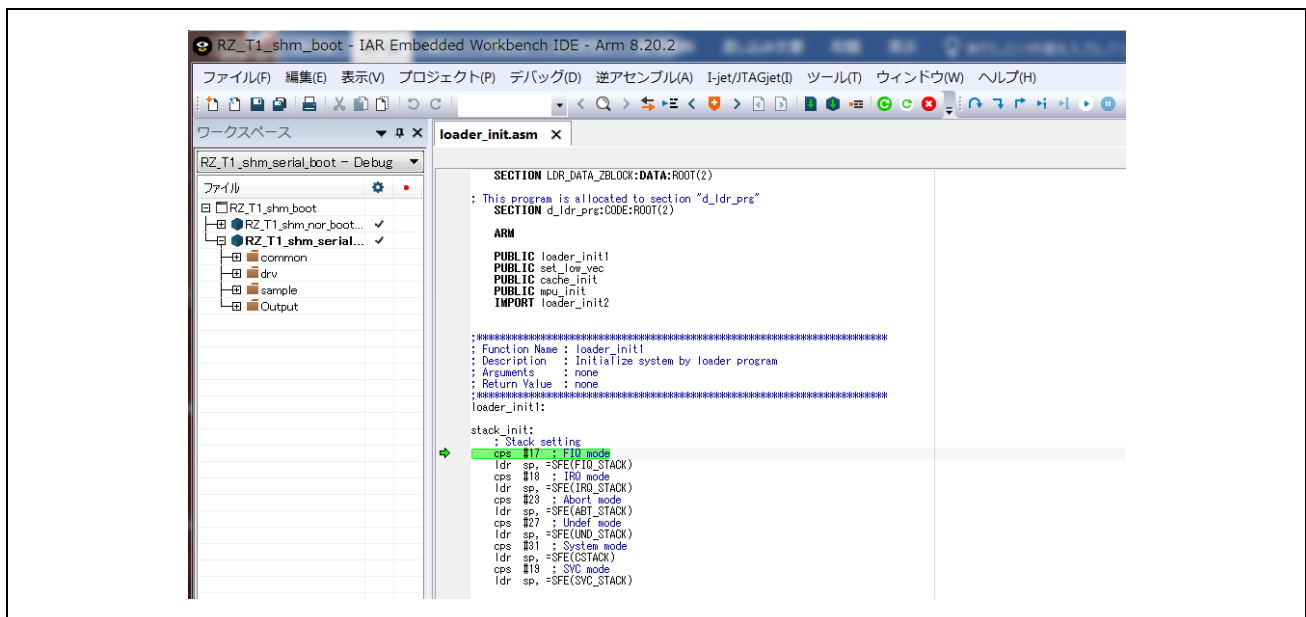


Figure 4.3: EWARM start screen

Program code of Cortex-M3 is linked as a binary image as part of the Cortex-R4 program, and it is copied to the extended internal RAM by the Cortex-R4 core after starting the program. After that, the Cortex-R4 core releases the reset of the Cortex-M3 core. and therefore, when start-up the Cortex-R4 sample program, program execution starts on both Cortex-M3 core and Cortex-R4 core.

5. Evaluation board setting

This section explains the board switch settings required for starting the debugger.

1. Boot mode setting

Selection of boot mode of the evaluation board is set by Dip switch for system setting (SW 4).

Boot mode selection should be set before connecting the DC adapter.

Table 5.1. Boot mode setting

SW4			Boot mode setting
3	2	1	
ON(Low)	ON(Low)	ON(Low)	Serial flash ROM Boot
ON(Low)	OFF(High)	ON(Low)	Parallel flash ROM Boot
other			Setting prohibited

2. LAN cable connection

Connection of Ethernet cable of the EtherCAT master (PC), please use the EtherCAT1 side.

6. IP address setting

In order to operate the EoE sample program, it is necessary to set the IP address of the EtherCAT master and the EtherCAT slave as fixed IP addresses.

IP address of the EtherCAT slave is set in the network configuration file of the TCP/IP stack of the sample program

workspace/iccarm/Cortex-M3/Device/Renesas/RIN_Engine/Source/Project_Dual/EtherCAT_EoE
/uNet3_sample/net_cfg.c

Table 6.1. IP address setting

Setting items	EtherCAT Master	EtherCAT Slave
IPAddress	192.168.1.99 ^(※)	192.168.1.100
Sub-net mask	255.255.255.0	255.255.255.0
Default Gateway	Blank	192.168.1.99 ^(※)

(※) To set the IP address of the EtherCAT master to something other than [192.168.1.99], also set the fault gateway of the EtherCAT slave to the same address.

Figure 6.1 shows the network card settings of the PC used as an EtherCAT master.
Leave the default gateway and DNS server settings blank.

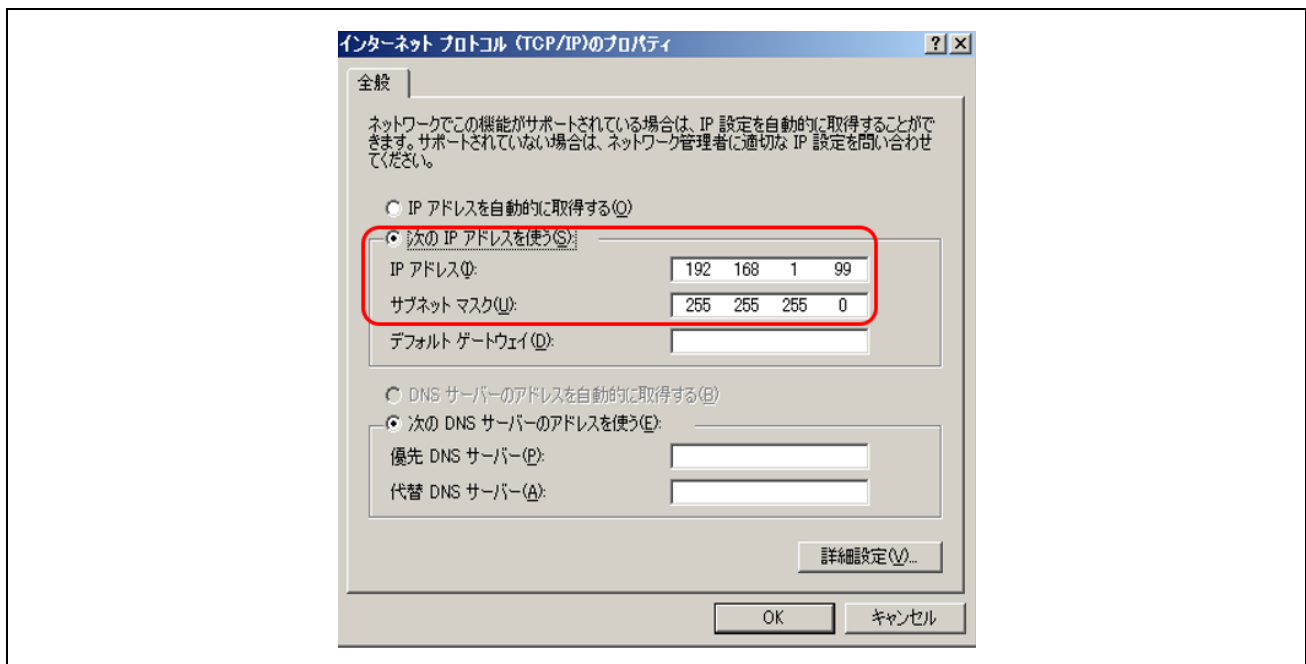


Figure 6.1: EWARM start screen

7. TwinCAT connection procedure

This section describes the procedure for operating the sample program using TwinCAT 3.

Build the source code of the sample program created earlier and start the program.

7.1 Copy ESI file

The ESI file is generated simultaneously when generating the EtherCAT slave stack code with the SSC tool

ESI file generated before launching TwinCAT to the predetermined place of TwinCAT, copy it to "/TwinCAT/3.x/Config/IO/EtherCAT".

- Copy source (SSC Tool generation ESI file)
workspace/iccarm/Cortex-M3/Device/Renesas/RIN_Engine/Source/Project_Dual/EtherCAT_EoE/RenesasSDK/RZT1 EtherCAT EoE.xml
- Copy destination (TwinCAT 3 installation folder)
/TwinCAT/3.x/Config/IO/EtherCAT

7.2 Connection with TwinCAT

Start up TwinCAT 3 in the following method.

From the start menu, select [Beckhoff] ⇒ [TwinCAT 3] ⇒ [TwinCAT XAE (VS 20 XX)]

After starting the program, create a new project of type TwinCAT XAE Project as [File] ⇒ [New] ⇒ [Project]. The following procedure is described below.

7.2.1 ESI file reload setting

Read the ESI file of the sample program added from TwinCAT.

Select [TwinCAT] ⇒ [EtherCAT Devices] ⇒ [Reload Device Descriptions].

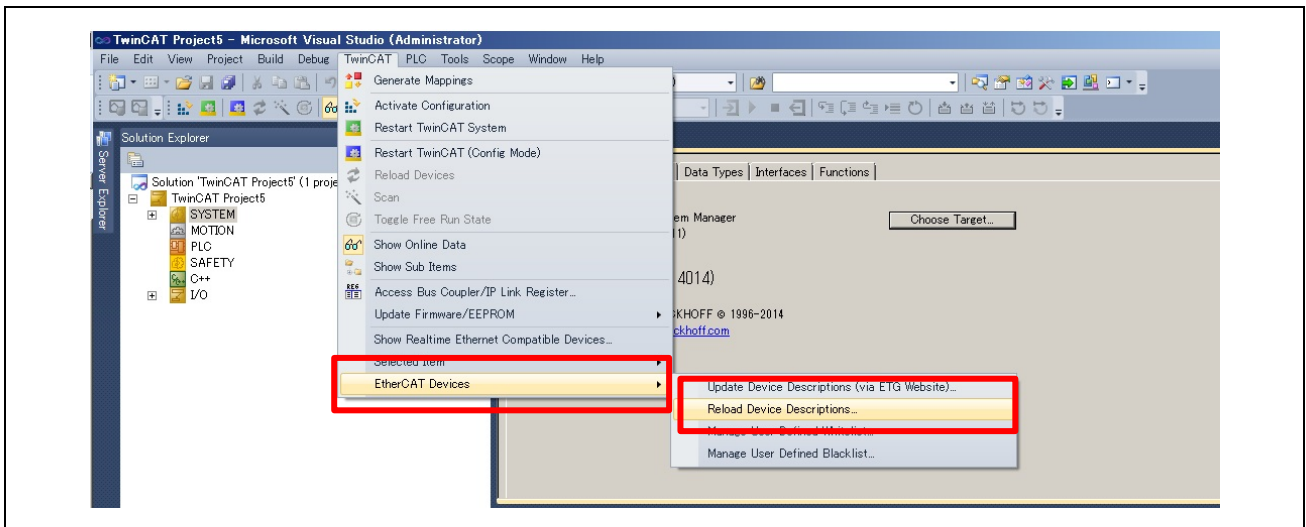


Figure 7.1: ESI file reload

7.2.2 Scanning I/O device

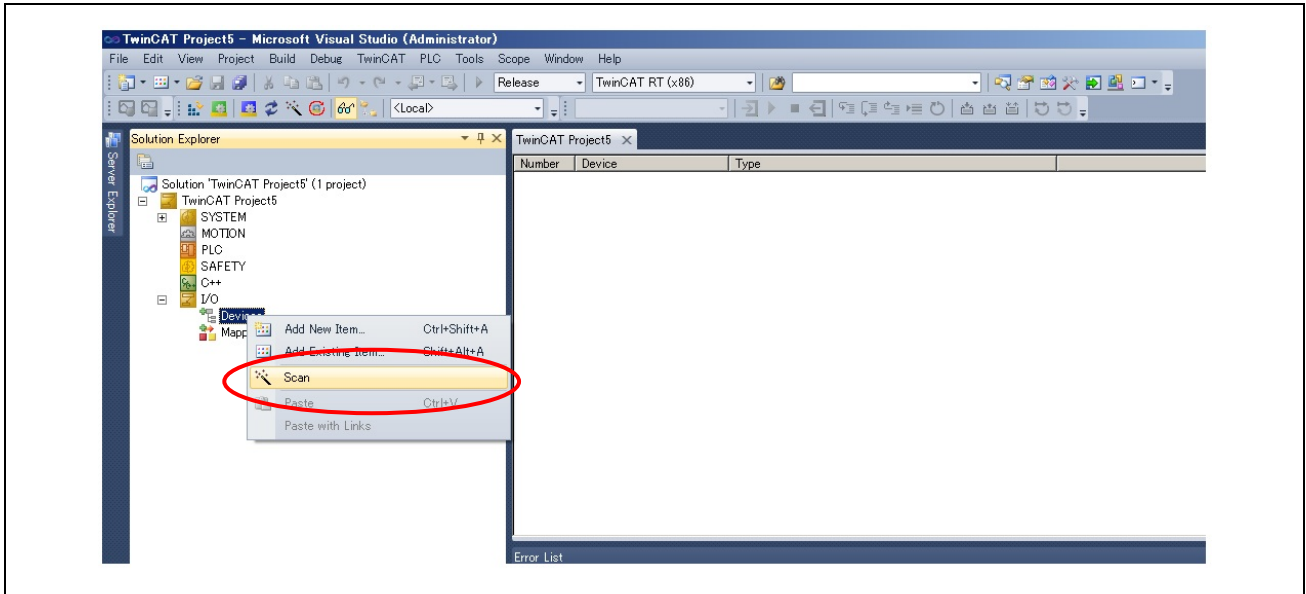


Figure 7.2: Scanning I/O device

Select the above [I / O Device] and right click to open another window. Select [Scan] in this separate window and execute it. For window settings displayed after Scan execution, please select according to Figure 7.3.

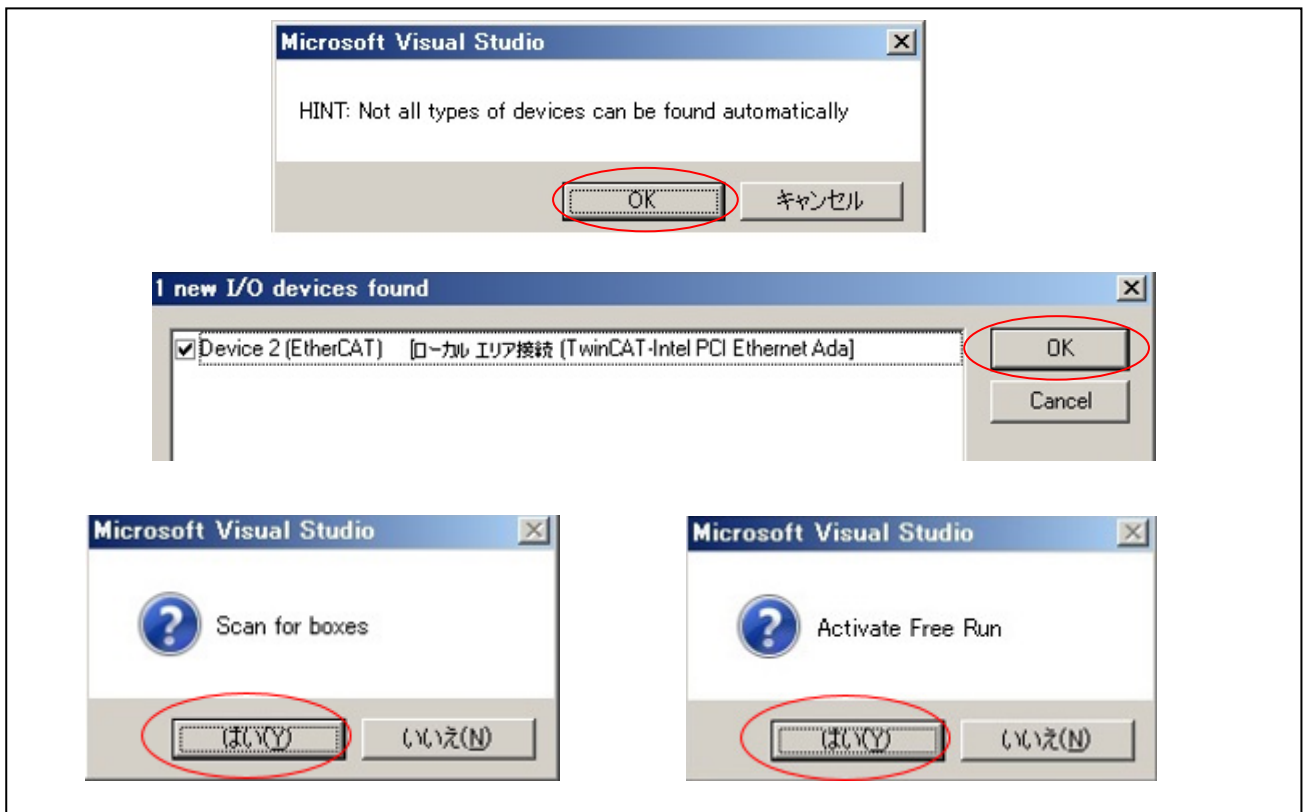


Figure 7.3: I/O Device Scan Settings

7.2.3 EEPROM data update

If data of another application is already written, please rewrite the EEPROM.
The procedure for rewriting the EEPROM is described below.

EEPROM is blank for the first time when purchasing the evaluation board, be sure to rewrite it. In case of blank, [Box 1 (PFFFFFFF RFFFFFFF)] is displayed.

- (1) Double click on [Box 1], the panel as shown in Figure 7.4 will be displayed.
- (2) Select [EtherCAT] tab
- (3) Click the [Advanced Setting] button.
- (4) Select [ESC Access] ⇒ [EEPROM] ⇒ [Hex Editor]
- (5) Select [Download from list].
- (6) Select [Available EEPROM Description].
[Renesas Electronics Corp.] ⇒ [RZ/T1-R Slaves]⇒[RZ/T1 EtherCAT EoE]
- (7) Click [OK] button.
Restart RZ/T1 after rewriting (power cycle or reset)
- (8) Run [TwinCAT] ⇒ [Restart TwinCAT System] please

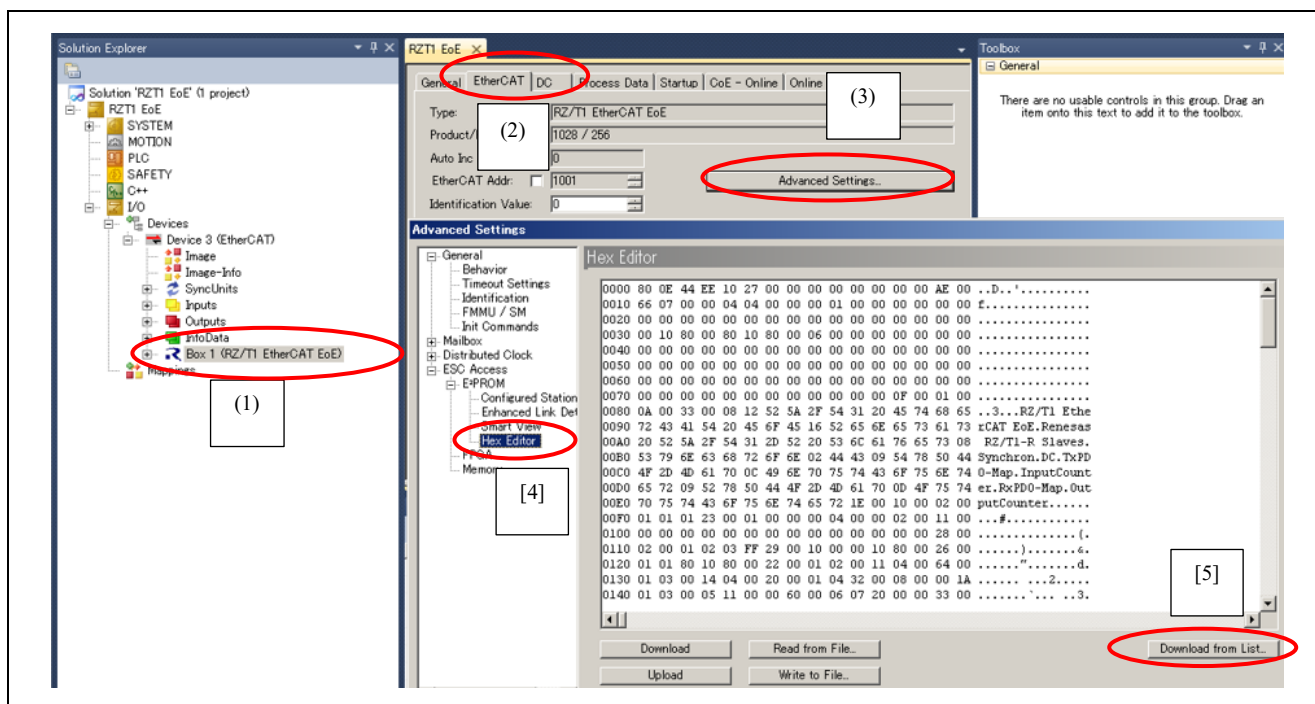


Figure 7.4: EEPROM rewriting procedure 1

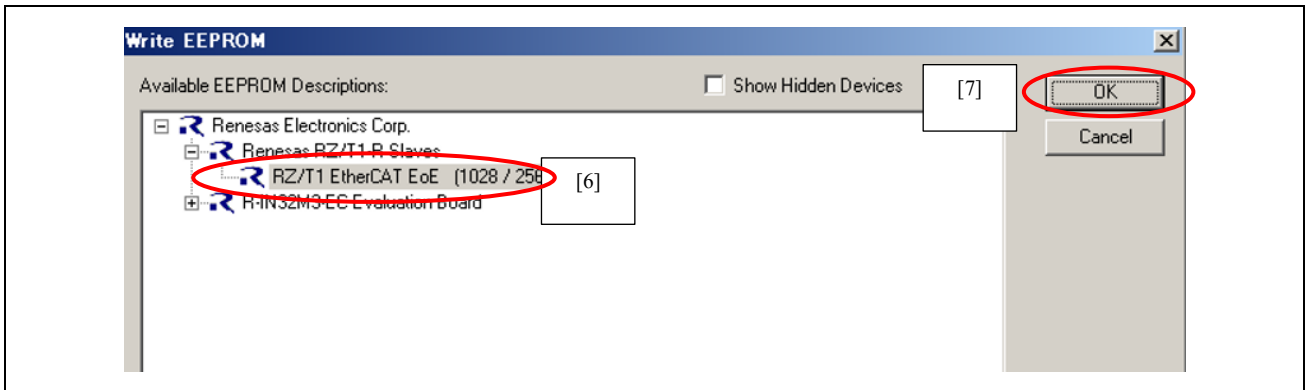


Figure 7.5: EEPROM rewriting procedure 2

7.2.4 Slave EoE settings

- (1) Double-click [Box 1] to display the panel.
- (2) Select [EtherCAT] tab
- (3) Click the [Advanced Setting] button.
- (4) Select [Mail box] ⇒ [EoE]
- (5) Check [IP Address].
- (6) IP Address: [192.168.1.100]
 Subnet Mask: [255.255.255.0]
 Default Gateway: [192.168.1.99]
 input the above
- (7) Click [OK] button.
- (8) Click the [Restart TwinCAT (Config Mode)] button to activate the EoE setting.

If reset the slave, the EoE setting will return to the initial state (invalid), please save the TwinCAT project file.

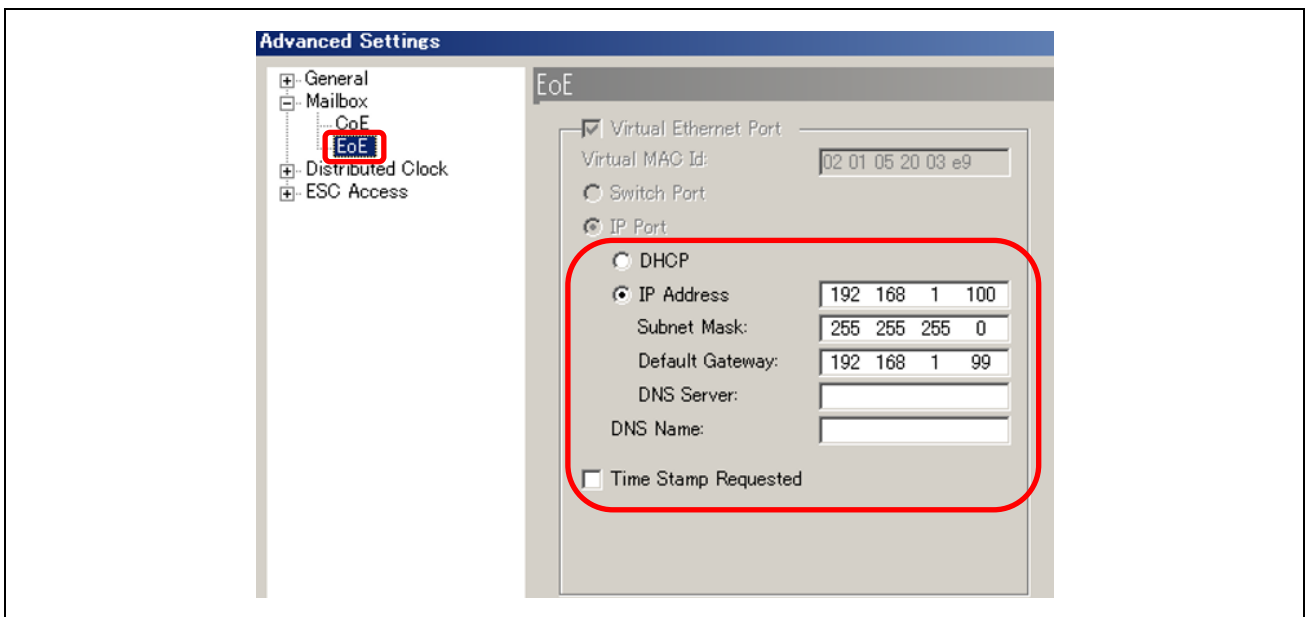


Figure 7.6: Slave EoE setting

8. Confirmation of sample program operation

8.1 EtherCAT

Input Counter is assigned to TxPDO, Output Counter is assigned to RxPDO, Input Counter can confirm the value, Output Counter can change its value.

Output Counter is 0, the value of Input Counter is continuously incremented.

Value other than 0 is set for Output Counter, the Input Counter becomes the value of Output Counter+1.

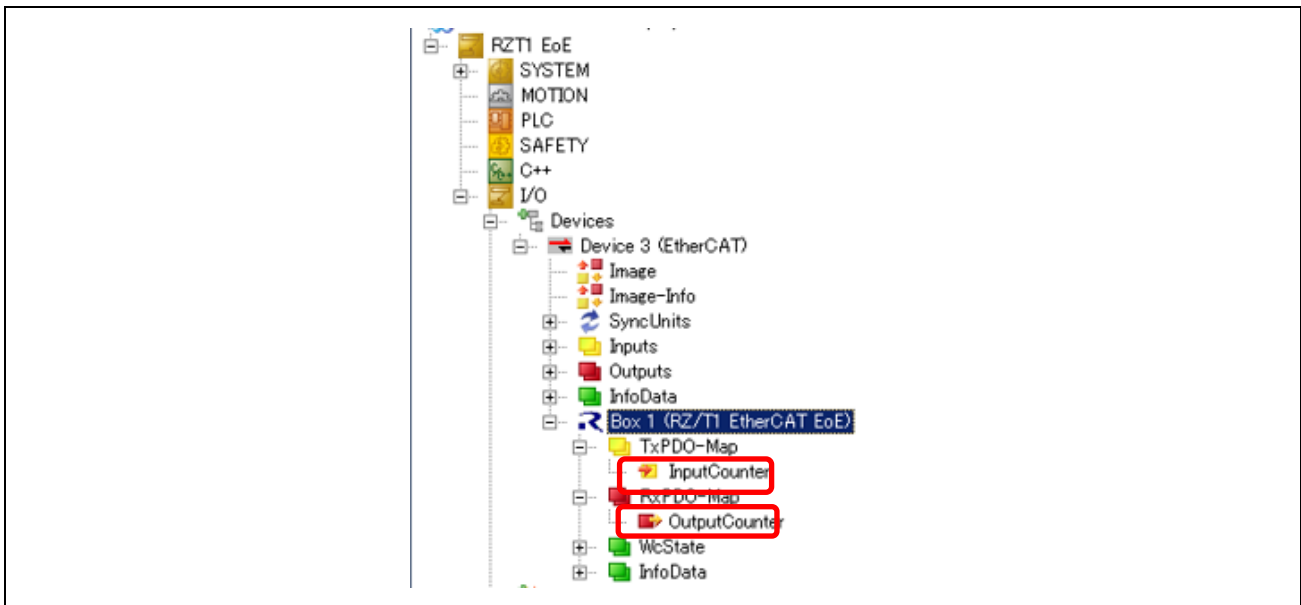


Figure 8.1: TxPDO and RxPDO

8.2 Web Server

- (1) Start the Web browser on the PC running the TwinCAT
- (2) Set URL field to http://192.168.1.100

After waiting a while, you can check the web page sent from RZ/T1 via EoE as shown in Figure 8.2.

Table 8.1 shows the items that can be checked on the Web server and their descriptions.

Table 8.1. Web server operation check item

items	Item Description	Behavior
LED Blinker Interval	Possible to change the blinking interval of LED0 to LED3 of the evaluation board.	After setting the numerical value, pressing the "LED" button will set the blinking interval time to the set value × 100 ms
Ping Request	Request a Ping response for the set IP address	Set the PC's IP address (192.168.1.99) and press the "PING" button. If there is a reply of Ping response, a success message will be displayed
Network Time Resolver	It does not work with the connection method with the EtherCAT master described in this application note.	
EtherCAT	Acquire the state of EtherCAT port 0 or 1.	Enter "0" or "1" and press "GET" button. The state of the port when pressed is displayed as shown in figure 8.3

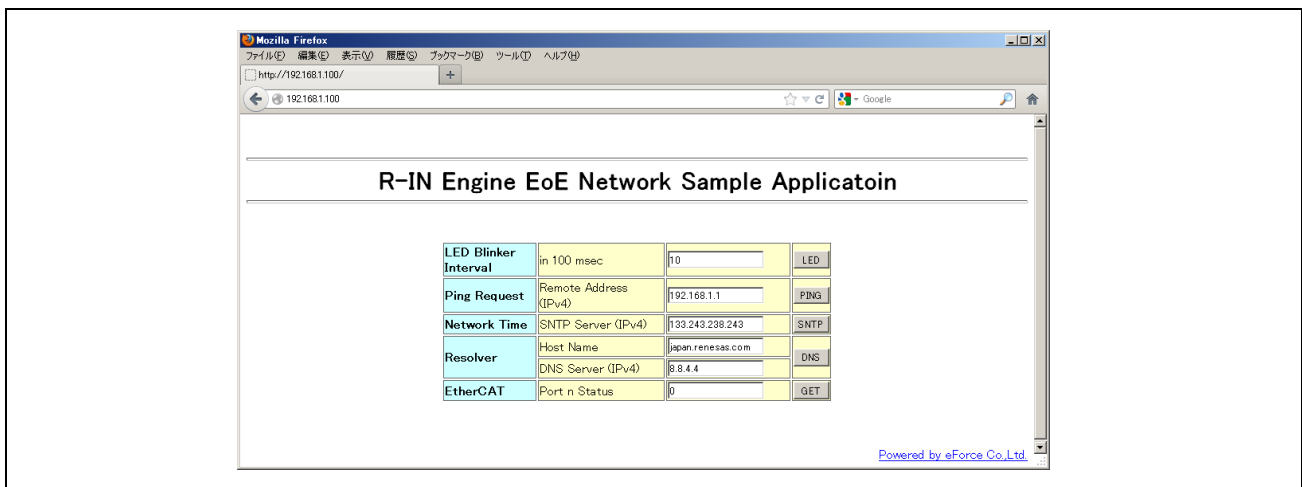


Figure 8.2: Web server screen

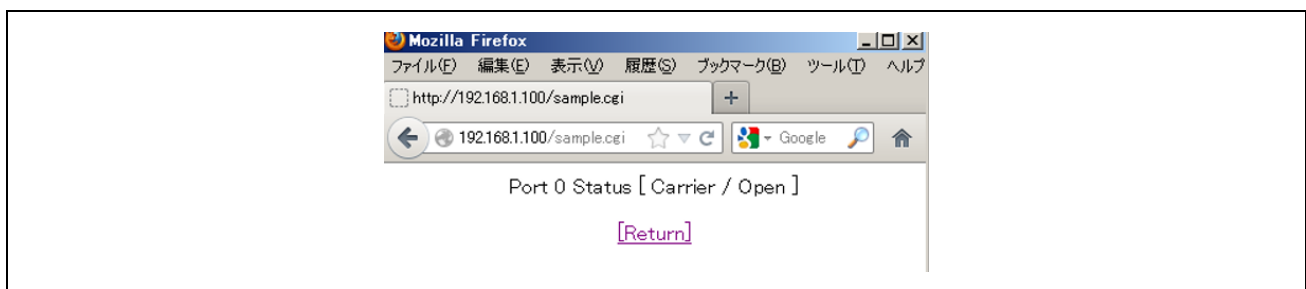


Figure 8.3: Web server EtherCAT port status acquisition result

9. Reference Documents

- Document / Application Notes / Sample Code

RZ / T1 group initial setting

(Please download the latest version from the Renesas Electronics website.)

RZ / T1 Group User's Manual: Hardware

(Please download the latest version from the Renesas Electronics website.)

RZ / T1 Evaluation Board RTK7910022C00000BR User's Manual

(Please download the latest version from the Renesas Electronics website.)

RZ / T1 group development tool start-up manual EtherCAT communication procedure (with R-IN Engine)

(Please download the latest version from the Renesas Electronics website.)

RZ / T1 Group User's Manual TCP / IP Stack

(Please download the latest version from the Renesas Electronics website.)

- Technical Update / Technical News

(Please download the latest version from the Renesas Electronics website.)

- Development environment

For IAR Integrated Development Environment (IAR Embedded Workbench for Arm), please download from the IAR website.

For software PLC (TwinCAT 3), please download it from Beckhoff Automation website.

10. Website and Support

Renesas Electronics Website

<http://www.renesas.com/>

Inquiries

<http://www.renesas.com/contact/>

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Nov 30, 2018	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

- The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product

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