

Introduction

This application notes describes a sample program that performs reset control of the Watchdog Timer (WDTA).

The major features of the program are listed below:

- After the WDTA starts operating, refreshing operations are triggered at 223.7-ms intervals by using a compare match timer (CMT).
- Generation of a software wait in response to the external interrupt (IRQ5) stops refreshing operations, which leads to the generation of a reset. After the reset is generated, LED2 is turned on.

Target Devices for Operation Checking

RZ/T1 Group

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Table of Contents

1.	Specifications	3
2.	Operating Environment	4
3.	Related Application Notes	5
4.	Peripheral Functions	6
5.	Hardware	7
5.1	Example of Hardware Configuration	7
5.2	Pins	7
6.	Software	8
6.1	Operation Overview	8
6.1.1	Project Settings	9
6.2	Memory Map	9
6.2.1	Assignment to Sections of Sample Program	9
6.2.2	MPU Settings	9
6.2.3	Exception Processing Vector Table	9
6.3	Interrupts	10
6.4	Fixed-Width Integer Types	10
6.5	Constants/Error Codes	10
6.6	Structures/Unions/Enumerated Types	11
6.7	Functions	13
6.8	Specifications of Functions	13
6.8.1	main	13
6.8.2	wdt0_init	13
6.8.3	R_WDT_Open	14
6.8.4	R_WDT_Control	15
6.8.5	R_IRQ9_isr	15
6.8.6	R_IRQ21_isr	15
6.9	Flowcharts	16
6.9.1	Main Processing	16
6.9.2	WDT0 Initialization	17
6.9.3	WDT Open Function	18
6.9.4	WDT Control Function	19
6.9.5	IRQ9 Interrupt (IRQ Pin Interrupt 5) Processing	21
6.9.6	IRQ21 Interrupt (Compare Match Timer Ch0 Interrupt) Processing	21
7.	Sample Program	22
8.	Reference Documents	23

1. Specifications

Table 1.1 lists the peripheral functions to be used and their applications and Figure 1.1 shows the operating environment.

Table 1.1 Peripheral Functions and Applications

Peripheral Function	Application
Clock Pulse Generator (CPG)	The CPG produces the CPU clock and low-speed on-chip oscillator clock signals
Interrupt Control Unit A (ICUA)	The ICUA is used for the external interrupt input pin (IRQ5) and compare match timer interrupt (CMI0)
Compare Match Timer (CMT)	The CMT is used for cycle counting of a compare match timer.
Watchdog Timer A (WDTA)	The WDTA operates with a timeout period of 546.1 ms and control must be applied to refresh its counter at regular intervals. An ECM reset is generated in response to an underflow or error in refreshing the WDTA counter.
Error Control Module (ECM)	The ECM is used to initialize the ERROROUT# pins and to indicate underflows of or errors in refreshing the WDTA.
General I/O port	The general I/O port is used to control pins for turning the LEDs on and off.

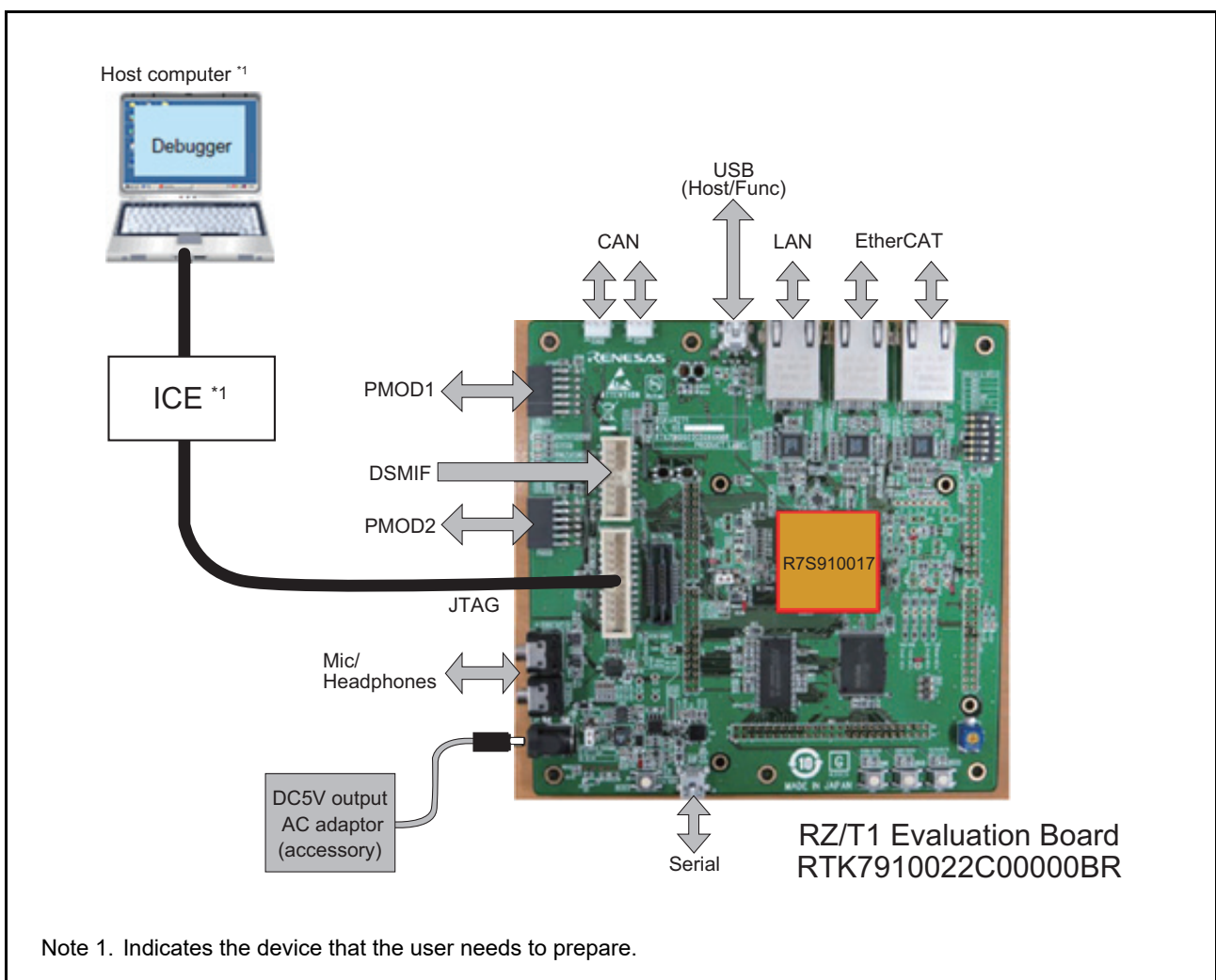


Figure 1.1 Operating Environment

2. Operating Environment

The sample program of this application is for the environment below.

Table 2.1 Operating Environment

Item	Description
Microcomputer	RZ/T1 Group
Operating frequency	CPUCLK = 450 MHz
Operating voltage	3.3 V
Integrated development environment	Manufactured by IAR Systems Embedded Workbench® for Arm Version 8.20.2 Manufactured by Arm DS-5™ 5.26.2 Manufactured by RENESAS e2studio 6.1.0
Operating modes	SPI boot mode 16-bit bus boot mode
Board	RZ/T1 Evaluation board (RTK7910022C00000BR)
Devices (functions to be used on the board)	<ul style="list-style-type: none"> • NOR flash memory (connected to CS0/CS1 space) Manufacturer: Macronix International Co. Ltd. Model: MX29GL512FLT2I-10Q • SDRAM (connected to CS2/CS3 space) Manufacturer: Integrated Silicon Solution Inc. Model: IS42S16320D-7TL • Serial flash memory Manufacturer: Macronix International Co. Ltd. Model: MX25L51245G

3. Related Application Notes

Refer to the relevant application notes listed below.

- RZ/T1 Group Initial Settings
- RZ/T1 Group Compare Match Timer (CMT)

4. Peripheral Functions

For the basics of the clock pulse generator (CPG), Watchdog Timer (WDTA), compare match timer (CMT), interrupt control unit A (ICUA), error control module (ECM), general input/output port, refer to the RZ/T1 Group User's Manual: Hardware.

5. Hardware

5.1 Example of Hardware Configuration

Figure 5.1 shows an example of hardware configuration.

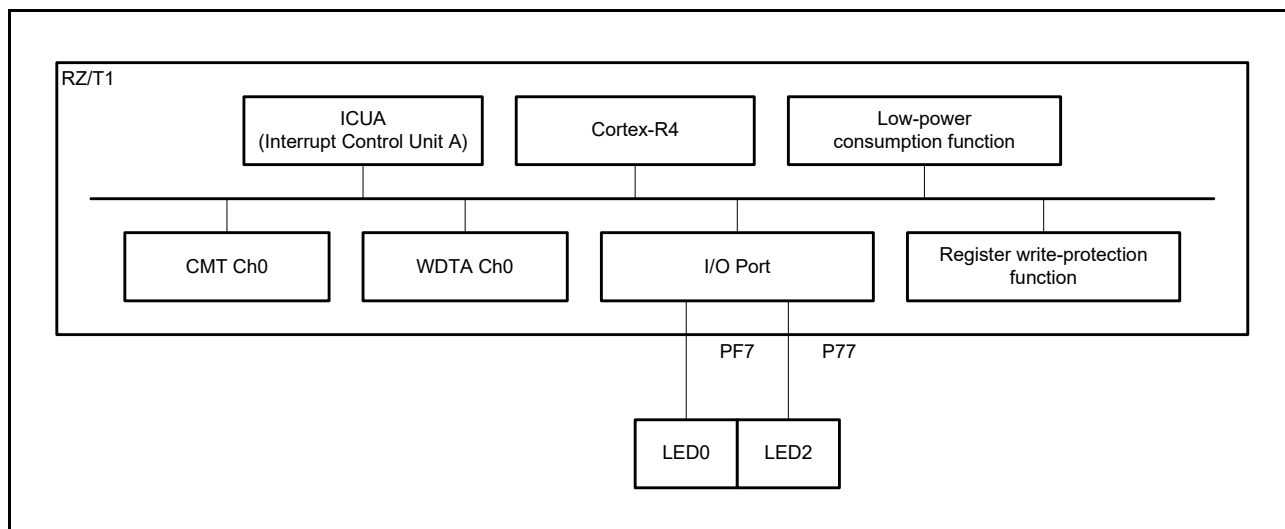


Figure 5.1 Example of Hardware Configuration

5.2 Pins

Table 5.1 shows pins to be used and their functions.

Table 5.1 Pins and Pin Functions

Pin Name	I/O	Function
MD0	Input	Selection of operating modes
MD1	Input	MD0 = L, MD1 = L, MD2 = L (SPI boot mode) MD0 = L, MD1 = H, MD2 = L (16-bit bus boot mode)
MD2	Input	
IRQ5	Input	SW2 (IRQ pin interrupt)
PF7	Output	Turning LED0 on and off
P77	Output	Turning LED2 on and off

6. Software

6.1 Operation Overview

The sample program makes the initial settings of the Watchdog Timer (WDTA), and then performs refreshing operations at regular intervals (227.3 ms) by using interval interrupts of the compare match timer.

Pressing SW2 down generates an external pin interrupt 5 and a software wait proceeds during the interrupt processing. During this period, as CMT interval interrupts are held, the WDTA stops refreshing operations. Thus, the value of the counter of the WDTA underflows and this leads to notification of an error to the ECM and then to generation of an ECM reset. LED2 is turned on based on the reset judgment after reset release.

Table 6.1 shows the functional overview of the sample program and Figure 6.1 shows the timing diagram.

Table 6.1 Functional Overview

Function	Description
Channel	Channel 0
Clock	PCLK/2048 (=75 MHz/2048)
Timeout	16384 cycles (= 447.4 ms)
Window	Start: 75% End: 25%
Notification of errors to ECM	Enabled

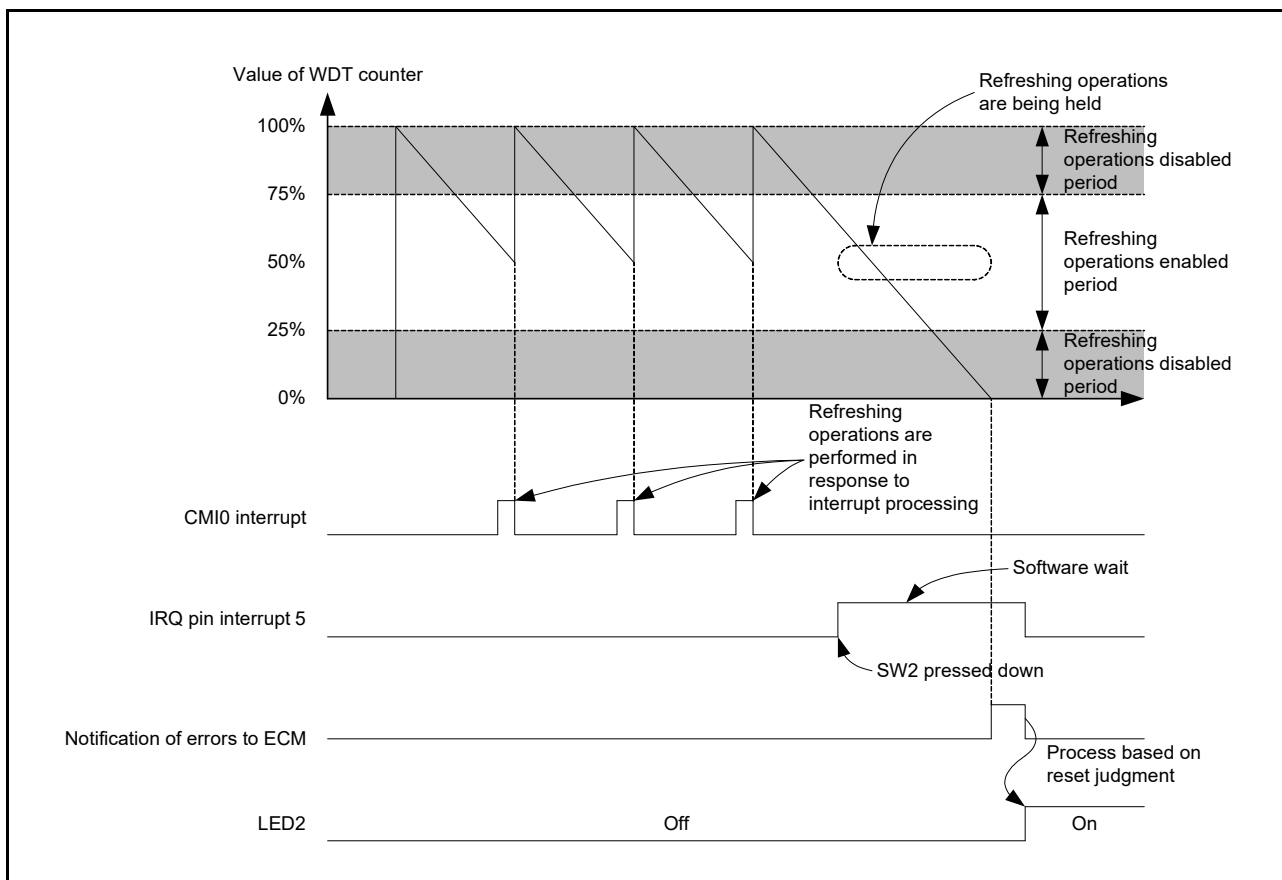


Figure 6.1 Timing Diagram

6.1.1 Project Settings

For the settings of the project to be used on the EWARM for development environment, refer to the Application Note: RZ/T1 Group Initial Settings.

6.2 Memory Map

For the address space of the RZ/T1 Group and a memory map of the RZ/T1 evaluation board, refer to the Application Note: RZ/T1 Group Initial Settings.

6.2.1 Assignment to Sections of Sample Program

Refer to the Application Note: RZ/T1 Group Initial Settings for the sections to be used in the sample program, assignment to sections (loading view) of the sample program in its initial state, and assignment to sections of the sample program following the application of scatter loading (execution view).

6.2.2 MPU Settings

Refer to the Application Note: RZ/T1 Group Initial Settings for MPU settings.

6.2.3 Exception Processing Vector Table

Refer to the Application Note: RZ/T1 Group Initial Settings for the vector table for exception processing.

6.3 Interrupts

Table 6.2 shows interrupts to be used in the sample program.

Table 6.2 Interrupts for Sample Program

Interrupt (Source ID)	Priority	Processing
IRQ pin interrupt 5 (IRQ9)	0	Pressing SW2 down causes an underflow without refreshing of the WDTA and generates an ECM reset. Based on the reset judgment after reset release, LED2 is turned on.
Compare match interrupt_ch0 (CMI0)	15	Every time an interval period (227.3-ms interval) is generated, refreshing operations of the WDTA are performed.

6.4 Fixed-Width Integer Types

Table 6.3 shows fixed width integers to be used in the sample program.

Table 6.3 Fixed-Width Integers for Sample Program

Symbol	Description
int8_t	8-bit signed integer (defined in the standard library)
int16_t	16-bit signed integer (defined in the standard library)
int32_t	32-bit signed integer (defined in the standard library)
int64_t	64-bit signed integer (defined in the standard library)
uint8_t	8-bit unsigned integer (defined in the standard library)
uint16_t	16-bit unsigned integer (defined in the standard library)
uint32_t	32-bit unsigned integer (defined in the standard library)
uint64_t	64-bit unsigned integer (defined in the standard library)

6.5 Constants/Error Codes

Table 6.4 shows constants to be used in the sample program.

Table 6.4 Constants for Sample Program

Constant Name	Setting Value	Description
WDT_STAT_REFRESH_ERR_MASK	(0x8000)	A definition to acquire a refreshing error flag from the WDT status.
WDT_STAT_UNDERFLOW_ERR_MASK	(0x4000)	A definition to acquire an underflow flag from the WDT status.
WDT_STAT_ERROR_MASK	(0xC000)	A definition to acquire a refreshing error flag and underflow flag from the WDT status.
WDT_STAT_COUNTER_MASK	(0x3FFF)	A definition to acquire a counter value from the WDT status.
WDT_CFG_PARAM_CHECKING_ENABLE	(1)	The API function of WDTA indicates enabling (1) or disabling (0) of parameter checking.

6.6 Structures/Unions/Enumerated Types

Figure 6.2 to Figure 6.4 show the structures, unions, and enumerated types to be used in the sample program.

```

/* API ERROR RETURN CODES */
typedef enum e_wdt_err      // WDT API error codes
{
    WDT_SUCCESS=0,
    WDT_ERR_OPEN_IGNORED,    // The module has already been Open()ed
    WDT_ERR_INVALID_ARG,    // Argument is not valid for parameter
    WDT_ERR_NULL_PTR,       // Received null pointer or missing required argument
    WDT_ERR_NOT_OPENED      // Open function has not yet been called
} wdt_err_t;

typedef enum e_wdt_ch      // WDT channel
{
    WDT_CHANNEL_0=0,        // Ch0
    WDT_CHANNEL_1,         // Ch1
    WDT_CHANNEL_MAX
} wdt_ch_t;

/* Open() DEFINITIONS */
typedef enum e_wdt_timeout // WDT Time-Out Period
{
    WDT_TIMEOUT_1024=0x0000u, // 1024 (cycles)
    WDT_TIMEOUT_4096=0x0001u, // 4096 (cycles)
    WDT_TIMEOUT_8192=0x0002u, // 8192 (cycles)
    WDT_TIMEOUT_16384=0x0003u, // 16,384 (cycles)
    WDT_NUM_TIMEOUTS
} wdt_timeout_t;

```

Figure 6.2 Structures/Unions/Enumerated Types for Sample Program

```

typedef enum e_wdt_clock_div      // WDT Clock Division Ratio
{
    WDT_CLOCK_DIV_4   =0x0010u,    // WDTCLK/4
    WDT_CLOCK_DIV_64  =0x0040u,    // WDTCLK/64
    WDT_CLOCK_DIV_128 =0x00F0u,    // WDTCLK/128
    WDT_CLOCK_DIV_512 =0x0060u,    // WDTCLK/512
    WDT_CLOCK_DIV_2048=0x0070u,    // WDTCLK/2048
    WDT_CLOCK_DIV_8192=0x0080u    // WDTCLK/8192
} wdt_clock_div_t;

typedef enum e_wdt_window_end     // Window End Position
{
    WDT_WINDOW_END_75=0x0000u,    // 75%
    WDT_WINDOW_END_50=0x0100u,    // 50%
    WDT_WINDOW_END_25=0x0200u,    // 25%
    WDT_WINDOW_END_0 =0x0300u    // 0% (window end position is not specified)
} wdt_window_end_t;

typedef enum e_wdt_window_start   // Window Start Position
{
    WDT_WINDOW_START_25 =0x0000u,  // 25%
    WDT_WINDOW_START_50 =0x1000u,  // 50%
    WDT_WINDOW_START_75 =0x2000u,  // 75%
    WDT_WINDOW_START_100=0x3000u   // 100% (window start position is not specified)
} wdt_window_start_t;

typedef enum e_wdt_timeout_control // Signal control when Time-out and Refresh error
{
    WDT_ERROR_ENABLE =0x00u, // Error output is enabled
    WDT_ERROR_DISABLE=0x80u  // Error output is disabled
} wdt_timeout_control_t;

```

Figure 6.3 Structures/Unions/Enumerated Types for Sample Program

```

typedef struct st_wdt_config      // WDT configuration options used in Open function
{
    wdt_timeout_t      timeout;      // Time-out period
    wdt_clock_div_t    wdtclk_div;   // WDT clock division ratio
    wdt_window_start_t window_start;  // Window start position
    wdt_window_end_t   window_end;   // Window end position
    wdt_timeout_control_t timeout_control; // ERROR output when time-out
} wdt_config_t;

/* Control() DEFINITIONS */

typedef enum e_wdt_cmd           // Command used in Control and GetStatus function
{
    WDT_CMD_GET_STATUS,          // Get WDT status
    WDT_CMD_REFRESH_COUNTING,   // Refresh the counter
    WDT_CMD_NO_ACTION,
} wdt_cmd_t;

```

Figure 6.4 Structures/Unions/Enumerated Types for Sample Program

6.7 Functions

Table 6.5 lists functions to be used.

Table 6.5 Functions

Function	Page Number
main	13
wdt0_init	13
R_WDT_Open	14
R_WDT_Control	15
R_IRQ9_isr	15
R_IRQ21_isr	15

6.8 Specifications of Functions

6.8.1 main

main	
Synopsis	Main processing
Declaration	int main (void)
Description	This function makes initial settings for the ports, ECM, CMT, ICU, and WDT, and starts operation of CMT0. After that, the main loop of the function repeatedly alternates between LED0 on and off.
Arguments	None
Return value	None
Supplement	None

6.8.2 wdt0_init

wdt0_init	
Synopsis	Initializing WDT0
Declaration	void wdt0_init (void)
Description	This function initializes the WDT0 and starts counting operation of the WDT0.
Arguments	None
Return value	None
Supplement	None

6.8.3 R_WDT_Open

R_WDT_Open

Synopsis	WDT open
Header	r_wdt_if.h
Declaration	wdt_err_t R_WDT_Open (uint16_t channel, void * const p_cfg)
Description	This function initializes WDTA-related registers and sets the options of the WDT counter.
Arguments	<p>uint16_t channel This specifies the WDT channels Setting range: (0, 1)</p> <p>void * const p_cfg The pointer that stores the data group to be set in the WDTA-related registers.</p> <p>Timeout period WDT_TIMEOUT_1024 WDT_TIMEOUT_4096 WDT_TIMEOUT_8192 WDT_TIMEOUT_16384</p> <p>Clock division ratio WDT_CLOCK_DIV_4 WDT_CLOCK_DIV_64 WDT_CLOCK_DIV_128 WDT_CLOCK_DIV_512 WDT_CLOCK_DIV_2048 WDT_CLOCK_DIV_8192</p> <p>Window stop WDT_WINDOW_END_75 WDT_WINDOW_END_50 WDT_WINDOW_END_25 WDT_WINDOW_END_0</p> <p>Window start WDT_WINDOW_START_25 WDT_WINDOW_START_50 WDT_WINDOW_START_75 WDT_WINDOW_START_100</p> <p>Notification of ECM errors WDT_ERROR_ENABLE WDT_ERROR_DISABLE</p>
Return value	<p>Execution result of the open function is returned.</p> <p>WDT_SUCCESS: IWDT initialized</p> <p>WDT_ERR_OPEN_IGNORED: Module already opened</p> <p>WDT_ERR_INVALID_ARG: Invalid values included in the element of the p_cfg structure.</p> <p>WDT_ERR_NULL_PTR: p_cfg pointer null</p>
Supplement	Setting WDT_CFG_PARAM_CHECKING_ENABLE that is defined by r_wdt_config.h to 1 enables checking of the parameters of the arguments.

6.8.4 R_WDT_Control

R_WDT_Control

Synopsis	Controlling WDT	
Header	r_wdt_if.h	
Declaration	wdt_err_t R_WDT_Control (uint16_t channel, wdt_cmd_t const cmd, uint16_t * p_status)	
Description	This function reads the WDT state of the specified channel and refreshes the down counter of the WDT.	
Arguments	uint16_t channel	WDT channel specification Setting range: (0, 1)
	wdt_cmd_t const cmd	Specifies the command to be executed IWDT_CMD_GET_STATUS IWDT_CMD_REFRESH_COUNTING
	uint16_t * p_status	The pointer to the storage positions of the counter and status flag
Return value	Execution result of the control function WDT_SUCCESS: Command completed WDT_ERR_INVALID_ARG: Argument value invalid WDT_ERR_NULL_PTR: p_status null. WDTERR_NOT_OPEND: Open unread.	
Supplement	Setting WDT_CFG_PARAM_CHECKING_ENABLE that is defined by r_wdt_config.h to 1 enables checking of the parameters of the argument.	

6.8.5 R_IRQ9_isr

R_IRQ9_isr

Synopsis	IRQ9 interrupt (IRQ pin interrupt 5) processing	
Declaration	void R_IRQ9_isr (void)	
Description	This function executes software wait processing (approx. 3 seconds). During this period, it causes an underflow of the watchdog timer and generates an ECM reset. It also turns LED2 on based on the reset judgment after reset release.	
Arguments	None	
Return value	None	
Supplement	None	

6.8.6 R_IRQ21_isr

R_IRQ21_isr

Synopsis	IRQ21 interrupt (compare match timer (CMI0)) processing	
Declaration	void R_IRQ21_isr (void)	
Description	This functions performs refreshing operations of the watchdog timer.	
Arguments	None	
Return value	None	
Supplement	None	

6.9 Flowcharts

6.9.1 Main Processing

Figure 6.5 shows a flowchart of main processing.

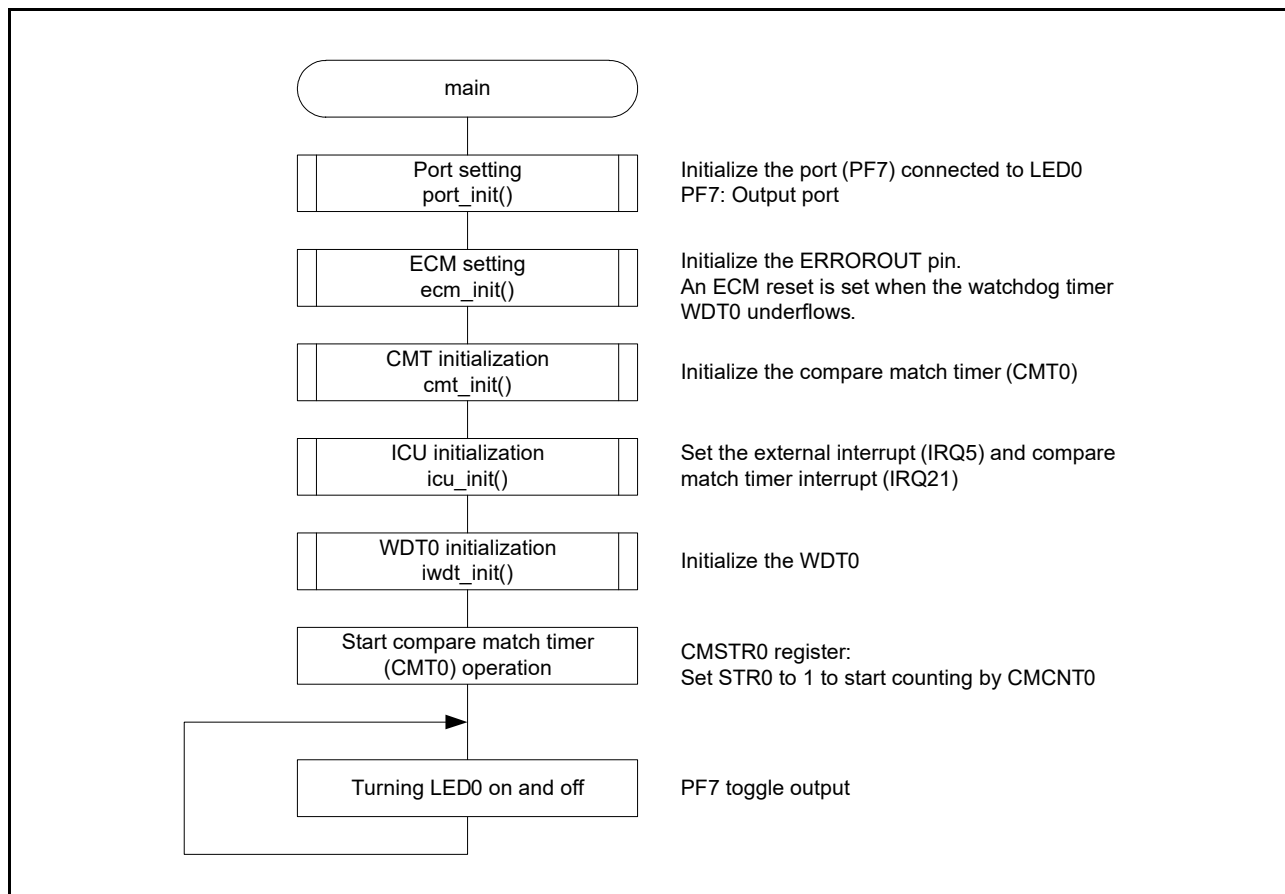


Figure 6.5 Main Processing

6.9.2 WDT0 Initialization

Figure 6.6 show a flowchart of WDT0 initialization.

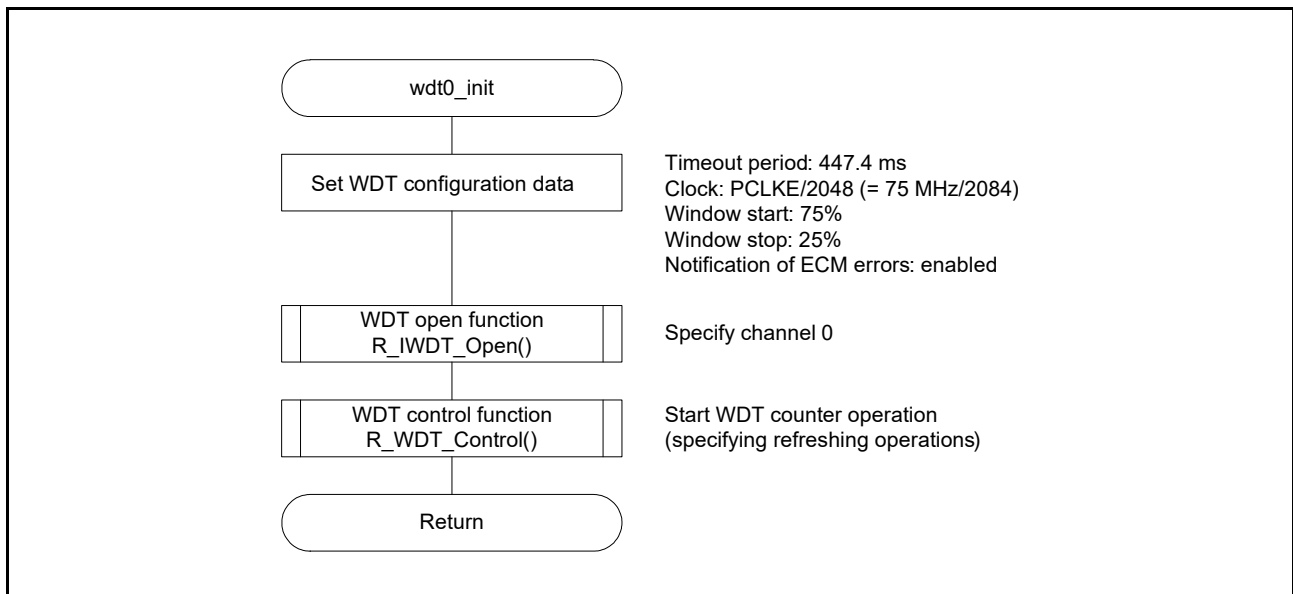


Figure 6.6 WDT0 Initialization

6.9.3 WDT Open Function

Figure 6.7 shows a flowchart of WDT open function.

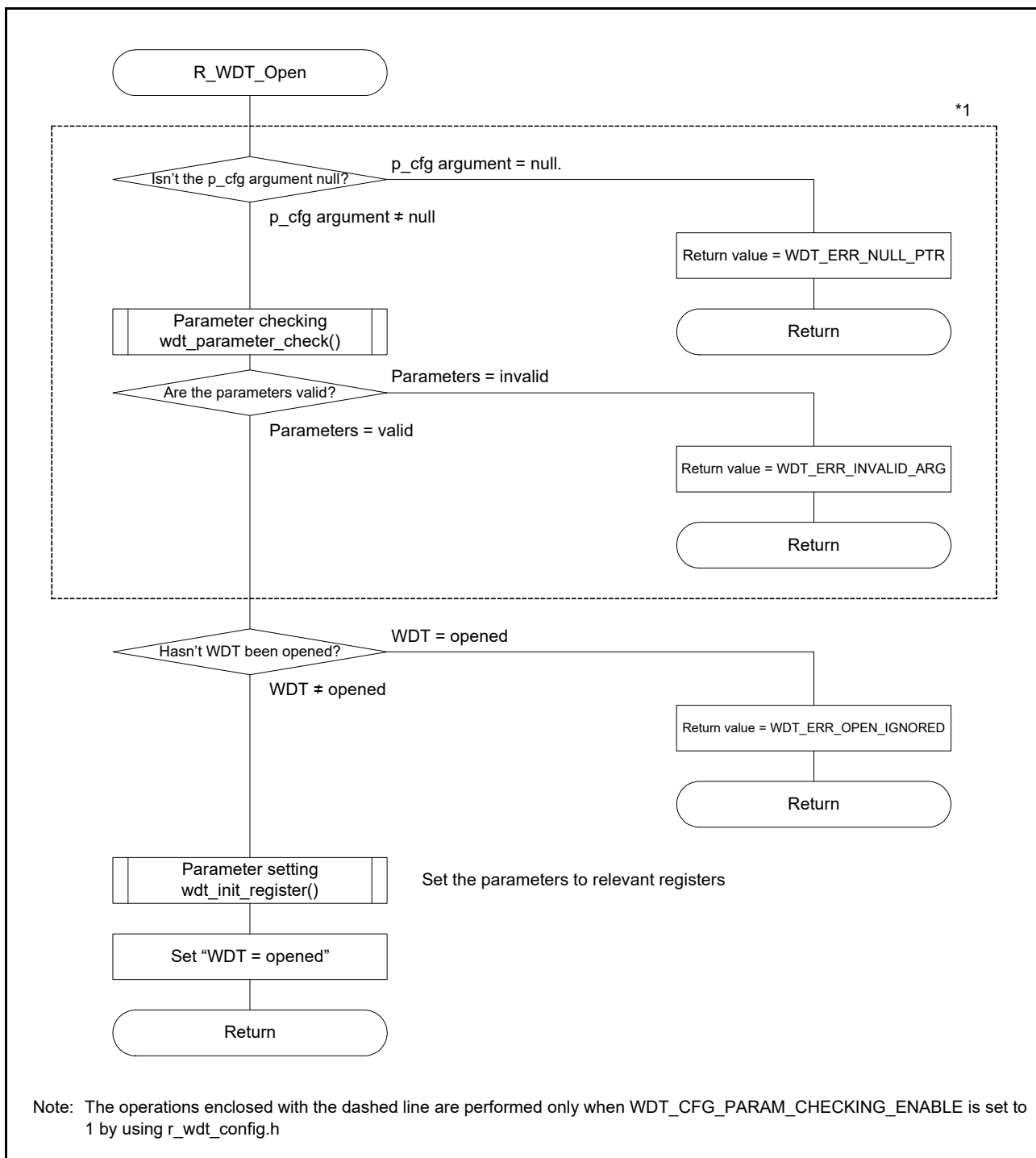


Figure 6.7 WDT Open Function

6.9.4 WDT Control Function

Figure 6.8 and Figure 6.9 show flowcharts of the WDT control function.

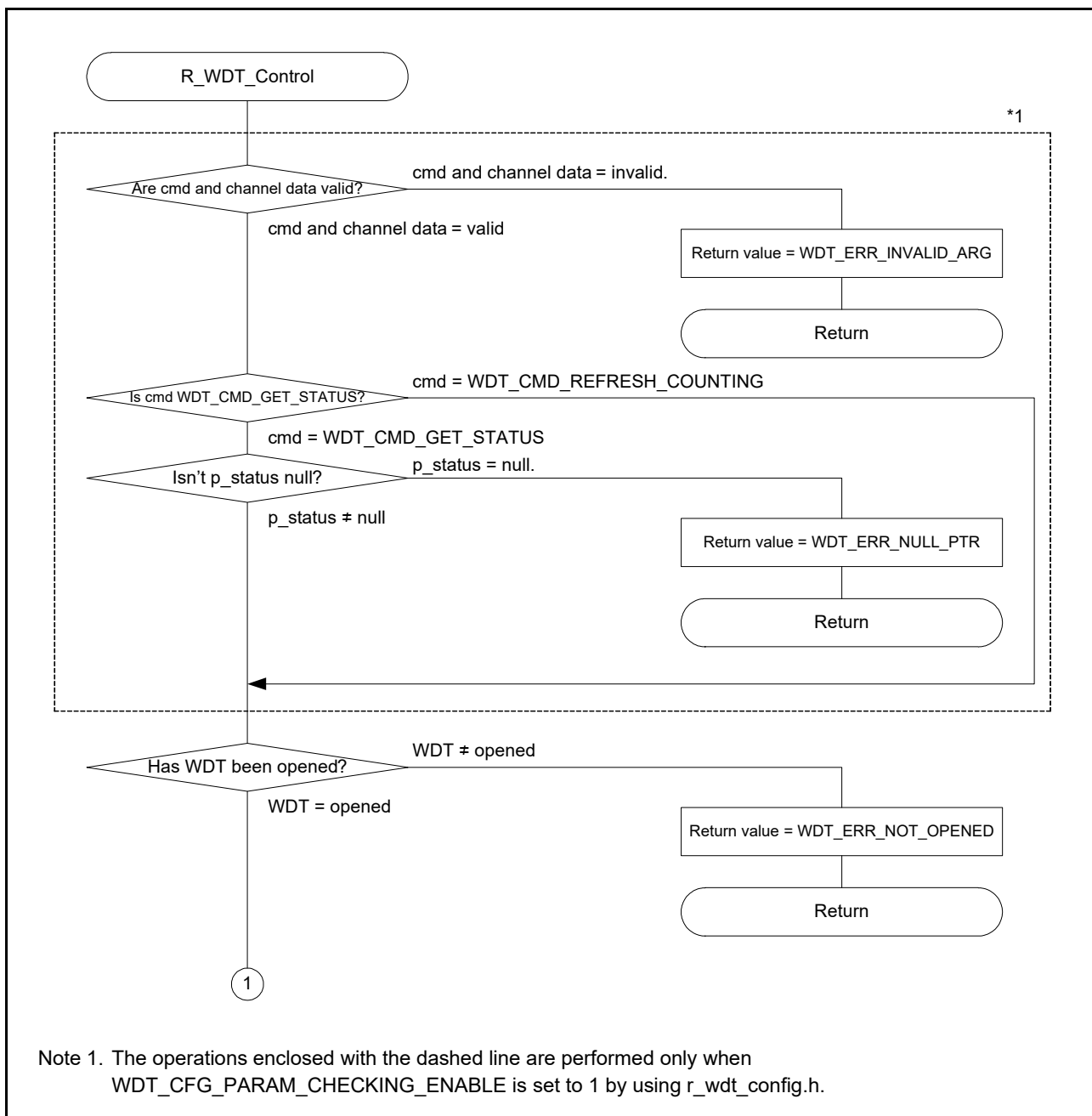


Figure 6.8 WDT Control Function

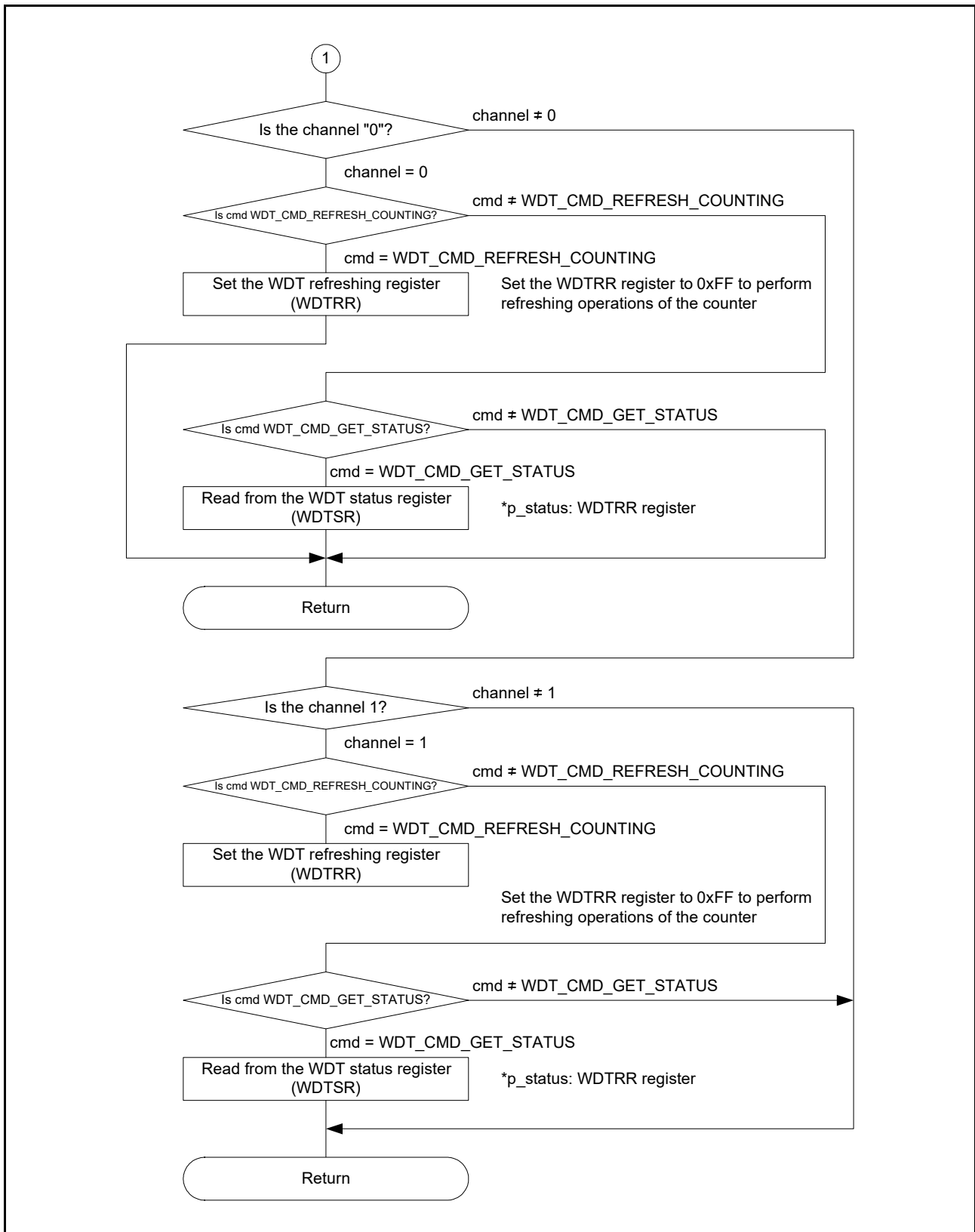


Figure 6.9 WDT Control Function

6.9.5 IRQ9 Interrupt (IRQ Pin Interrupt 5) Processing

Figure 6.10 shows a flowchart of the IRQ9 interrupt (IRQ pin interrupt 5) processing.

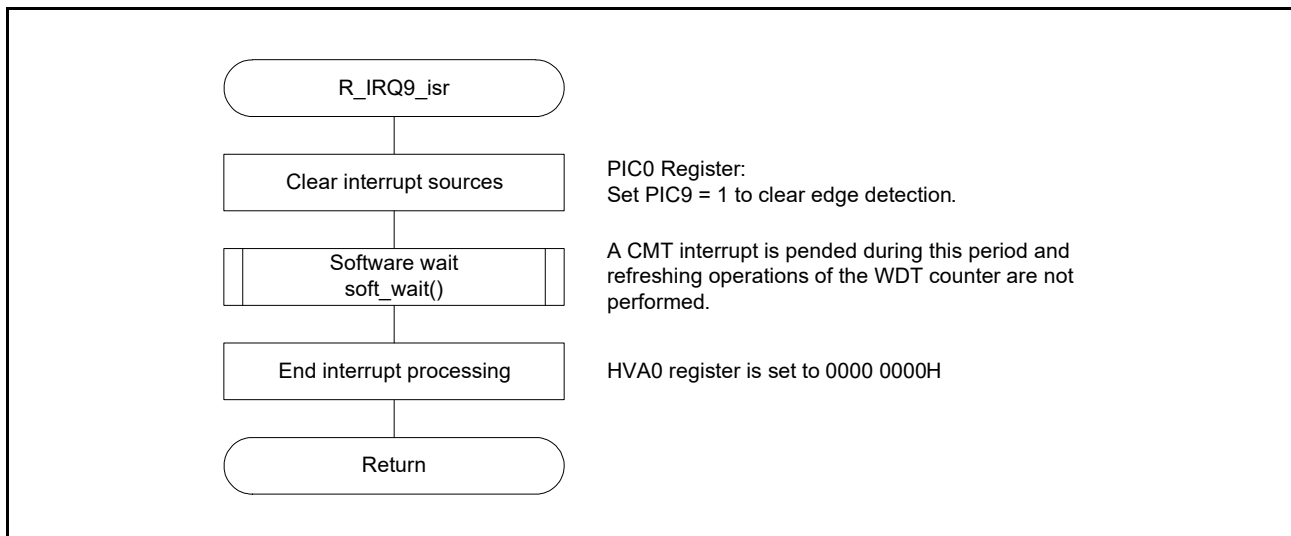


Figure 6.10 IRQ9 Interrupt (IRQ Pin Interrupt 5) Processing

6.9.6 IRQ21 Interrupt (Compare Match Timer Ch0 Interrupt) Processing

Figure 6.11 shows a flowchart of IRQ21 interrupt (compare match timer ch0 interrupt) processing.

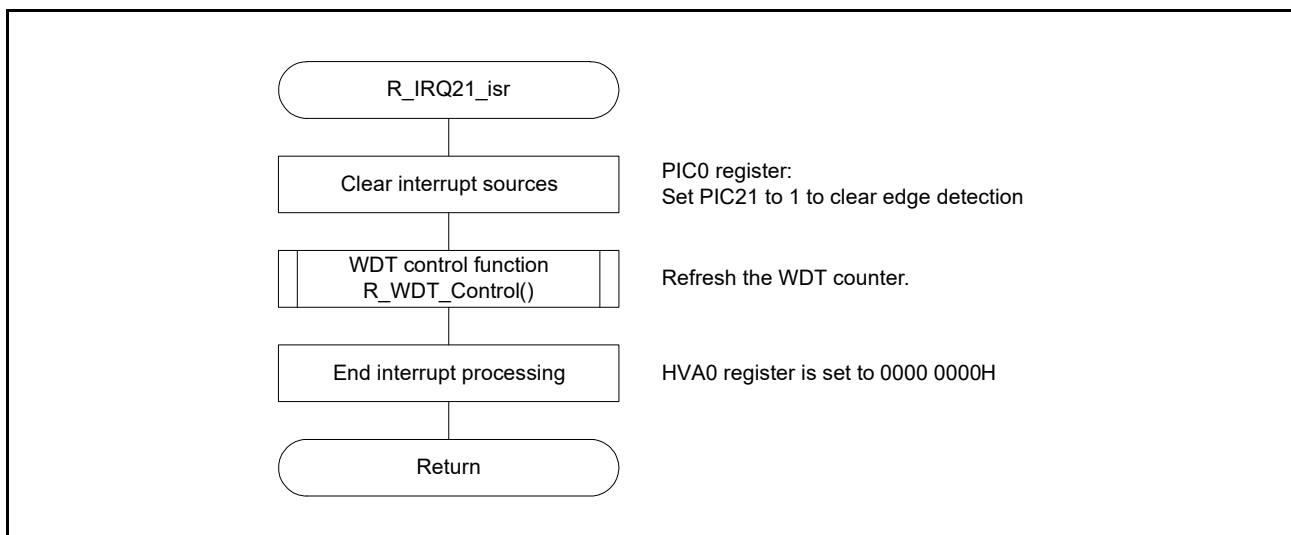


Figure 6.11 IRQ21 Interrupt (Compare Match Timer ch0 Interrupt) Processing

7. Sample Program

The sample program is available on the Renesas Electronics website.

8. Reference Documents

User's manual: hardware:

RZ/T1 Group User's Manual: Hardware

(Download the latest version of the manual from the Renesas Electronics website.)

RZ/T1 Evaluation Board RTK7910022C00000BR User's Manual

(Download the latest version of the manual from the Renesas Electronics website.)

Technical Update / Technical News

(Download the latest version of the update or news from the Renesas Electronics website.)

User's manual: Development Environment

For IAR integrated development environment (IAR Embedded Workbench® for Arm), visit the IAR Systems website.

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Website and Support

Renesas Electronics website

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Inquiries

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Revision History

Application Note: Watchdog Timer (WDTA)

Rev.	Date	Description	
		Page	Summary
0.20	Mar. 18, 2015	—	First Edition issued
1.00	Apr. 10, 2015	—	Only the revision number was changed to be posted on a website.
1.10	Aug. 18, 2015	2. Operating Environment	
		4	Table 2.1 Operating Environment: Integrated Development Environment, partially amended and added
		6. Software	
		9	6.2.4 Required Memory Size: Description and reference added
		9	Table 6.2: Table title was partially amended
		10	Table 6.3 added
		10	Table 6.4 added
1.20	Dec. 04, 2015	2. Operating Environment	
		4	Table 2.1 Operating Environment: Integrated Development Environment, information partially amended
1.30	Apr. 05, 2017	2. Operating Environment	
		4	Table 2.1 Operating Environment: Integrated Development Environment, modified
		6. Software	
		—	6.2.4 Required Memory Size, deleted
1.40	Jun. 07, 2018	2. Operating Environment	
		4	Table 2.1 Operating Environment: The description on the integrated development environment, modified
		5. Hardware	
		7	Figure 5.1 Hardware configuration example: The name of module, modified
		8. Related Documents	
		23	The name of IAR Embedded Workbench, modified

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

- The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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