RX610 Group

Example of Pulse Output Using TMR (Cascade Connection)

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Abstract

This application note presents a sample program that uses the TMR (8-bit timer) module of the RX610 Group to output a user-defined number of pulses with a 50% duty cycle.

Target Device

RX 610 Group

Introduction

The documentation in this application note is based on the *RX610 Group Hardware Manual*. The appended program code can be used with the devices listed above, on which operation has been confirmed.

Note that changes are sometimes made to the functional specifications of individual devices. Check the latest version of the *Hardware Manual* and make a careful evaluation before using this application note.

The program works with an endian specification of big or little and with left or right specified as the bit order.

Contents

1. Specifications

TMR0 and TMR1 are configured in a cascade connection (compare match count mode) and a user-defined number of pulse cycles with a 50% duty cycle are output from the TMO0 pin by having TMR0 count the output pulses and TMR0 count the compare matches with TMR1 (Figure 1). In this application note, when the PCLK frequency is 50 MHz, the pulse period can be set to any duration from 0.64 µs to 40.96 µs, specified in 0.32 µs increments. In addition, the number of pulses can be specified as any value from 1 to 255.

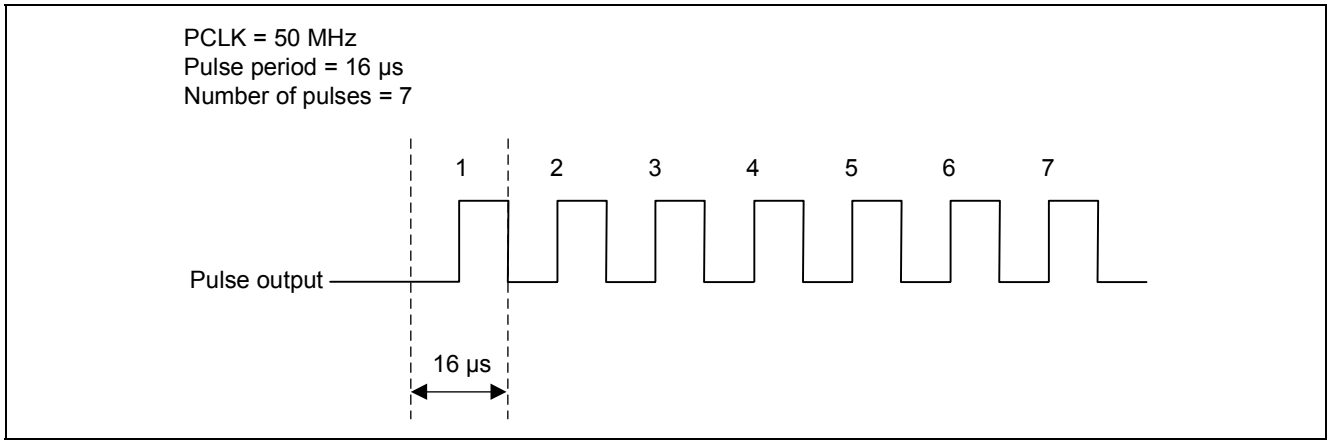


Figure 1 Pulse Output Timing

2. 8-Bit Timer (TMR) Function Description

The device has an 8-bit timer (TMR) module based on 8-bit counters. The TMR comprises two units (unit 0 and unit 1), each with two channels, for a total of four channels. The 8-bit timer module can be used to count external events and also be used as a multifunction timer in a variety of applications, such as generation of counter resets, interrupt requests, and pulse output with a desired duty cycle using a compare-match signal for two registers.

2.1 Operation with Cascade Connection

Setting bits CSS1 and CSS0 in the TMR0.TCCR or TMR1.TCCR register to 11b causes the two channels of the TMR unit to be configured in a cascade connection. Cascade connection can be used in 16-bit count mode, in which the two channels function as a single 16-bit timer, or in compare match count mode, in which TMR1 counts the compare matches of TMR0.

2.1.1 Compare Match Count Mode

When bits CSS1 and CSS0 in the TMR1.TCCR register are set to 11b, the TMR1.TCNT counter counts the number of times compare match A is generated by TMR0. TMR0 and TMR1 are controlled independently. Conditions such as generation of interrupts, output from the TMOn (n = 0, 1) pins, and counter clear are in accordance with the settings for each channel.

2.2 Block Diagram

Figure 2 is a block diagram of the 8-bit timer (unit 0) used by the sample program.

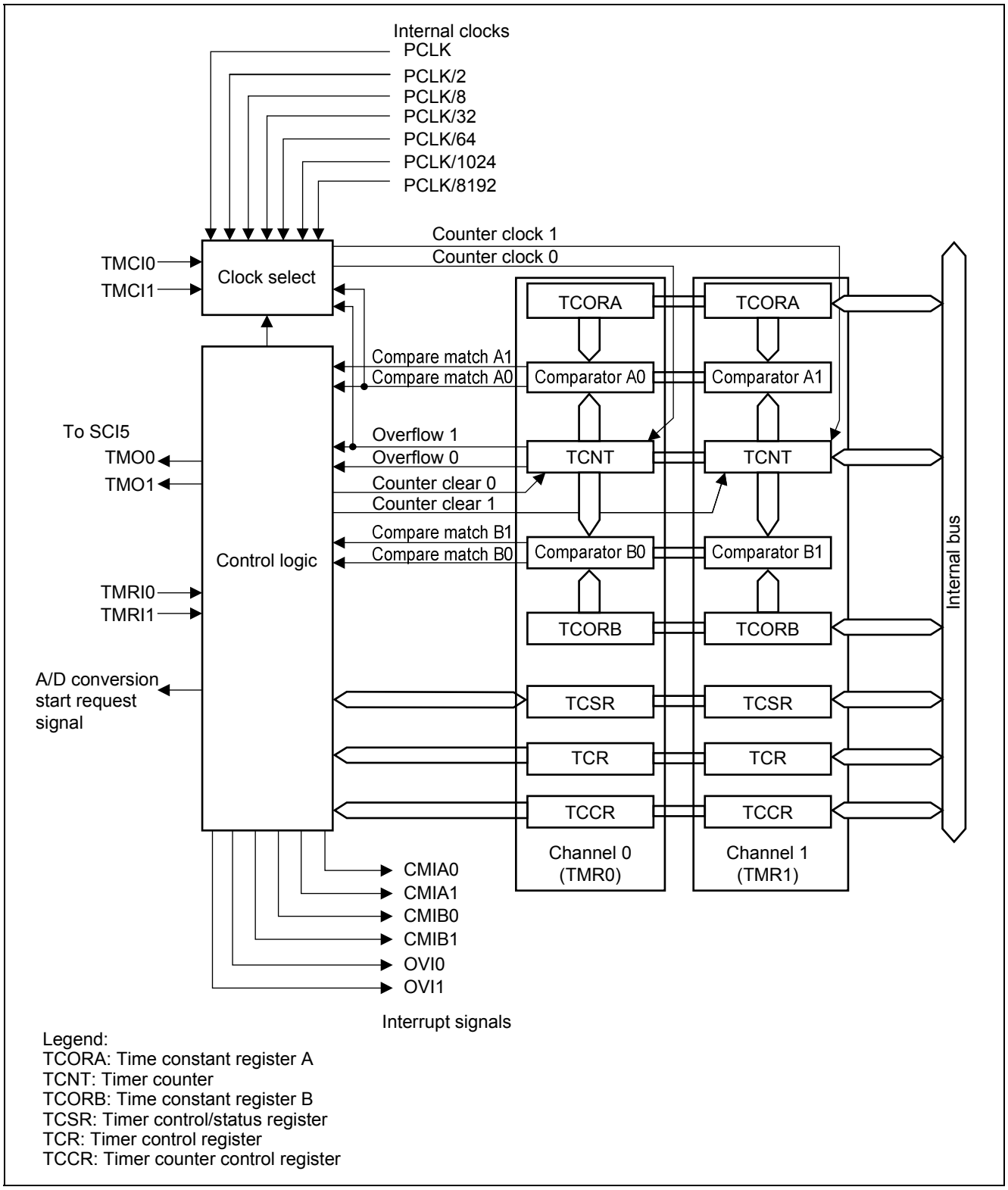


Figure 2 TMR (Unit 0) Block Diagram

3. Operation

Figure 3 illustrates the operation of the sample program.

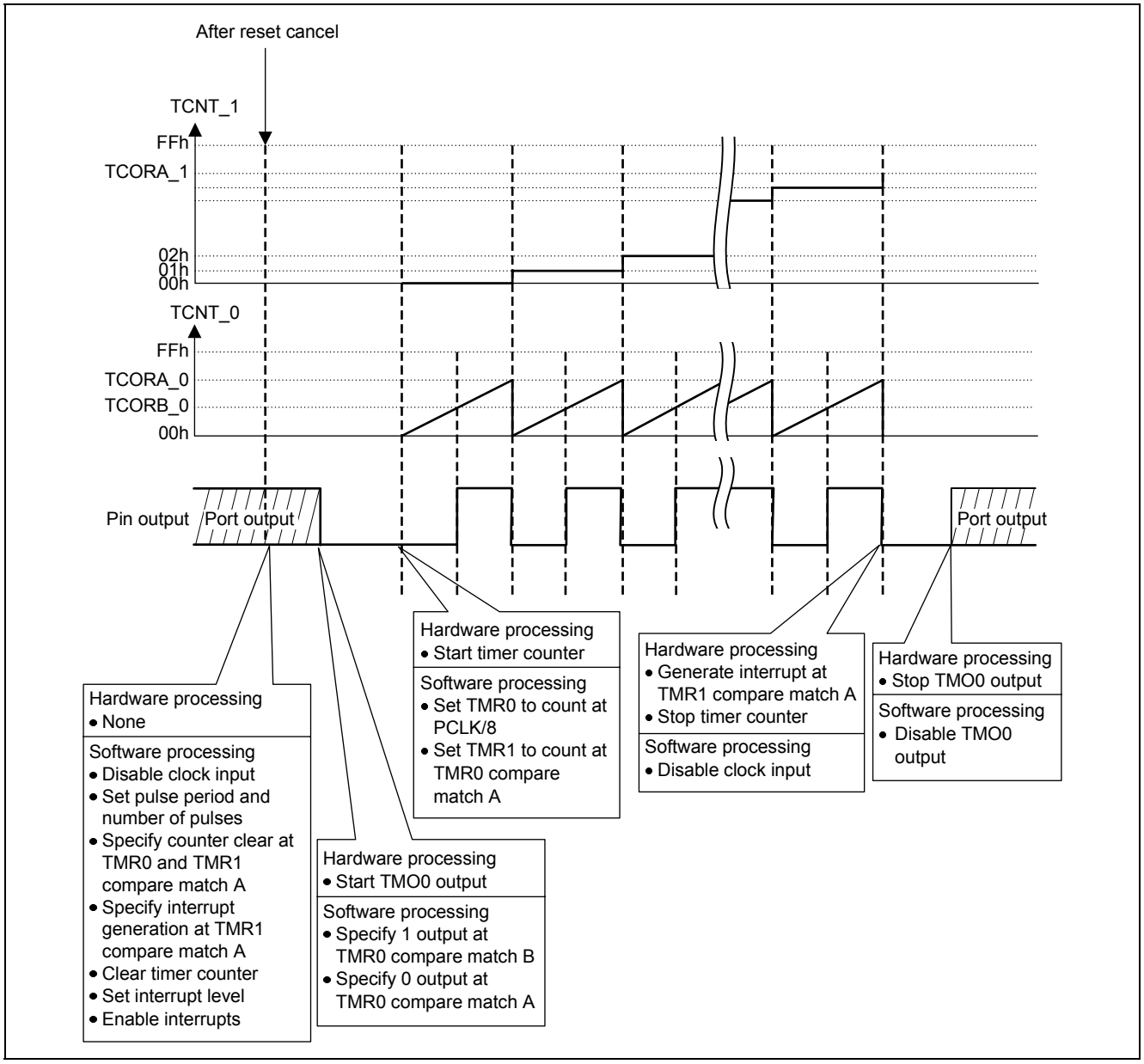


Figure 3 Operation

4. Software Description

4.1 Symbolic Constants

Table 1 List of Symbolic Constants

Constant Name	Setting Value	Description	Used by Functions
CYCLE	49	Pulse period setting constant (setting range: 1 to 127)	main
COUNT	7	Number of pulses setting constant (setting range: 1 to 255)	main
PULSE_OK	0	Error processing code (normal end)	main, pulse
CYCLE_ERROR	1	Error processing code (pulse period setting value error)	main, pulse
COUNT_ERROR	2	Error processing code (number of pulses setting value error)	main, pulse

4.2 List of Functions

Table 2 List of Functions

Function Name	Description
PowerON_Reset_PC	• Initial settings function Sets INTB, FPSW, and PSW, changes processor mode, calls main function.
main	• Main function Sets initial values, calls pulse function.
init_pulse	• Pulse output initialization function Makes register settings.
Excep_TMR1_CMI1A	• TMR1 compare match interrupt function Stops pulse output.

4.2.1 PowerON_Reset_PC Function

(1) Functional overview

The PowerON_Reset_PC function initializes the stack pointer (SP) and uses embedded functions and a standard library function to set interrupt mask bits, make uninitialized/initialized data settings, etc. Then it calls the main function.

(2) Arguments

None

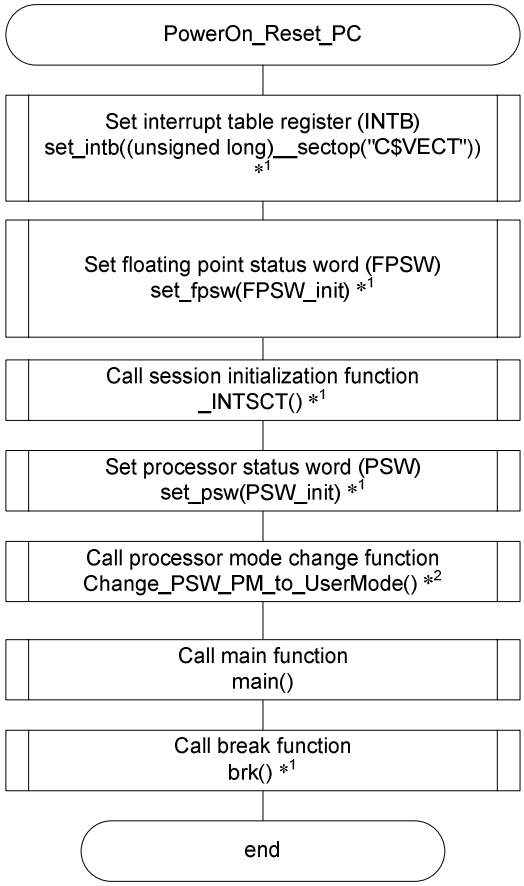
(3) Return values

None

(4) Description of I/O registers used

None

(5) Flowchart



Notes: 1. • set_intb, set_fpsw, and set_psw functions: embedded functions
• _INTSCT function: standard library function
• brk function: embedded function
2. • Transition from supervisor mode to user mode
For details, see “Development Environment Manual” in 6, Reference Documents.

Figure 4 Flowchart of PowerON_Reset_PC Function

4.2.2 main Function

(1) Functional overview

The main function first makes settings in the system clock control register (SCKCR), then cancels the module stop state of TMR0 and TMR1. Then it calls the init_pulse function to initialize the 8-bit timer and generate pulse output.

(2) Arguments

None

(3) Return values

None

(4) Description of I/O registers used

The I/O registers used by this function are shown below.

Note that the setting values shown are those used in this application note and differ from the initial values.

System Clock Control Register (SCKCR) Number of Bits: 32 Address: 080020h

Bit	Symbol	Setting Value	Bit Name	Function	R/W
b11 to b8	PCK[3:0]	1	Peripheral module clock (PCLK) select bits	These bits set the peripheral module clock (PCLK) frequency. 1: Input clock × 4	R/W
b19 and b18	BCK[3:0]	2	External bus clock (BCLK) select bits	These bits set the external bus clock (BCLK) frequency. 2: Input clock × 2	R/W
b23	PSTOP1	0	BCLK output stop bit	This bit controls BCLK output. 0: BCLK output	R/W
b27 to b24	ICK[3:0]	0	System clock (ICLK) select bits	These bits set the system clock (ICLK) frequency. 0: Input clock × 8	R/W

Module Stop Control Register A (MSTPCRA) Number of Bits: 32 Address: 080010h

Bit	Symbol	Setting Value	Bit Name	Function	R/W
b5	MSTPA5	0	8-bit timer 1/0 (unit 0) module stop bit	This bit controls the module stop state. Target modules: TMR1, TMR0 0: Module stop state canceled	R/W

4.2.3 init_pulse Function

(1) Functional overview

The init_pulse function initializes registers associated with TMR0 and TMR1.

(2) Arguments

Argument	Type	Argument Name	Argument Value	Description
1st argument	unsigned char	pulse_cycle	1 to 127	For setting the pulse period
2nd argument	unsigned char	pulse_count	1 to 255	For setting the number of pulses

(3) Return values

Type	Return Value Name	Return Value	Description
unsigned char	return_code	PULSE_OK	PULSE_OK (0) : Normal end
		CYCLE_ERROR	CYCLE_ERROR (1): Pulse period setting value error
		COUNT_ERROR	COUNT_ERROR(2): Number of pulses setting value error

(4) Description of I/O registers used

The I/O registers used by this function are shown below.

Note that the setting values shown are those used in this application note and differ from the initial values.

Timer Counter Control Register (TMR0.TCCR) Number of Bits: 8 Address: 08820Ah

Bit	Symbol	Setting Value	Bit Name	Function	R/W
b2 to b0	CKS[2:0]	000/ 010	Clock select bits	These bits select the clock. 00-00: Clock input disabled 01010: Use internal clock and count at PCLK/8	R/W
b4 and b3	CSS[1:0]	00/01	Clock source select bits		R/W
b7	TMRIS	0	Timer reset input select bit	This bit selects the external reset detection condition. 0: Cleared at rising edge of the external reset	R/W

Timer Counter Control Register (TMR1.TCCR) Number of Bits: 8 Address: 08820Bh

Bit	Symbol	Setting Value	Bit Name	Function	R/W
b2 to b0	CKS[2:0]	000	Clock select bits	These bits select the clock. 00-00: Clock input disabled 11- - -: Count at TMR0.TCNT compare match A	R/W
b4 and b3	CSS[1:0]	00/11	Clock source select bits		R/W
b7	TMRIS	0	Timer reset input select bit	This bit selects the external reset detection condition. 0: Cleared at rising edge of the external reset	R/W

Time Constant Register A (TMR0.TCORA, TMR1.TCORA)

Number of Bits: 8 Addresses: 088204h, 088205h

TCORA is an 8-bit readable/writable register.

The value of the TCORA register is constantly compared with the TCNT counter value. When a match is detected, the compare match A signal is set to 1. Note that no comparison is performed while data is being written to the TCORA register.

The timer output from the TMO0 and TMO1 pins can be controlled by means of the compare match A signal and the settings of bits OSA1 and OSA0 in TCSR.

Time Constant Register B (TMR0.TCORB)

Number of Bits: 8 Address: 088206h

TCORB is an 8-bit readable/writable register.

The value of the TCORB register is constantly compared with the TCNT counter value. When a match is detected, the compare match B signal is set to 1. Note that no comparison is performed while data is being written to the TCORB register. The timer output from the TMO0 pin can be controlled by means of the compare match B signal and the settings of bits OSB1 and OSB0 in TCSR.

Timer Control Register (TMR0.TCR)

Number of Bits: 8 Address: 088200h

Bit	Symbol	Setting Value	Bit Name	Function	R/W
b4 and b3	CCLR [1:0]	01	Counter clear bits	These bits select the method by which the counter is cleared. 01: Cleared by compare match A	R/W
b5	OVIE	0	Timer overflow interrupt enable bit	This bit selects whether overflow interrupt requests (OVI0) are enabled or disabled. 0: Overflow interrupt requests (OVI0) disabled	R/W
b6	CMIEA	0	Compare match interrupt enable A bit	This bit selects whether compare match A interrupt requests (CMIA0) are enabled or disabled. 0: Compare match A interrupt requests (CMIA0) disabled	R/W
b7	CMIEB	0	Compare match interrupt enable B bit	This bit selects whether compare match B interrupt requests (CMIB0) are enabled or disabled. 0: Compare match B interrupt requests (CMIB0) disabled	R/W

Timer Control Register (TMR1.TCR) **Number of Bits: 8** **Address: 088201h**

Bit	Symbol	Setting Value	Bit Name	Function	R/W
b4 and b3	CCLR [1:0]	01	Counter clear bits	These bits select the method by which the counter is cleared. 01: Cleared by compare match A	R/W
b5	OVIE	0	Timer overflow interrupt enable bit	This bit selects whether overflow interrupt requests (OVI1) are enabled or disabled. 0: Overflow interrupt requests (OVI1) disabled	R/W
b6	CMIEA	1	Compare match interrupt enable A bit	This bit selects whether compare match A interrupt requests (CMIA1) are enabled or disabled. 0: Compare match A interrupt requests (CMIA1) disabled	R/W
b7	CMIEB	0	Compare match interrupt enable B bit	This bit selects whether compare match B interrupt requests (CMIB1) are enabled or disabled. 0: Compare match B interrupt requests (CMIB1) disabled	R/W

Timer Control/Status Register (TMR0.TCSR) **Number of Bits: 8** **Address: 088202h**

Bit	Symbol	Setting Value	Bit Name	Function	R/W
b1 and b0	OSA[1:0]	01	Output select bits A	These bits select the output method when compare match A occurs. 01: 0 output	R/W
b3 and b2	OSB[1:0]	10	Output select bits B	These bits select the output method when compare match B occurs. 10: 1 output	R/W
b4	ADTE	0	A/D trigger enable bit	This bit enables or disables A/D converter start requests by compare match A. 0: A/D converter start requests by compare match A disabled	R/W

Timer Counter (TMR0.TCNT, TMR1.TCNT) **Number of Bits: 8** **Addresses: 088208h, 088209h**

TCNT is an 8-bit readable/writable up-counter.

Bits CSS1, CSS0, and CKS2 to CKS0 in TCCR are used to select the clock.

The TCNT counter can be cleared by an external reset input signal, compare match A signal, or compare match B signal. The signal used for clearing is selected by bits CCLR1 and CCLR0 in TCR.

When the TCNT counter overflows (from FFh to 00h), the interrupt flag is set to 1.

The sample program clears the TCNT counter value to 0.

Interrupt Priority Register 69 (IPR69) **Number of Bits: 8** **Address: 087369h**

Bit	Symbol	Setting Value	Bit Name	Function	R/W
b2 to b0	IPR[2:0]	001	Interrupt priority level select bits	These bits specify the priority level of interrupt requests. 001: Level 1	R/W

Priority levels specified by bits IPR2 to IPR0 are used only to determine the priority of interrupt requests to the CPU, and do not affect activation requests to the DTC and DMAC.

The CPU only accepts and handles interrupt requests with a priority level higher than that specified by bits IPL2 to IPL0 in PSW.

If two or more interrupt requests are generated at the same time, their priority levels are compared with the value of bits IPR2 to IPR0. If interrupt requests of the same priority level are generated at the same time, the interrupt request with the smaller vector number takes precedence.

Interrupt Request Enable Register 16 (IER16) **Number of Bits: 8** **Address: 087216h**

The IER16 register is used to enable or disable interrupt requests.

When interrupt request enable bit 1 (IEN1) is set to 1, interrupt requests by TMR1 compare match A are enabled.

(5) Expression for calculating setting value

The expression used to calculate the setting value of the pulse_cycle argument from the pulse period to be output is shown below.

Pulse period to be output = 16 µs

Initial settings: PCLK = 50 MHz, TMR division ratio = 1/8

$$\text{pulse\_cycle} = \frac{\text{Pulse period} \times \text{PCLK} \times \text{TMR division ratio}}{2} - 1$$

$$= \frac{16\ \mu\text{s} \times 50\ \text{MHz} \times 1/8}{2} - 1$$

$$= 49$$

4.2.4 Excep_TMR1_CMI1A Function

(1) Functional overview

The Excep_TMR1_CMI1A function is an interrupt handler called by TMR1 compare match A. It stops pulse output by disabling the TMR0 and TMR1 clock inputs and changing the settings so that the signal does not change when a TMR0 compare match occurs.

(2) Arguments

None

(3) Return Values

None

(4) Description of I/O registers used

The I/O registers used by this function are shown below.

Note that the setting values shown are those used in this application note and differ from the initial values.

Timer Counter Control Register (TMR0.TCCR) Number of Bits: 8 Address: 08820Ah

Bit	Symbol	Setting Value	Bit Name	Function	R/W
b2 to b0	CKS[2:0]	000	Clock select bits	These bits select the clock. 00-00: Clock input disabled	R/W
b4 and b3	CSS[1:0]	00	Clock source select bits		R/W
b7	TMRIS	0	Timer reset input select bit	This bit selects the external reset detection condition. 0: Cleared at rising edge of the external reset	R/W

Timer Counter Control Register (TMR1.TCCR) Number of Bits: 8 Address: 08820Bh

Bit	Symbol	Setting Value	Bit Name	Function	R/W
b2 to b0	CKS[2:0]	000	Clock select bits	These bits select the clock. 00-00: Clock input disabled	R/W
b4 and b3	CSS[1:0]	00	Clock source select bits		R/W
b7	TMRIS	0	Timer reset input select bit	This bit selects the external reset detection condition. 0: Cleared at rising edge of the external reset	R/W

Timer Control/Status Register (TMR0.TCSR) **Number of Bits: 8** **Address: 088202h**

Bit	Symbol	Setting Value	Bit Name	Function	R/W
b1 and b0	OSA[1:0]	00	Output select bits A	These bits select the output method when compare match A occurs. 00: No change	R/W
b3 and b2	OSB[1:0]	00	Output select bits B	These bits select the output method when compare match B occurs. 00: No change	R/W
b4	ADTE	0	A/D trigger enable bit	This bit enables or disables A/D converter start requests by compare match A. 0: A/D converter start requests by compare match A disabled	R/W

4.3 Flowcharts

Figure 5 shows flowcharts of the main function and Excep_TMR1_CMI1A function (interrupt function), and figure 6 shows a flowchart of the init_pulse function.

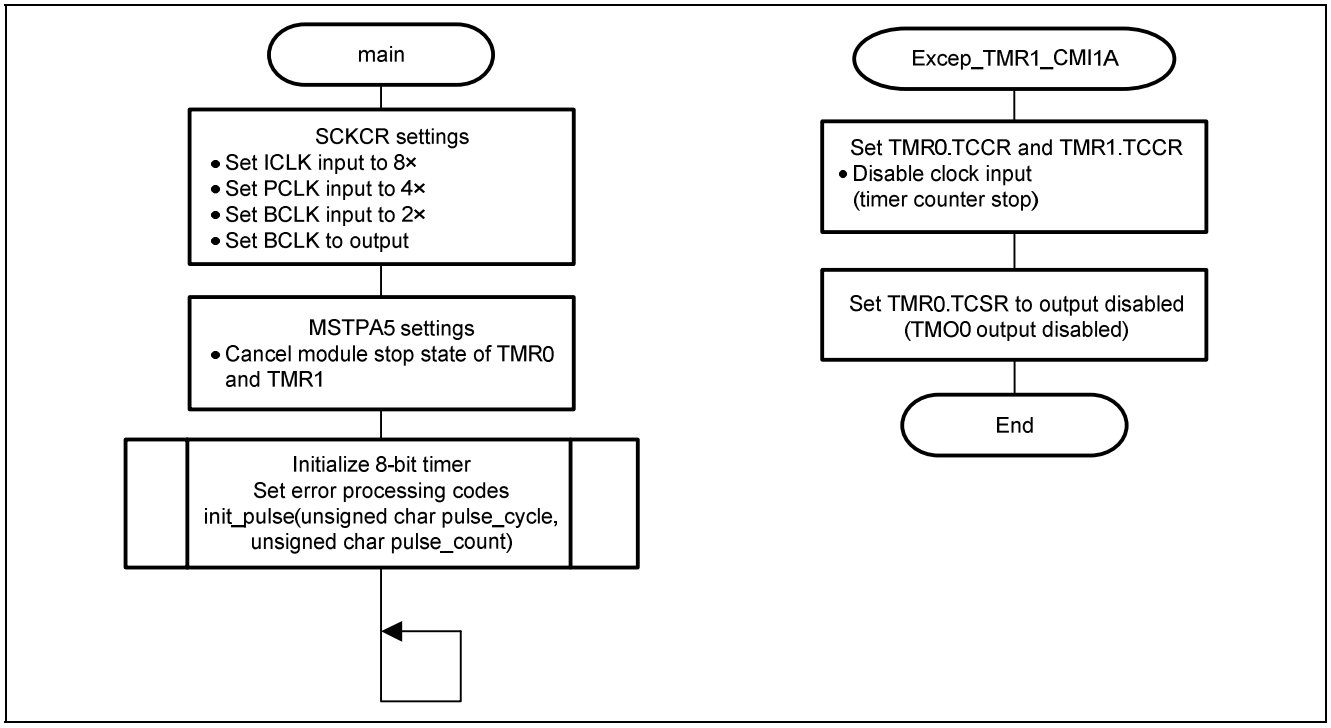


Figure 5 Flowcharts of main Function and Excep_TMR1_CMI1A Function

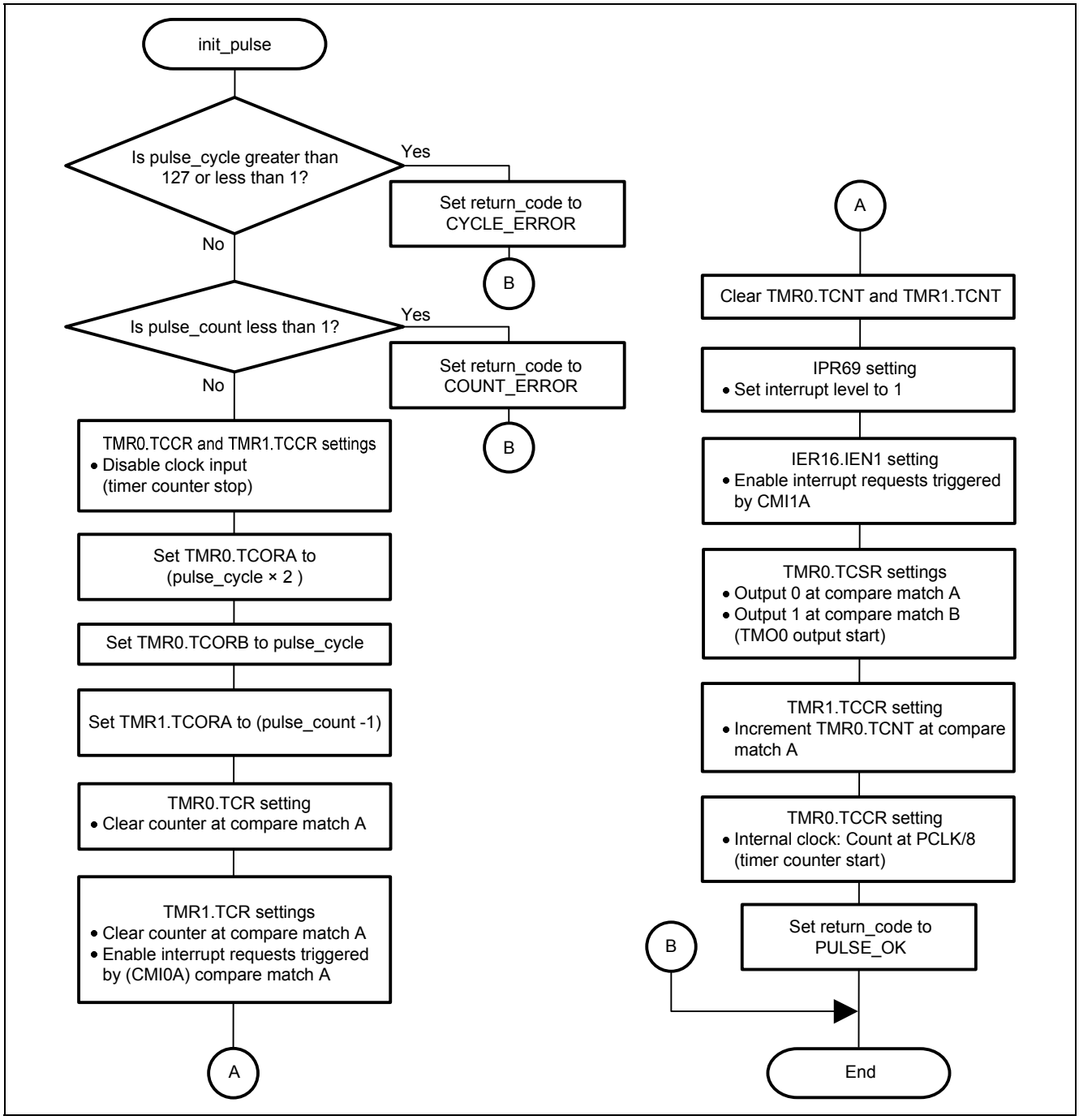


Figure 6 Flowchart of init_pulse Function

5. Operation Confirmation Environment

Table 3 shows the environment for confirming the operation of the example program.

Table 3 Operation Confirmation Environment

Item	Name
Device	RX610 (R5F56108VNFP)
Board	Evaluation board
Power supply voltage	5.0 V (CPU operating voltage: 3.3 V)
Input clock	12.5 MHz (ICLK = 100 MHz, PCLK = 50 MHz, BCLK = 25 MHz)
Operating temperature	Room temperature
HEW	Version 4.07.00.007
Toolchain	RX Standard Toolchain (V.1.0.0.0) RX Family C/C++ Compile Driver V.1.00.00.001 RX Family C/C++ Compiler V.1.00.00.001 RX Family Assembler V.1.00.00.001 Optimizing Linkage Editor V.10.00.00.001 RX Family C/C++ Standard Library Generator V.1.00.00.001
Debugger	RX E20 SYSTEM V.1.00.00.000

6. Reference Documents

- Hardware Manual
  RX610 Group Hardware Manual
  (The latest version can be downloaded from the Renesas Electronics Web site.)
- Development Environment Manual
  RX Family C/C++ Compiler Package User's Manual
  (The latest version can be downloaded from the Renesas Electronics Web site.)
- Technical Updates
  (The latest information can be downloaded from the Renesas Electronics Web site.)

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   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
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3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

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5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

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