RX210 Group

Setting External Bus Pins

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Abstract

This document describes external bus pins and connection examples using the external bus with a 100-pin package in the RX210 Group.

Products

RX210 Group (100-pin package)

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. External Bus Pins

1.1 External Bus Pins According to Data Bus Width

The external bus pins used vary according to the data bus width of the separate bus or multiplexed bus.

Table 1.1 lists the Pins Used According to Bus Type and Data Bus Width.

Table 1.1 Pins Used According to Bus Type and Data Bus Width (1)

External Bus Pin	8-Bit Separate Bus	16-Bit Separate Bus	8-Bit Multiplexed Bus
A0 to A7 (2)	Available	Available	N/A
A8 to A15	Available (4)	Available (4)	Available (4)
A16 to A23	Available (4)	Available (4)	Available (4)
D0 to D7 (A0/D0 to A7/D7)	Available	Available	Available
D8 to D15 (A8/D8 to A15/D15)	N/A	Available	N/A
BC0# (2)	Available	Available	Available
BC1#	N/A	Available	N/A
CS0#	Available	Available	Available
CS1#	Available	Available	Available
CS2#	Available	Available	Available
CS3#	Available	Available	Available
RD#	Available	Available	Available
WR0#/WR# (3)	Available	Available	Available
WR1#	N/A	Available	N/A
ALE	N/A	N/A	Available
WAIT#	Available	Available	Available

Notes:

1. The 16-bit multiplexed bus is also supported though it is not described in the application note.
2. The A0 and BC0# pin share the same pin. A0 pin is enabled when in byte strobe mode and BC0# pin is enabled when in single write strobe mode. The mode used is specified depending on the area. Note that the 8-bit external bus width cannot be set in single write strobe mode.
3. The WR0# signal and WR# signal are identical. The WR0# signal is particularly referred to as WR# in single write strobe mode.
4. Select an address pin used depending on the connected external memory size.

1.2 Pins Used

Pins not used as external bus pins can be used as general ports.

Table 1.2 and Table 1.3 list Settings when Pins are Used as External Bus Pins or General Ports. The Pin No. in the tables indicates pin numbers of the LQFP package. Figure 1.1 shows Pin Assignments of LQFP Package, Figure 1.2 shows Pin Assignments of TFLGA Package for the Separate Bus, and Figure 1.3 shows Pin Assignments of TFLGA Package for the Multiplexed Bus.

Table 1.2 Settings when Pins are Used as External Bus Pins or General Ports (1/2)

Pin No.	Used as General Port			Used as External Bus Pin		
	General Port	Register Setting	Input/ Output	External Bus Pin	Register Setting	Input/ Output
24	P24	PFCSE.CS4E = 0	I/O	CS0#	PFCSE.CS4E = 1	Output
23	P25	PFCSE.CS5E = 0	I/O	CS1#	PFCSE.CS5E = 1	Output
22	P26	PFCSE.CS2E = 0	I/O	CS2#	PFCSE.CS2E = 1	Output
21	P27	PFCSE.CS3E = 0	I/O	CS3#	PFCSE.CS3E = 1	Output
44	P50	—	(Note 1)	WR#/WR0#	—	Output
43	P51	PFBCR0.WR1BC1E = 0 PFBCR1.WAITS[1:0] = 00b or 01b or 10b	I/O	WR1#/ BC1#	PFBCR0.WR1BC1E = 1 PFBCR1.WAITS[1:0] = 00b or 01b or 10b	Output
				WAIT#	PFBCR0.WR1BC1E = 0 PFBCR1.WAITS[1:0] = 11b	Input (2)
42	P52	—	(Note 1)	RD#	—	Output
41	P53	—	(Note 1)	BCLK	—	Output
40	P54	PFBCR1.ALEOE = 0	I/O	ALE	PFBCR1.ALEOE = 1	Output
39	P55	PFBCR1.WAITS[1:0] = 10b or 11b	I/O	WAIT#	PFBCR1.WAITS[1:0] = 00b or 01b	Input (2)
70	PA0	PFBCR0.ADRLE = 0	I/O	A0/BC0#	PFBCR0.ADRLE = 1	Output
69 to 63	PA1 to PA7	PFBCR0.ADRLE = 0	I/O	A1 to A7	PFBCR0.ADRLE = 1	Output
61	PB0	PFAOE0.A8E = 0	I/O	A8	PFAOE0.A8E = 1	Output
59	PB1	PFAOE0.A9E = 0	I/O	A9	PFAOE0.A9E = 1	Output
58	PB2	PFAOE0.A10E = 0	I/O	A10	PFAOE0.A10E = 1	Output
57	PB3	PFAOE0.A11E = 0	I/O	A11	PFAOE0.A11E = 1	Output
56	PB4	PFAOE0.A12E = 0	I/O	A12	PFAOE0.A12E = 1	Output
55	PB5	PFAOE0.A13E = 0	I/O	A13	PFAOE0.A13E = 1	Output
54	PB6	PFAOE0.A14E = 0	I/O	A14	PFAOE0.A14E = 1	Output
53	PB7	PFAOE0.A15E = 0	I/O	A15	PFAOE0.A15E = 1	Output

Notes:
1. When using an external bus, ports P50, P52, and P53 cannot be used as general I/O ports.
2. When the specified port is not used as the WAIT# pin, the port can be used as a general input port by setting the external wait enable bit in the CSn mode register (CSnMOD.EWENB) to 0 (external wait is disabled).

Table 1.3 Settings when Pins are Used as External Bus Pins or General I/O Ports (2/2)

Pin No.	Used as General Port			Used as External Bus Pin		
	General Port	Register Setting	Input/ Output	External Bus Pin	Register Setting	Input/ Output
52	PC0	PFAOE0.A16E = 0	I/O	A16	PFAOE0.A16E = 1	Output
51	PC1	PFAOE0.A17E = 0	I/O	A17	PFAOE0.A17E = 1	Output
50	PC2	PFAOE0.A18E = 0	I/O	A18	PFAOE0.A18E = 1	Output
49	PC3	PFAOE0.A19E = 0	I/O	A19	PFAOE0.A19E = 1	Output
48	PC4	PFAOE1.A20E = 0 PFCSE.CS7E = 0	I/O	A20	PFAOE1.A20E = 1 PFCSE.CS7E = 0	Output
				CS3#	PFAOE1.A20E = 0 PFCSE.CS7E = 1	Output
47	PC5	PFAOE1.A21E = 0 PFCSE.CS6E = 0 PFBCR1.WAITS[1:0] = 00b or 01b or 11b	I/O	A21	PFAOE1.A21E = 1 PFCSE.CS6E = 0 PFBCR1.WAITS[1:0] = 00b or 01b or 11b	Output
				CS2#	PFAOE1.A21E = 0 PFCSE.CS6E = 1 PFBCR1.WAITS[1:0] = 00b or 01b or 11b	Output
				WAIT#	PFAOE1.A21E = 0 PFCSE.CS6E = 0 PFBCR1.WAITS[1:0] = 10b	Input (2)
46	PC6	PFAOE1.A22E = 0 PFCSE.CS0E = 0	I/O	A22	PFAOE1.A22E = 1 PFCSE.CS1E = 0	Output
				CS1#	PFAOE1.A22E = 0 PFCSE.CS1E = 1	Output
45	PC7	PFAOE1.A23E = 0 PFCSE.CS0E = 0	I/O	A23	PFAOE1.A23E = 1 PFCSE.CS0E = 0	Output
				CS0#	PFAOE1.A23E = 0 PFCSE.CS0E = 1	Output
79 to 86	PD0 to PD7	—	(Note 1)	D0 to D7	—	I/O
71 to 78	PE0 to PE7	PFBCR0.DHE = 0	I/O	D8 to D15	PFBCR0.DHE = 1	I/O

Notes:
1. When using an external bus, ports PD0 to PD7 cannot be used as general I/O ports.
2. When the specified port is not used as the WAIT# pin, the port can be used as a general input port by setting the external wait enable bit in the CSn mode register (CSnMOD.EWENB) to 0 (external wait is disabled).

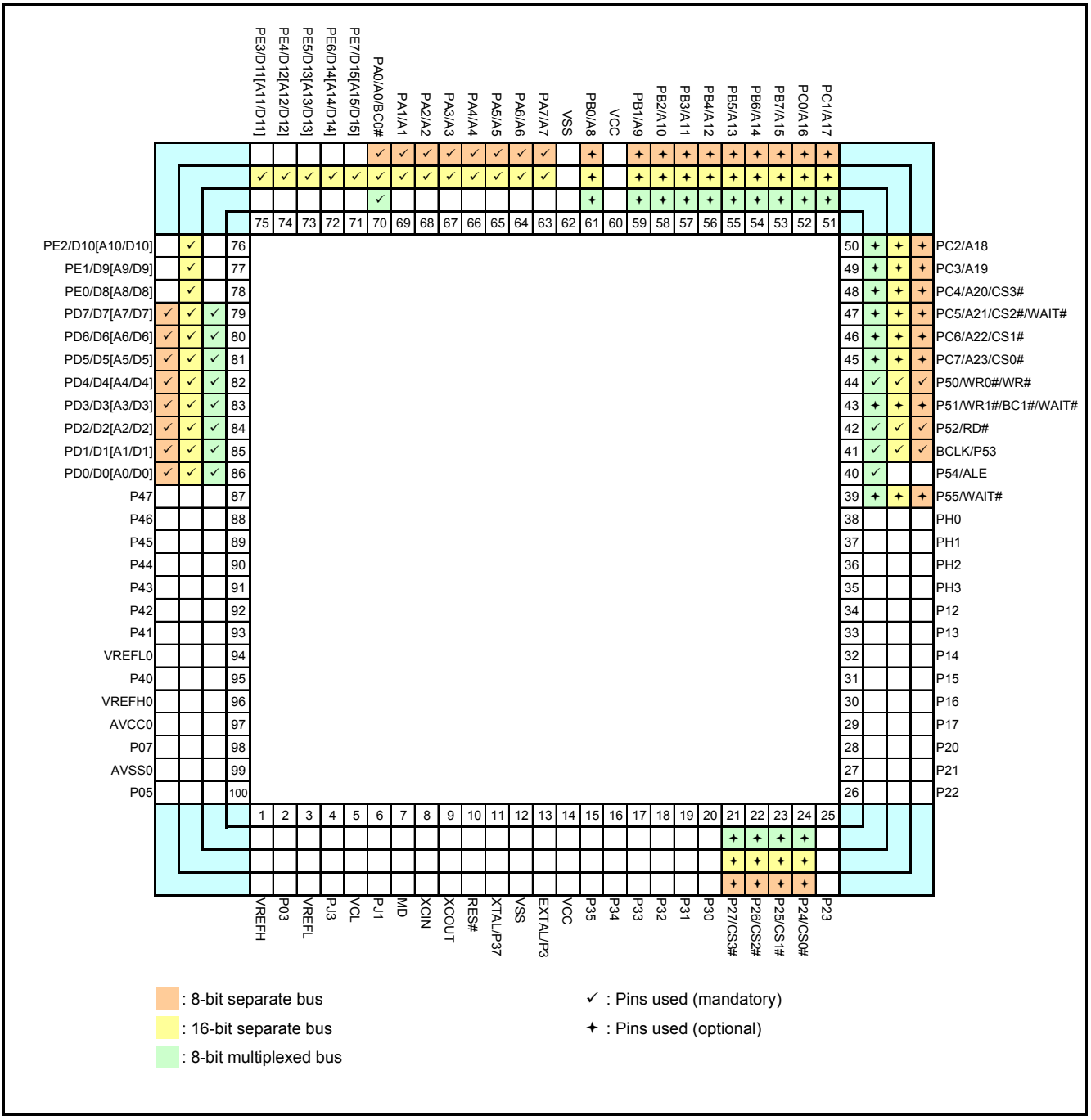


Figure 1.1 Pin Assignments of LQFP Package

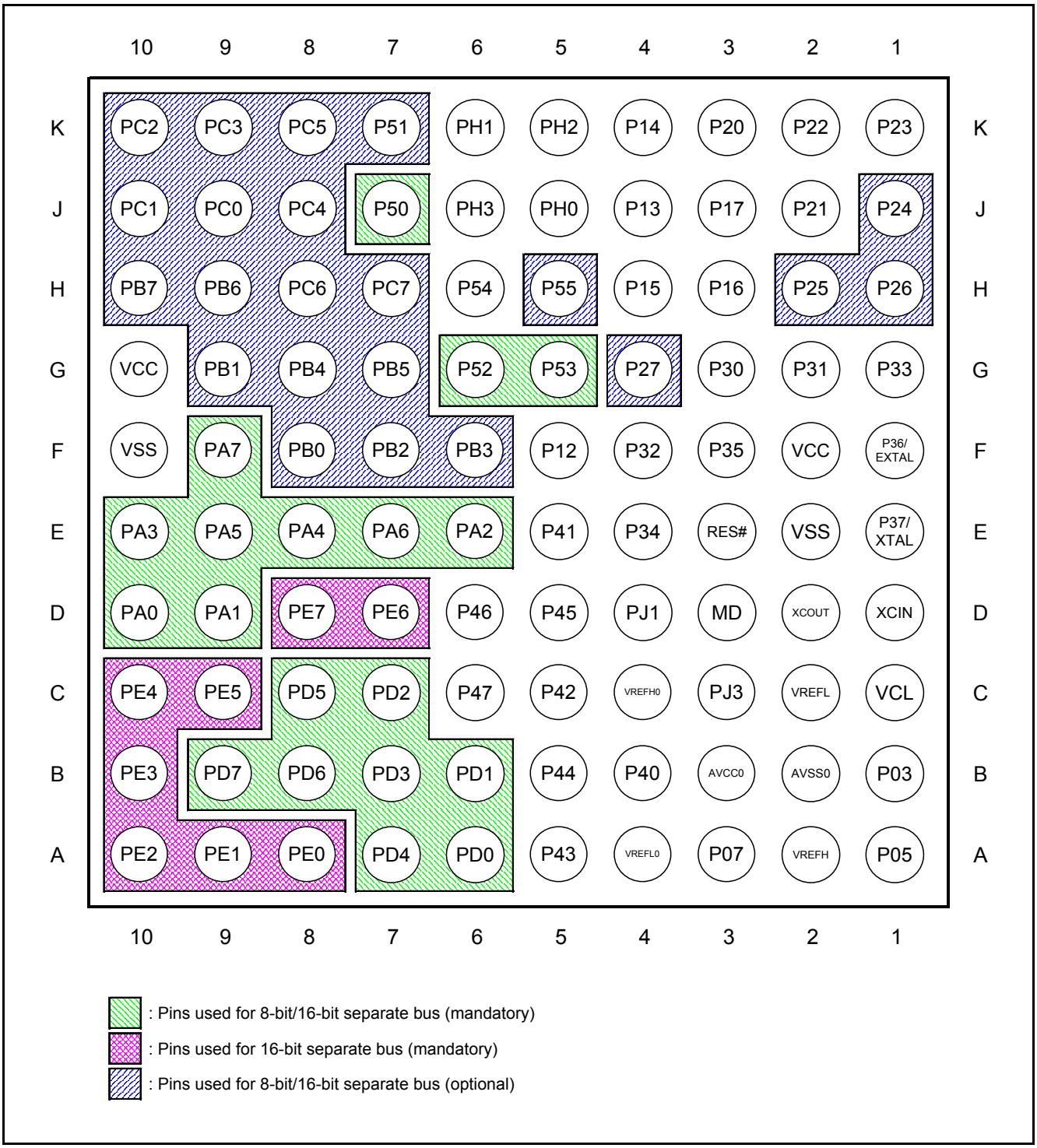


Figure 1.2 Pin Assignments of TFLGA Package for the Separate Bus

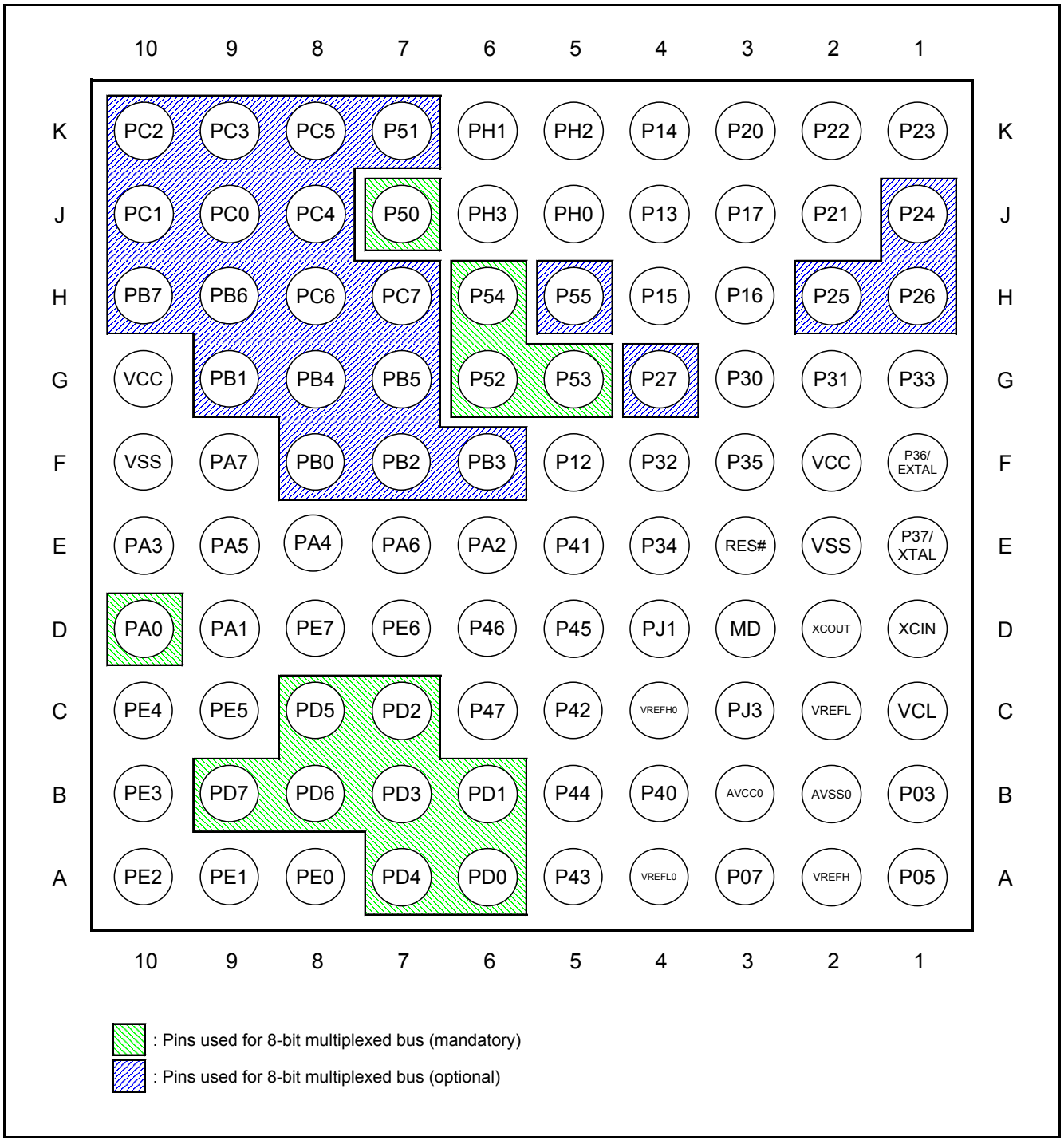
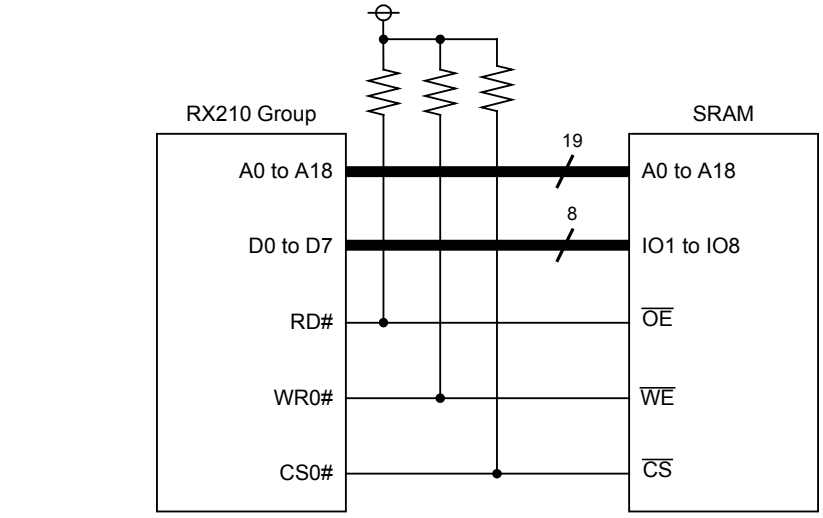


Figure 1.3 Pin Assignments of TFLGA Package for the Multiplexed Bus

2. Connecting the External Bus

2.1 Connecting the 8-Bit Separate Bus

Figure 2.1 shows an example of connecting the RX210 Group MCU to an external device with the separate bus (data bus width is 8 bits).

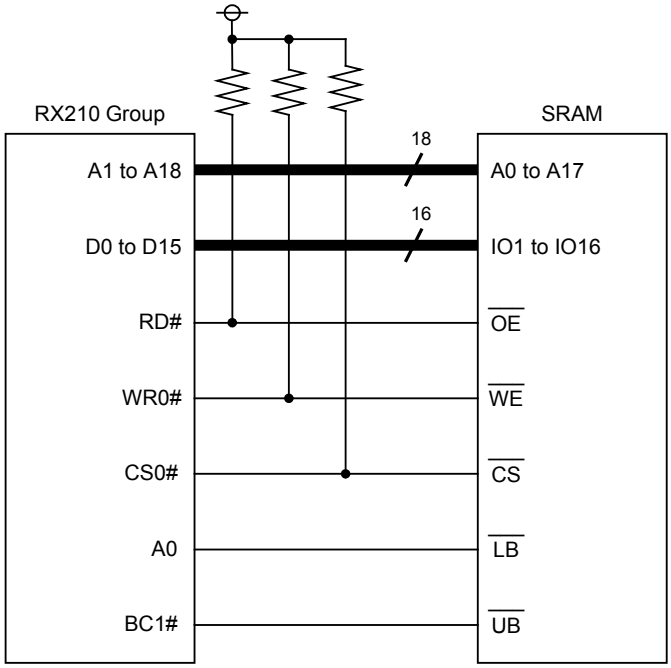


Note:
1. Pull-up resistors on the buses are not shown here. However it is recommended to add a pull-up resistor to each bus signal line.

Figure 2.1 Connection Example for the 8-Bit Separate Bus

2.2 Connecting the 16-Bit Separate Bus

Figure 2.2 shows an example of connecting the RX210 Group MCU to an external device with the separate bus (data bus width is 16 bits).

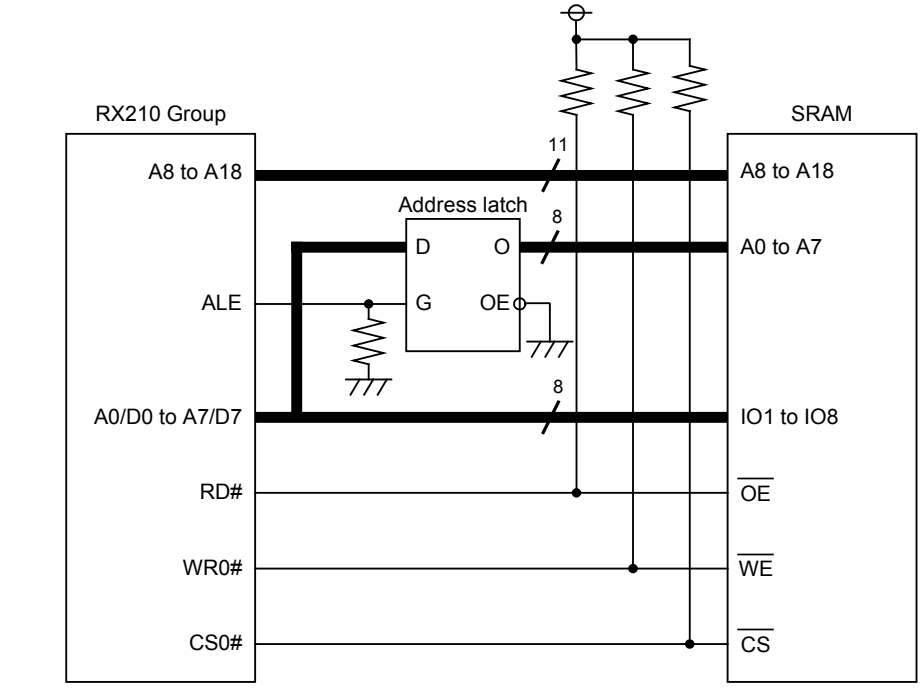


Note:
1. Pull-up resistors on the buses are not shown here. However it is recommended to add a pull-up resistor to each bus signal line.

Figure 2.2 Connection Example for the 16-Bit Separate Bus

2.3 Connecting the 8-Bit Multiplexed Bus

Figure 2.3 shows an example of connecting the RX210 Group MCU to an external device with the multiplexed bus (data bus width is 8 bits).



Note:
1. Pull-up resistors on the buses are not shown here. However it is recommended to add a pull-up resistor to each bus signal line.

Figure 2.3 Connection Example for the 8-Bit Multiplexed Bus

3. Reference Documents

User's Manual: Hardware
RX210 Group User's Manual: Hardware Rev.1.10 (R01UH0037EJ)
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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