RX210 Group

Register Write Protection Setting Example

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Abstract

This application note describes the RX210 Group microcontroller’s register write protection functions.

Product

RX210 Group

When using the code presented in this application note with a different microcontroller, modify the code according to the specifications of that microcontroller and test the code thoroughly.

Contents

1. Protection Setup Procedures

This application note describes the procedures for enabling and disabling protection functions.

1.1 Register Write Protection

Table 1.1 lists the register write protection settings and figure 1.1 shows code examples for the register write protection function.

Table 1.1 Register Write Protection Settings

Register	PRCR
Objects protected	• The following registers are protected by the PRC0 bit. SCKCR, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, HOCOCR2 • The following registers are protected by the PRC1 bit. SYSCR0, SYSCR1, SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, OPCCR, RSTCKCR, MOSCWTCR, SOSCWTCR, PLLWTCR, DPSBYCR, DPSIER0, DPSIER2, DPSIFR0, DPSIFR2, DPSIEGR0, DPSIEGR2, FHSSBYCR, LOCOWTCR2, HOCOWTCR2, MOFCR, HOCOPCR, SWRR • The following processing is protected by the PRC2 bit. Writing to 0008 0200h. • The following registers are protected by the PRC3 bit. LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR
Register modification conditions	Word access must be used to set this register. The upper byte of the set value must be A5h and the lower byte is used to set the corresponding bits. Note: When the upper byte is read, the value read will be 00h.

Correct code example

To set just the PRC0 bit to 1

```
SYSTEM.PRCR.WORD = 0xA501;
```

To set the PRC0, PRC1, and PRC3 bits to 0

```
SYSTEM.PRCR.WORD = 0xA500;
```

Wrong code example

Code that fails to set the PRC0, PRC1, and PRC3 bits to 1

```
SYSTEM.PRCR.WORD = 0xA500;  /* Since this line uses word access, */
                            /* PRC0, PRC1, and PRC3 will be set to 0. */
SYSTEM.PRCR.BIT.PRC0 = 1;   /* Since bit access is used, the setting will not be reflected in the bit values. */
SYSTEM.PRCR.BIT.PRC1 = 1;   /* Since bit access is used, the setting will not be reflected in the bit values. */
SYSTEM.PRCR.BIT.PRC3 = 1;   /* Since bit access is used, the setting will not be reflected in the bit values. */
```

Figure 1.1 Register Write Protection Code Samples

1.2 PFS Register Write Protection

Table 1.2 lists the PFS register write protection settings and figure 1.2 shows code examples that use register write protection.

Table 1.2 PFS Register Write Protection Settings

Register	PWPR
Objects protected	• The following registers are protected by the B0WI bit. PFSWE bit • The PFSWE bit protects the following registers. PnPFS register (n = 03, 05, 07, 12 to 17, 20 to 27, 30 to 34, 40 to 47, 54 to 55, A0 to A7, B0 to B7, C0 to C7, D0 to D7, E0 to E7, H0 to H3, J1, J3)
Register modification conditions	There are no restrictions on register access units. The protection is cleared by setting the B0WI bit to 0 and then setting the PFSWE bit to 1. Note, however, that setting both the B0WI and PFSWE bits at the same time by accessing in bytes does not clear the write protection. To enable protection, set the B0WI bit to 1 and the PFSWE bit to 0. Protection can be enabled by setting the B0WI and PFSWE bits at the same time by accessing in bytes.

Correct code example

Enabling or clearing PFS register protection using bit access

```
MPC.PWPR.BIT.B0WI = 0;          /* Protection can be cleared by setting in bit units. */
MPC.PWPR.BIT.PFSWE = 1;
/*******************************/
/* Setting the PFS register */
/*******************************/
MPC.PWPR.BIT.PFSWE = 0          /* Protection can be enabled by setting in bit units. */
MPC.PWPR.BIT.B0WI = 1;
```

Enabling or clearing PFS register protection using byte access

```
MPC.PWPR.BYTE = 0x00;           /* Protection can be cleared by setting in byte units if the setting order is correct. */
MPC.PWPR.BYTE = 0x40;
/*******************************/
/* Setting the PFS register */
/*******************************/
MPC.PWPR.BYTE = 0x80;           /* For enabling protection, two bits can be set at the same time. */
```

Wrong code example

Code that fails to enable or clear PFS register protection

```
MPC.PWPR.BYTE = 0x40;           /* Since it is not possible to clear protection by setting the 2 bits at the same time. */
                                /* This one line cannot clear the protection. */
/*******************************/
/* Setting the PFS register */
/*******************************/
MPC.PWPR.BIT.B0WI = 1;          /* Since this line enables PFSWE protection, */
MPC.PWPR.BIT.PFSWE = 0          /* the operation on this line is not reflected and the PFSWE bit remains 1. */
```

Figure 1.2 PFS Register Write Protection Code Examples

1.3 MST/TRS Write Protection

Table 1.3 lists the MST/TRS register write protection settings and figure 1.3 shows code examples that use MST/TRS register write protection.

Table 1.3 MST/TRS Write Protection Settings

Register	ICMR1.MTWP bit
Objects protected	ICCR2.MST bit ICCR2.TRS bit
Register modification conditions	There are no restrictions on register access sizes. Writing the protection target bit is enabled when the bit is set to 1, and disabled when the bit is set to 0.

Correct code example

Enabling or clearing PFS register protection using bit access

```
RIIC.ICMR1.BIT.MTWP = 1;          /* Protection can be cleared by setting in bit units. */

/* Modifying the ICCR2.MST and ICCR2.TSR bits is possible. */

RIIC.ICMR1.BIT.MTWP = 0;          /* Protection can be enabled by setting in bit units. */
```

Figure 1.3 MST/TRS Write Protection Code Examples

1.4 ROM/E2 Data Flash Write/Erase Protection

The RX210 Group microcontrollers provide a function that protects the ROM/E2 data flash from writing or erasing.

Table 1.4 lists the flash memory write/erase related registers and figure 1.4 shows code examples that use flash memory write/erase protection.

Table 1.4 Flash Memory Write/Erase Related Registers

Register	FWEPROR
Objects protected	• The following operations are protected by the FWEPROR.FLWE bits. Flash memory write and erase operations
Register modification conditions	• FWEPROR.FLWE bits There are no restrictions on register access sizes. Flash memory write and erase operations are enabled when the FWEPROR.FLWE bits are set to 01b, and disabled when those bits are set to 00b, 10b, or 11b.

Sample code

Enabling flash memory write/erase using bit access

```
FLASH.FWEPROR.BIT.FLWE = 0x01;          /* Uses bit access to enable writing. */
```

Disabling flash memory write/erase using byte access

```
FLASH.FWEPROR.BYTE = 0x00;              /* Uses byte access to enable writing. */
```

Figure 1.4 Flash Memory Write/Erase Protection Code Examples

1.5 ROM Data Flash Write/Erase Protection with the Lock Bit

The RX210 Group microcontrollers can protect ROM data flash from write or erase operations by enabling the lock bit.

Table 1.5 lists the lock bit based ROM data flash write/erase protection related registers and figure 1.5 shows code examples that use this lock bit based ROM data flash write/erase protection.

Table 1.5 Related Registers of ROM Data Flash Write/Erase Protection with the Lock Bit

Register	FENTRYR FPROTR
Objects protected	• The following bits are protected by the FENTRYR register. FPROTR.FPROTCN bit can be modified when the FENTRYR register is any value other than 0000h. • The following operations are protected by the FPROTR.FPROTCN bit ROM data flash write/erase protection with the lock bit.
Register modification conditions	• FENTRYR register Word access must be used to write this register. Furthermore, when the upper byte is 0xAA, the value written will be reflected in the register. When the internal ROM is disabled, the FENTRYR register will be 0000h and writing will not be possible. [Conditions for setting the FENTRY0 bit to 1 (ROM P/E mode)] → The FENTRYR register must be 0000h. [Conditions for setting the FENTRY0 bit to 0 (ROM read mode)] → Writing a word whose upper byte is a value other than 0xAA in word access mode → Writing to the FENTRYR register when the FENTRYR register has a value other than 0000h. • FPROTR register Word access must be used to write this register. Furthermore, when the upper byte is 0x55, the value written will be reflected in the register. [Conditions for setting the FPROTCN bit to 1] → When the FENTRYR register has a value other than 0000h, using word access to write 1 to the FPROTCN bit and 0x55 to the upper byte at the same time. [Conditions for setting the FPROTCN bit to 0] (The FPROTCN bit will become 0 if any of the following apply.) → Writing a value other than 0x55 to the upper byte using word access → Using word access to write 0 to the FPROTCN bit and 0x55 to the upper byte at the same time. → The FENTRYR register becomes 0000h.

Code example

When the lock bit is enabled

```
FLASH.FENTRYR.WORD = 0xAA01; /* May only be accessed using word access */
FLASH.FPROTR.WORD = 0x5501;    /* Modification is possible since the FENTRYR register has a value other than 0000h. */
```

When the lock bit is disabled

```
FLASH.FENTRYR.WORD = 0xAA00;  /* The FPROTR register can be set to 0000h by setting the FENTRYR register to 0000h. */
```

Figure 1.5 Code Examples of ROM Data Flash Write/Erase Protection with the Lock Bit

1.6 E2 Data Flash Write/Erase Protection

The RX210 Group microcontrollers support write/erase protection of specific blocks in the E2 data flash memory.

Table 1.6 lists the E2 data flash write/erase related registers and figure 1.6 shows flash memory write/erase protections code samples.

Table 1.6 E2 Data Flash Write/Erase Protection Related Registers

Register	DFLWE0
Objects protected	• The following operations are protected by the DFLWE0.DBWE00 bit. Writing/erasing the DB00 to DB15 blocks. • The following operations are protected by the DFLWE0.DBWE01 bit. Writing/erasing the DB16 to DB31 blocks. • The following operations are protected by the DFLWE0.DBWE02 bit. Writing/erasing the DB32 to DB47 blocks. • The following operations are protected by the DFLWE0.DBWE03 bit. Writing/erasing the DB48 to DB63 blocks.
Register modification conditions	• DFLWE0 Word access must be used to write this register. Furthermore, when the upper byte is 0x1E, the values of DBWE00 to DBWE03 can be modified.

Correct code example

Setting the DBWE00 and DBWE01 bits to 1

```
FLASH.DFLWE0.WORD = 0x1E03;   /* Since this performs a word access with the upper byte being 0x1E, */
                              /* the set value will be reflected in the register. */
```

Wrong code example

Setting the DBWE00 and DBWE01 bits to 1

```
FLASH.DFLWE0.WORD = 0x1E00;
FLASH.DFLWE0.BIT.DBWE00 = 1;  /* Since bit access is used, the set value is not reflected in the register. */
FLASH.DFLWE0.BIT.DBWE01 = 1;  /* Like the previous line, the set value is not reflected in the register. */
```

Figure 1.6 Flash Memory Write/Erase Protection Code Examples

1.7 E2 Data Flash Read Protection

The RX210 Group microcontrollers support read protection of specific blocks in the E2 data flash memory.

Table 1.7 lists the E2 data flash read related registers and figure 1.7 shows flash memory read protections code samples.

Table 1.7 E2 Data Flash Read Related Registers

Register	DFLRE0
Objects protected	• The following operations are protected by the DFLRE0.DBRE00 bit. Reading the DB00 to DB15 blocks. • The following operations are protected by the DFLRE0.DBRE01 bit. Reading the DB16 to DB31 blocks. • The following operations are protected by the DFLRE0.DBRE02 bit. Reading the DB32 to DB47 blocks. • The following operations are protected by the DFLRE0.DBRE03 bit. Reading the DB48 to DB63 blocks.
Register modification conditions	Word access must be used to write this register. Furthermore, when the upper byte is 0x2D, the values of DBRE00 to DBRE03 can be modified.

Correct code example

Setting the DBRE00 and DBRE01 bits to 1

```
FLASH.DFLEE0.WORD = 0x2D03;    /* Since this performs a word access with the upper byte being 0x2D, */
                               /* the set value will be reflected in the register. */
```

Wrong code example

Setting the DBRE00 and DBRE01 bits to 1

```
FLASH.DFLRE0.WORD = 0x2D00;
FLASH.DFLRE0.BIT.DBRE00 = 1;   /* Since bit access is used, the set value is not reflected in the register. */
FLASH.DFLRE0.BIT.DBRE01 = 1;   /* Like the previous line, the set value is not reflected in the register. */
```

Figure 1.7 E2 Data Flash Read Protection Code Examples

2. Sample Code

The sample code can be downloaded from the Renesas Electronics Corporation web site.

3. Reference Documents

Hardware manual
RX210 User's Manual: Hardware, Revision 1.10
(Download the latest version of this manual from the Renesas Electronics Corporation web site.)

Technical updates and technical news
(The latest technical information can be downloaded from the Renesas Electronics Corporation web site.)

C compiler manual
RX210 C Compiler Package, Version 1.02
C Compiler User's Manual, Revision 1.00
(Download the latest version of this manual from the Renesas Electronics Corporation web site.)

Website and Support

Renesas Electronics website
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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

Colophon 2.2