RL78/G23

SNOOZE Mode Sequencer Application Guide

Introduction

This application note describes the advantages of using the SNOOZE mode sequencer (SMS) mounted on the RL78/G23.

Target Device

RL78/G23

When applying the sample program covered in this application note to another microcomputer, modify the program.

according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Overview of the SNOOZE Mode Sequencer (SMS)

The SMS sequentially executes a maximum of 32 processes out of 21 types of processes including arithmetic operations, branch instructions, and control of peripheral functions (such as timers and serial communication). The SMS starts when triggered by an interrupt request signal from a peripheral function or an output signal from the ELCL. The SMS can perform processes independent of the CPU, which means the SMS can run when the CPU is in standby mode. The SMS requires less operating current compared to the CPU. By assigning some of the CPU's processes to the SMS, system power consumption is decreased.

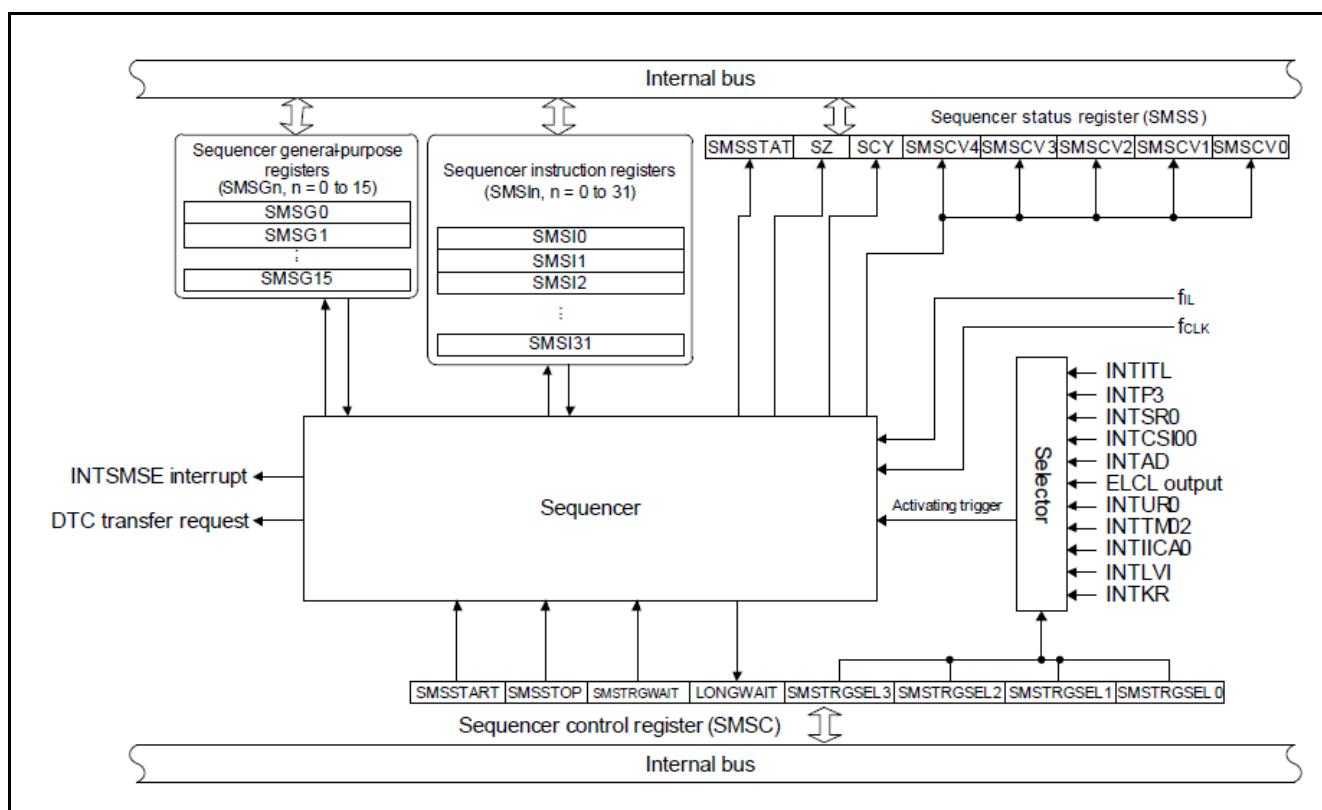## 1.1 Configuration

Figure1.1 is a block diagram of the SMS.

Figure 1.1　Block Diagram of the SMS

1.2 Features

The features of the SMS are as follows.

● The SMS can sequentially perform a maximum of 32 preset processes.

You can combine any of 21 types of processes to execute varieties of tasks. For details about the available processes, see Table 1.3   SMS processing list (1/2 and Table 1.4   SMS processing list (2/2).

● You can select the timing to start the SMS.

You can select the timing to start the SMS from 11 activation triggers (including the end of A/D conversion, interval detection interrupt, and completion of data reception by the UART). For the types of activation triggers, see section 1.3.1 Activation trigger.

● The system can reduce power consumption.

The SMS requires less operating current compared to the CPU and can operate while the CPU is in standby mode. If the target process can be performed by the SMS, the system can reduce power consumption by letting the SMS perform the process while placing the CPU in SNOOZE mode (stopping clock signals being applied to the CPU).

If you want the SMS to wait, combine wait processing and conditional wait processing 1 or 2. When the wait time is predictable (such as the wait time for UART transmission processing), combining wait processing with conditional wait processing 1 or 2 (instead of performing conditional wait processing 1 or 2 alone) reduces required operating current.

● The SMS can control peripheral functions.

The SMS can transfer data between its sequencer general-purpose registers and the SFRs/RAM. Using this capability, the SMS can control the peripheral functions. For example, the SMS can transfer data from an SFR via its sequencer general-purpose register to the RAM. This means that the result of A/D conversion or the data received by the UART or CSI can be stored in the RAM.

● The SMS can calculate data.

The SMS can add and subtract the data stored in the sequencer general-purpose registers. The SMS can also perform division by powers of 2 by right-shifting data. For example, the SMS can calculate the average of A/D conversion results.

● The SMS can judge data and branch processing.

The SMS can judge data through comparison and branch processing based on the result of the judgement. By using branches, the SMS can repeat the same task.

● The SMS can perform wait processing.

By specifying the low-speed on-chip oscillator clock as the clock for wait processing, the SMS can wait up to 500 ms. The SMS can also wait until the value of a bit in an SFR/RAM changes. For example, the SMS can wait until A/D conversion ends or data reception by the UART or CIS completes.

● At the end of SMS processing, you can choose to restore the CPU from standby mode or hold the CPU in standby mode.

You can choose whether to issue an interrupt request signal when the SMS ends processing. This feature allows you to select whether to release the CPU from standby mode or keep the CPU in standby mode when the SMS ends processing.

● The SMS can directly start the data transfer controller (DTC).

By sending a request signal to the DTC, the SMS can start the DTC. With the DTC, the SMS can execute a wider variety of tasks.

1.3   Setting

1.3.1   Activation trigger

Table 1.1 shows a list of SMS activation triggers.

Table 1.1   List of activation triggers

Classification	Activation trigger
Timer	Interval detection interrupt (INTITL) from the 32-bit interval timer
	Timer channel 02 count or capture end interrupt (INTTM02)
Communication	UART0 reception transfer end interrupt (INTSR0)
	UARTA0 reception transfer end interrupt (INTUR0)
	CSI00 transfer end interrupt (INTCSI00)
	IICA0 communication end interrupt (INTIICA0)
Voltage detection	A/D conversion end interrupt (INTAD)
	Voltage detection interrupt (INTLVI)
Pin input	Pin input edge detection interrupt (INTP3)
	Key return signal detection interrupt (INTKR)
Other	ELCL output signal

1.3.2   Selection of operating clock

Table 1.2 shows the SMS operating clock and operating status. SMS operates with the clock selected for the CPU clock.

Table 1.2   Operating clock and operating status

Operation clock	HALT Mode	STOP Mode	SNOOZE Mode
High-speed on-chip oscillator clock	Operable	The activating trigger for the SNOOZE mode sequencer can be accepted	Operable
Middle-speed on-chip oscillator clock	Operable	The activating trigger for the SNOOZE mode sequencer can be accepted	Operable
Low-speed on-chip oscillator clock	Operable	Operation disabled	Operation disabled
High-speed system clock	Operable	Operation disabled	Operation disabled
Subsystem clock	Operable	Operation disabled	Operation disabled

1.3.3 Commands for Use in Processing by the Sequencer

Table 1.3 and Table 1.4 list the names and descriptions of the 21 types of processes the SMS can perform. You can combine a maximum of 32 processes for the SMS.

Table 1.3   SMS processing list (1/2)

Processing	Operation
8-bit data transfer 1	Transfers the 8-bit data stored in a sequencer general-purpose register to the specified address.
8-bit data transfer 2	Transfers the 8-bit data stored at the specified address to a sequencer general-purpose register.
16-bit data transfer 1	Transfers the 16-bit data stored in a sequencer general-purpose register to the specified address.
16-bit data transfer 2	Transfers the 16-bit data stored at the specified address to a sequencer general-purpose register.
1-bit data setting	Sets the specified bit at the specified address to 1.
1-bit data clearing	Clears the specified bit at the specified address (set to 0).
1-bit data transfer	Stores the value of the specified bit at the specified address in the SCY flag.

Word addition	Adds the 16-bit data value stored in sequencer general-purpose register n and the 16-bit data value stored in sequencer general-purpose register m, and stores the result in sequencer general-purpose register n.
	  Sets the SZ flag when the result of addition is 0000H.
	  Sets the SCY flag when the result of addition has a carry.

Word subtraction	Subtracts the 16-bit data value stored in sequencer general-purpose register m from the 16-bit data value stored in sequencer general-purpose register n, and stores the result in sequencer general-purpose register n.
	  Sets the SZ flag when the result of subtraction is 0000H.
	  Sets the SCY flag when the result of subtraction has a borrow.

Word comparison	Subtracts the 16-bit data value stored in sequencer general-purpose register m from the 16-bit data value stored in sequencer general-purpose register n. Does not store the result.
	  Sets the SZ flag when the result of subtraction is 0000H.
	  Sets the SCY flag when the result of subtraction has a borrow.

Logical shift right	Right-shifts the value in a sequencer general-purpose register by 1 bit. Stores 0 in bit 15 and the value of bit 0 in the SCY flag.
Branch 1 (SCY = 1)	Branches to the sequencer instruction register of the relative address specified by the first and second operands when the SCY flag is set. Executes the next process when the SCY flag is cleared.
Branch 2 (SCY = 0)	Branches to the sequencer instruction register of the relative address specified by the first and second operands when the SCY flag is cleared. Executes the next process when the SCY flag is set.
Branch 3 (SZ = 1)	Branches to the sequencer instruction register specified by the first and second operands when the SZ flag is set. Executes the next process when the SZ flag is cleared.
Branch 4 (SZ = 0)	Branches to the sequencer instruction register specified by the first and second operands when the SZ flag is cleared. Executes the next process when the SZ flag is set.

Table 1.4   SMS processing list (2/2)

Processing	Operation
Wait	Holds the next process for the period of the specified number of clock cycles.
Conditional wait 1 (bit = 1)	Holds the current process while the specified bit at the specified address is set to 1.
Conditional wait 2 (bit = 0)	Holds the current process while the specified bit at the specified address is set to 0.
Termination	Ends the processing of the SMS. The SMSS register is cleared to 00H.
Interrupt plus termination	Ends the processing of the SMS after issuing an INTSMSE interrupt signal.
DTC activation	Issues a request for activating the DTC.

2. SMS Use Example

As an example of using the SMS, this chapter describes how the SMS determines the average of the results of the 8 most recent A/D conversions. A chart of reduced power consumption due to the use of the SMS is also included.

2.1 Overview of Calculating the Average of A/D Conversion Results

Figure 2.1 shows the mechanism of calculating the average and Figure 2.2 shows the flowchart of average calculation processing.

After a series of A/D conversions, the SMS calculates the average of the results of the 8 most recent A/D conversions.

To calculate the average, the SMS performs steps (1) to (4) in Figure 2.1. The Total stores the total value of the last 8 A/D conversion results. The SMS subtracts the oldest data from this total value, adds the latest A/D conversion result, and updates the Total. The SMS then divides this new Total by divisor 8 (right-shift by 3 bits) to determine the average of the 8 most recent A/D conversion results.
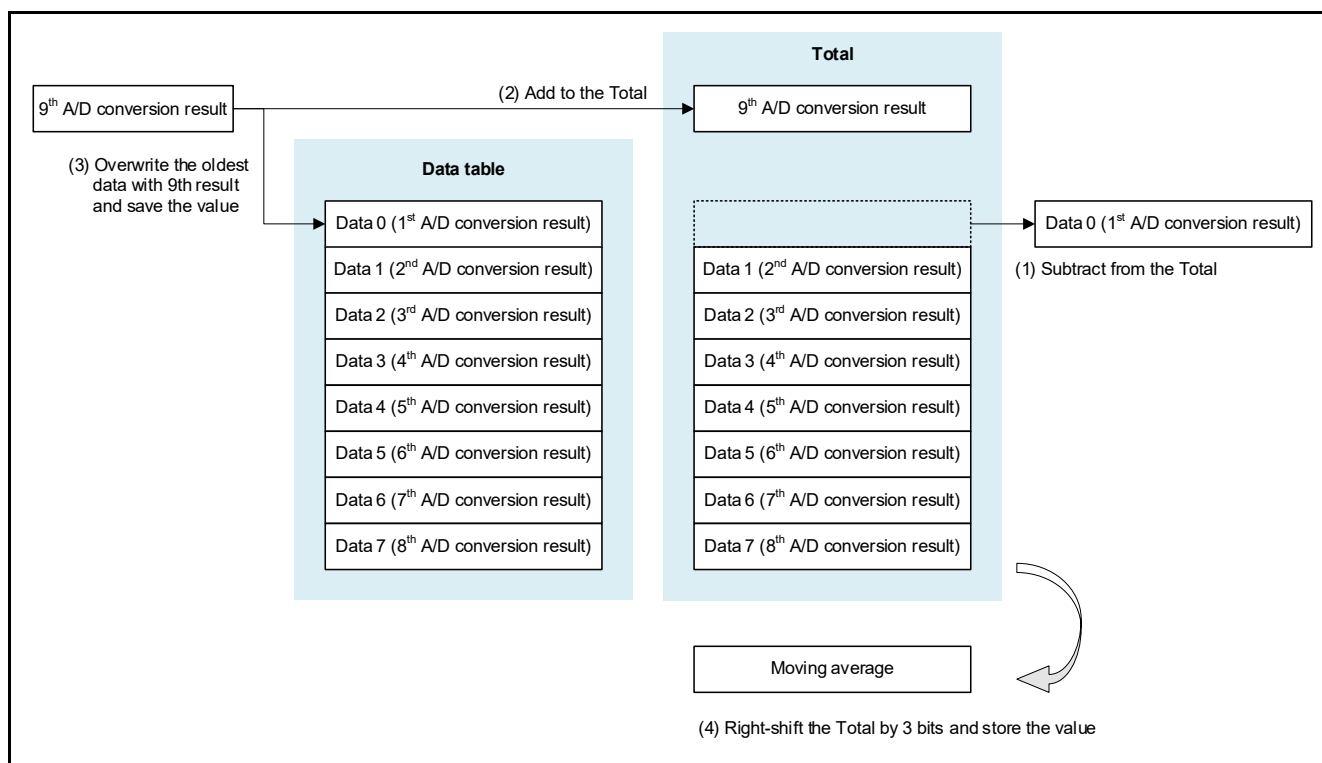

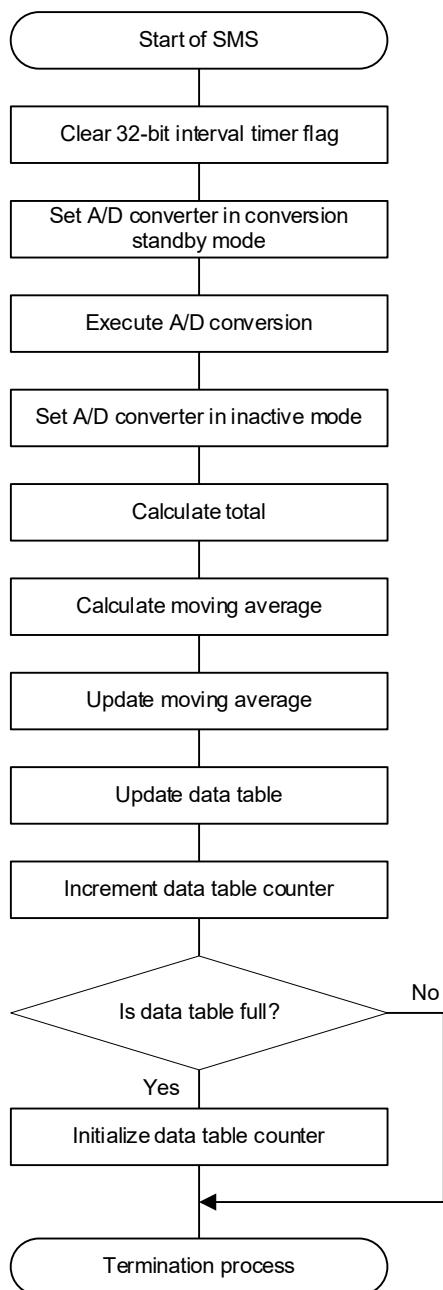Figure 2.1   Mechanism of Calculating the Average

Figure 2.2   Flowchart of Average Calculation Processing

Table 2.1 lists the details of average calculation processing by the SMS.

Table 2.1   Details of Average Calculation Processing by the SMS

Item	Operation	Processing to use
Clearing the 32-bit interval timer flag	Clears the ITF00 bit.	1-bit data clearing
Setting the A/D converter in conversion standby mode	Sets the ADCE bit.	1-bit data setting
	Waits (3 us).	Wait
Executing A/D conversion	Clears the ADIF bit.	1-bit data clearing
	Sets the ADCS bit.	1-bit data setting
	Waits (2 us).	Wait
	Waits until the ADIF bit is set to 1.	Conditional wait 1 (bit = 1)
	Clears the ADIF bit.	1-bit data clearing
	Reads the A/D conversion result.	16-bit data transfer 2
Setting the A/D converter in inactive mode	Clears the ADCE bit.	1-bit data clearing
Calculating the total	Reads the oldest data from the data table.	16-bit data transfer 2
	Subtracts the oldest data from the Total.	Word subtraction
	Adds the A/D conversion result to the Total.	Word addition
Calculating the average	Stores the Total in the calculation variable.	16-bit data transfer 1
	Right-shifts the calculation variable value by 1 bit.	Logical shift right
	Right-shifts the calculation variable value by 1 bit.	Logical shift right
	Right-shifts the calculation variable value by 1 bit.	Logical shift right
Updating the average	Stores the calculation variable value in the RAM.	16-bit data transfer 1
Updating the data table	Stores the A/D conversion result in the data table.	16-bit data transfer 1
Incrementing the data table counter	Updates the reference source address for the data table.	Word addition
Checking the data table upper limit	Compares the data table address and the last address.	Word comparison
	Branches to the termination process if the SCY flag is set to 1.	Branch 1
Initializing the data table counter	Initializes the data table counter.	16-bit data transfer 1
Terminating processing	Performs the termination process.	Termination

2.2　Power Consumption by SMS Processing

　Figure 2.3 shows the chart of power consumption by SMS processing using the calculation of the average of the 8 most recent A/D conversion results as an example. For comparison, Figure 2.4 shows a chart of power consumption by the CPU when it calculates the same average after it is triggered by an interrupt.
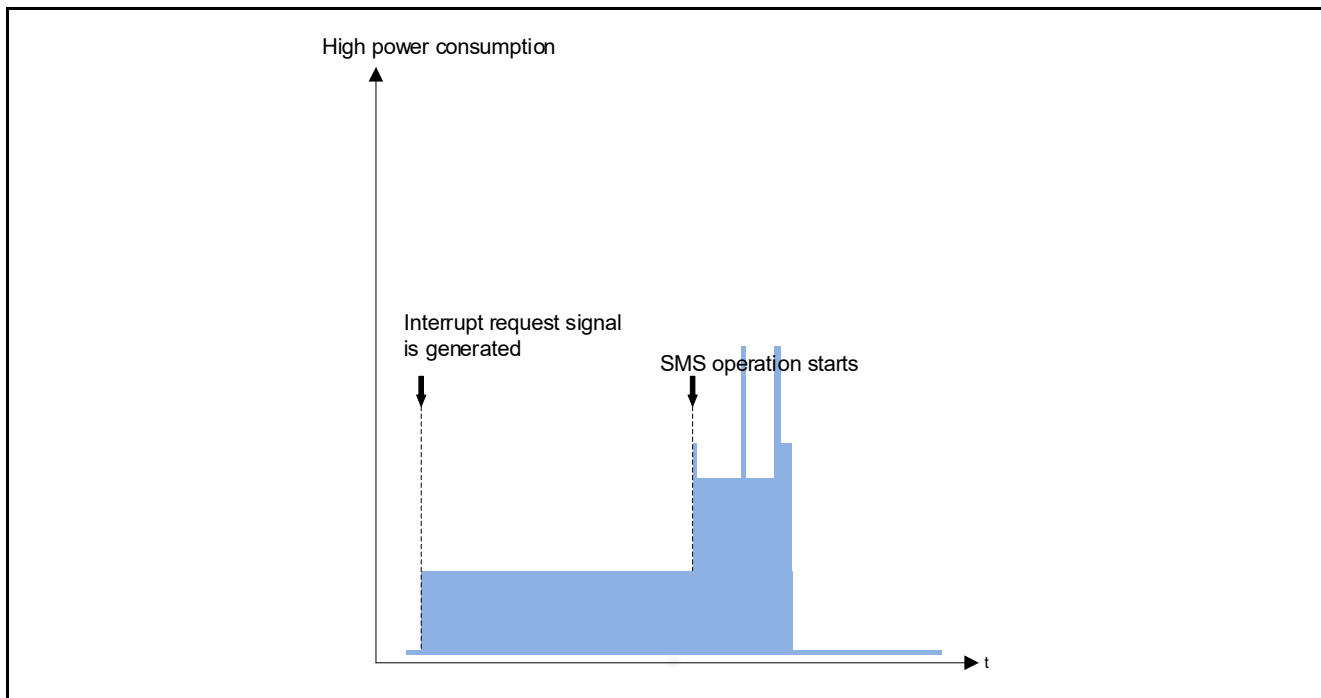

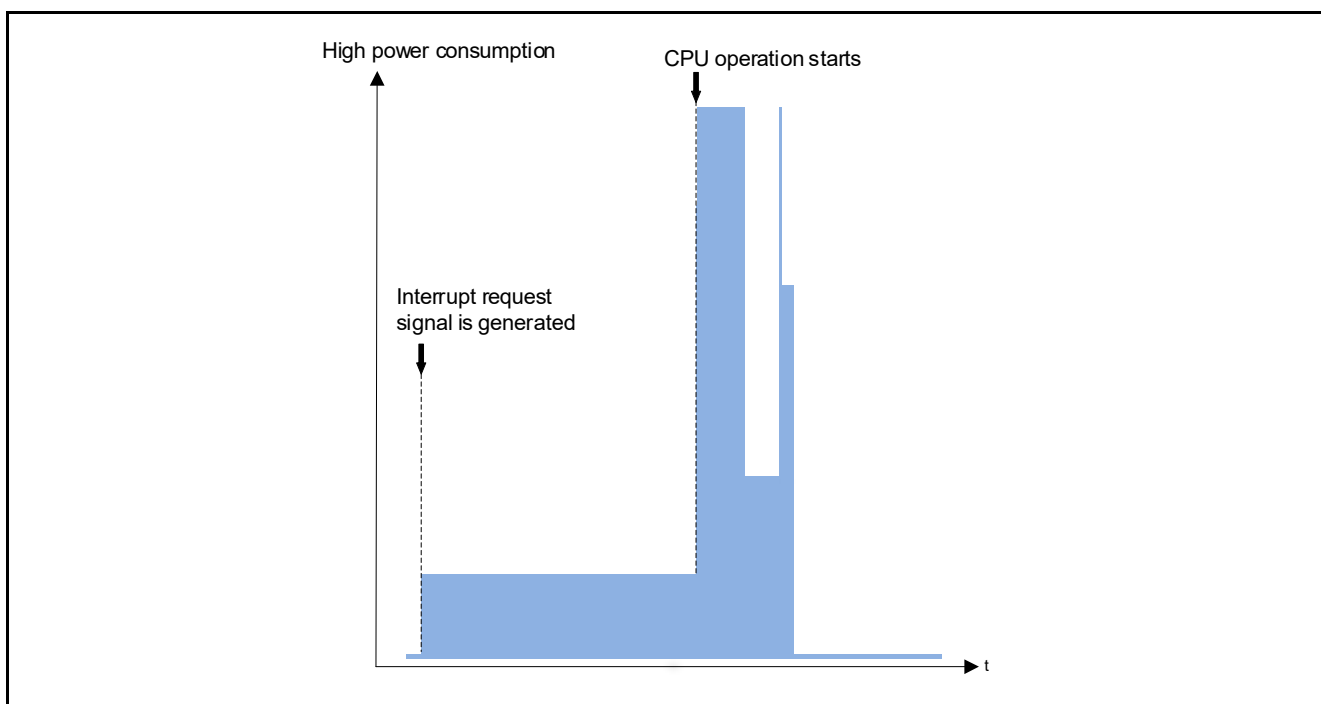
Figure 2.3　Power Consumption by SMS Processing

Figure 2.4　Power Consumption by CPU Processing

3.   Application Examples for the System

This chapter describes cases of assigning some of CPU processing (control of peripheral functions, arithmetic operations, judgement of data) to the SMS.

- Monitoring power supply voltages

    For details, see the application note "SMS Power Supply Monitoring (R01AN5605)".

    To monitor power supply voltages, the SMS is set to start periodically using the 32-bit interval timer. The SMS is used to configure the A/D converter (select the internal reference voltage) so that the A/D converter measures power supply voltages. The SMS lets the A/D converter perform 2 A/D conversions and stops the A/D converter. The second A/D conversion result is used as the monitored power supply voltage. The SMS compares the monitored value with the threshold value. If the monitored value exceeds the threshold value, the SMS activates the CPU to store data or perform other necessary procedures.

- Determining long or short press of a button

    For details, see the application note "SMS Button Long / Short Press Judgment (R01AN5609)".

    To determine whether a button is long pressed or short pressed, the SMS is set to start when triggered by an external interrupt. When the SMS starts, it waits 125 ms. Then, the SMS checks the applicable port level to determine whether the button is long pressed or short pressed. When the SMS detects the button is being pressed, it continues processing and repeats 125-ms wait and port level checking for the specified number of times. If the button is still being pressed after the waits and checking of the specified number of times, the SMS determines that the button is long pressed and activates the CPU.

- Controlling LED blinking and dimming

    For details, see the application note "SMS LED Blinking Dimming Control (R01AN5611)".

    To control flashing and dimming of an LED, the SMS is set to start periodically using the 32-bit interval timer. The SMS is used to update the duty cycle of PWM output (a set of channels of the timer array unit is configured as PWM output) to dim the LED.

- Detecting fire

    For details, see the application note "SMS Fire Detection Operation (R01AN5617)".

    To detect any event of fire, the SMS is set to start periodically using the 32-bit interval timer. The SMS is used to enable a sensor and an infrared LED to detect any presence of smoke. Then, the A/D converter is configured to convert the analog sensor output to a digital value. After A/D conversion is performed, the SMS stops the A/D converter, the sensor, and the infrared LED. The SMS compares the A/D conversion result and the threshold value to determine whether smoke is present. If smoke is detected, the SMS activates the CPU.

- Calculating moving average

    For details, see the application note "SMS Moving Average Calculation (R01AN5610)".

    To calculate the moving average, the SMS is set to start periodically using the 32-bit interval timer. The SMS is used to configure the A/D converter to perform A/D conversion. After A/D conversion, the SMS adds the result to the total of 8 past A/D conversion results. Then, the SMS performs a right shift instruction 3 times to calculate the average from the total value. The SMS stores the average value in the RAM and ends processing.

4.   Sample Code

Sample code can be downloaded from the Renesas Electronics website.

5.   Reference Documents

RL78/G23 User's Manual: Hardware (R01UH0896J)
RL78 Family User's Manual: Software (R01US0015J)
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can downloaded from the Renesas Electronics website.

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Revision History

Rev.	Date	Description	
		Page	**Summary**
1.00	2021.4.13	—	First edition issued

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1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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