

RL78/G23

Setting the Window Comparator

Introduction

This document describes a method to operate the window comparator using the RL78/G23 comparator.

Target Device

RL78/G23

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

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1. Specification

1.1 Overview of Specification

This application note describes how to use the 2 comparators mounted on the RL78/G23 as a window comparator.

When an analog input voltage satisfies the following condition, the VCOUT0 pin outputs a HIGH signal; if it does not satisfy the following condition, the VCOUT0 pin outputs a LOW signal.

Lower threshold reference voltage (internal reference voltage) < Input voltage < Higher threshold reference voltage (D/A converter 0 output)

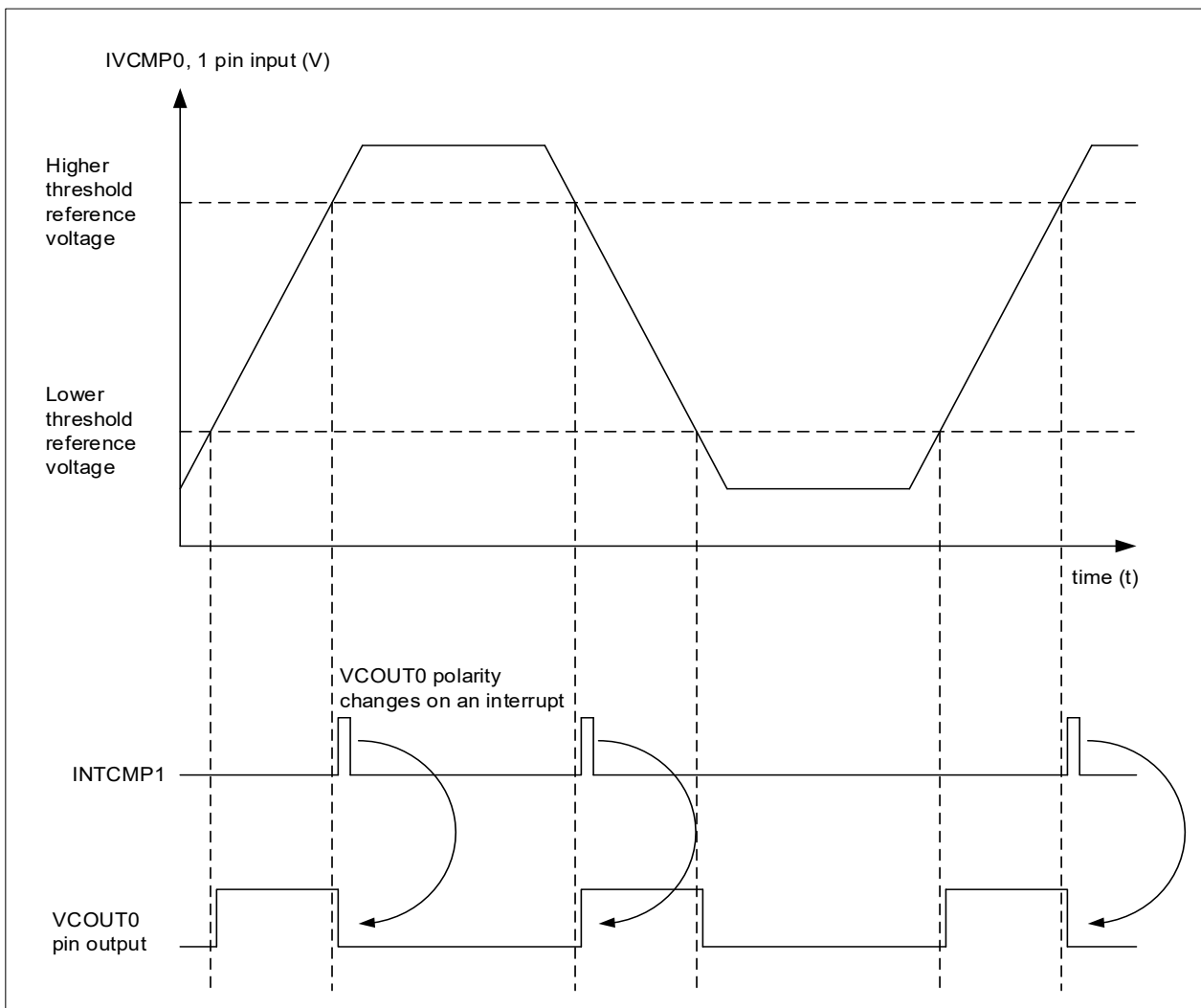
Note that an LED is turned on when comparator high-speed mode is selected.

Table 1-1 lists the peripheral functions to be used and their uses, and Figure 1-1 gives an overview of the window comparator operation.

Table 1-1 Peripheral Function and Use

Peripheral Function	Use
Comparator	Compares input voltages with reference voltages.
D/A converter	Supplies the higher threshold reference voltage.

Figure 1-1 Overview of Window Comparator Operation



1.2 Outline of Operation

Comparator 0 and comparator 1 are combined to work as a window comparator. Set the internal reference voltage as the reference voltage for comparator 0, and set the output of D/A converter 0 as the reference voltage for comparator 1. Set the output voltage of D/A converter 0 higher than the internal reference voltage.

Use a digital filter (sampling clock: fCLK/32) and output the filtered comparator comparison result from the VCOUT0 pin. The VCOUT0 pin outputs a HIGH or LOW signal depending on the condition.

Input voltage		VCOUT0
On a rising edge	On a falling edge	
When the voltage exceeds comparator 1 reference voltage	—	Outputs a LOW signal.
When the voltage exceeds comparator 0 reference voltage	When the voltage is below comparator 1 reference voltage	Outputs a HIGH signal.
—	When the voltage is below comparator 0 reference voltage	Outputs a LOW signal.

(1) Initialize an I/O port.
<Setting condition>

- P53 pin: Set as an output port and set 1 as output (to turn off the connected LED).

(2) Initialize D/A converter 0.

<Setting conditions>

- Use normal mode as the operation mode.
- Set the analog output voltage to 200 (3.91 V when $V_{DD} = 5.0$ V).

(3) Initialize comparator 0.

<Setting conditions>

- Use comparator low-speed mode.
- Select "Supply from the internal reference voltage" for the reference voltage.
- Use "1.4 V to V_{DD} " as the reference voltage range.
- Select "Comparator 0 filter enabled, sampling at fCLK/32" for "filter selection".
- Select "Interrupt request by comparator 0 both-edge detection" for "edge detection".
- Select "Comparator 0 output is output to VCOUT0" for "VCOUT0 output polarity selection".
- Select "Comparator 0 VCOUT0 pin output enabled".
- Select "Comparator 0 interrupt request disabled".
- Use the IVCMP0 pin.

(4) Initialize comparator 1.

<Setting conditions>

- Use comparator low-speed mode.
- Select “Supply from D/A converter 0 output” for the reference voltage.
- Use “1.4 V to V_{DD} ” as the reference voltage range.
- Select “Comparator 1 filter enabled, sampling at $f_{CLK}/32$ ” for “filter selection”.
- Select “Interrupt request by comparator 1 both-edge detection” for “edge detection”.
- Select “Comparator 1 interrupt request enabled”.
- Use the IVCMP1 pin.

(5) When comparator high-speed mode is selected, the LED lights.

(6) When comparator 1 generates an interrupt, the setting value of the C0OP bit (VCOUT0 output polarity selection) changes depending on the value of the C1MON bit (comparator 1 monitor flag).

- The C0OP bit is set to 0 when the C1MON bit is 0 (input voltage < D/A converter 0 output).
- The C0OP bit is set to 1 when the C1MON bit is 1 (input voltage > D/A converter 0 output).

2. Operation Confirmation Conditions

The operation of the sample code in this application note is confirmed based on the conditions described in Table 2-1.

Table 2-1 Operation Confirmation Conditions

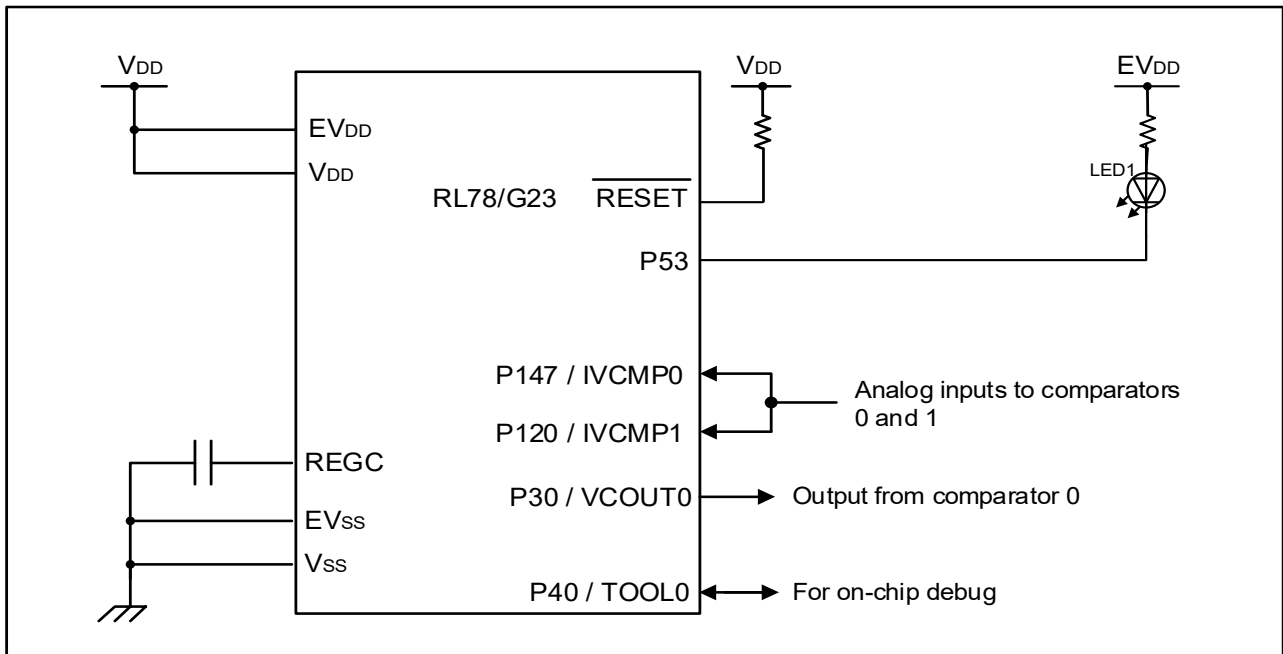
Item	Description
MCU used	RL78/G23 (R7F100GLG)
Operating frequency	<ul style="list-style-type: none"> ● High-speed on-chip oscillator clock (f_{IH}): 32 MHz
Operating voltage	5.0 V (can be operated at 2.0 V to 5.5V) LVD0 operations (V_{LVD0}): Reset mode At rising edge TYP. 1.90 V (1.84 V to 1.95 V) At falling edge TYP. 1.86 V (1.80 V to 1.91 V)
Integrated development environment (CS+)	CS+ for CC E8.05.00f from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.09.00 from Renesas Electronics Corp.
Integrated development environment (e2studio)	e2studio V2021-01 from Renesas Electronics Corp.
C compiler (e2studio)	CC-RL V1.09.00 from Renesas Electronics Corp.
Integrated development environment (IAR)	IAR Embedded Workbench for Renesas RL78 V4.20.1 from IAR Systems Corp.
C compiler (IAR)	IAR C/C++ Compiler for Renesas RL78 V4.20.1.2260 from IAR Systems Corp.
Board used	RL78/G23 Fast Prototyping Board

3. Hardware Descriptions

3.1 Example of Hardware Configuration

Figure 3-1 shows an example of the hardware configuration used in the application note.

Figure 3-1 Hardware Configuration



- Note 1. This schematic circuit diagram is simplified to show the outline of connections. When creating actual circuits, design them using appropriate pin processing so that the circuits meet electrical characteristics. (Connect input-only ports to V_{DD} or V_{SS} individually through a resistor.)
- Note 2. Connect pins (with a name beginning with EV_{SS}), if any, to V_{SS}, and connect pins (with a name beginning with EV_{DD}), if any, to V_{DD}.
- Note 3. Set V_{DD} to a voltage not less than the reset release voltage (V_{LVD0}) set by the LVD0.

3.2 List of Pins to be Used

Table 3-1 lists the pins to be used and their functions.

Table 3-1 Pins to be Used and Their Functions

Pin name	I/O	Functions
P53	Output	Turns an LED on in comparator high-speed mode.
P147 / IVCMP0	Input	Analog input to comparator 0
P120 / IVCMP1	Input	Analog input to comparator 1
P30 / VCOUT0	Output	Output from comparator 0

Caution In this application note, only the used pins are processed. When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements.

4. Software Explanation

4.1 Setting of Option Byte

Table 4-1 shows the option byte settings.

Table 4-1 Option Byte Settings

Address	Setting Value	Contents
000C0H / 040C0H	11101111B	Disables the watchdog timer. (Counting stopped after reset)
000C1H / 040C1H	11111110B	LVD0 detection voltage: reset mode At rising edge TYP. 1.90 V (1.84 V to 1.95 V) At falling edge TYP. 1.86 V (1.80 V to 1.91 V)
000C2H / 040C2H	11101000B	HS mode, High-speed on-chip oscillator clock (f_{IH}): 32 MHz
000C3H / 040C3H	10000101B	Enables on-chip debugging

4.2 List of Constants

Table 4-2 lists the constants that are used in the sample code.

Table 4-2 Constant

Constant Name	Setting Value	Description
COMP_HIGHSPEED_MODE	-	Enables comparator high-speed mode.
LED_ON	00H	LED control: On
LED_OFF	01H	LED control: Off
WAITCOUNT_3US	16	Wait count for 3 μ s as DAC settling time

4.3 List of Functions

Table 4-3 shows a list of functions.

Table 4-3 Functions

Function Name	Outline
r_Config_COMP1_interrupt	Comparator 1 interrupt processing

4.4 Specification of Functions

The function specifications of the sample code are shown below.

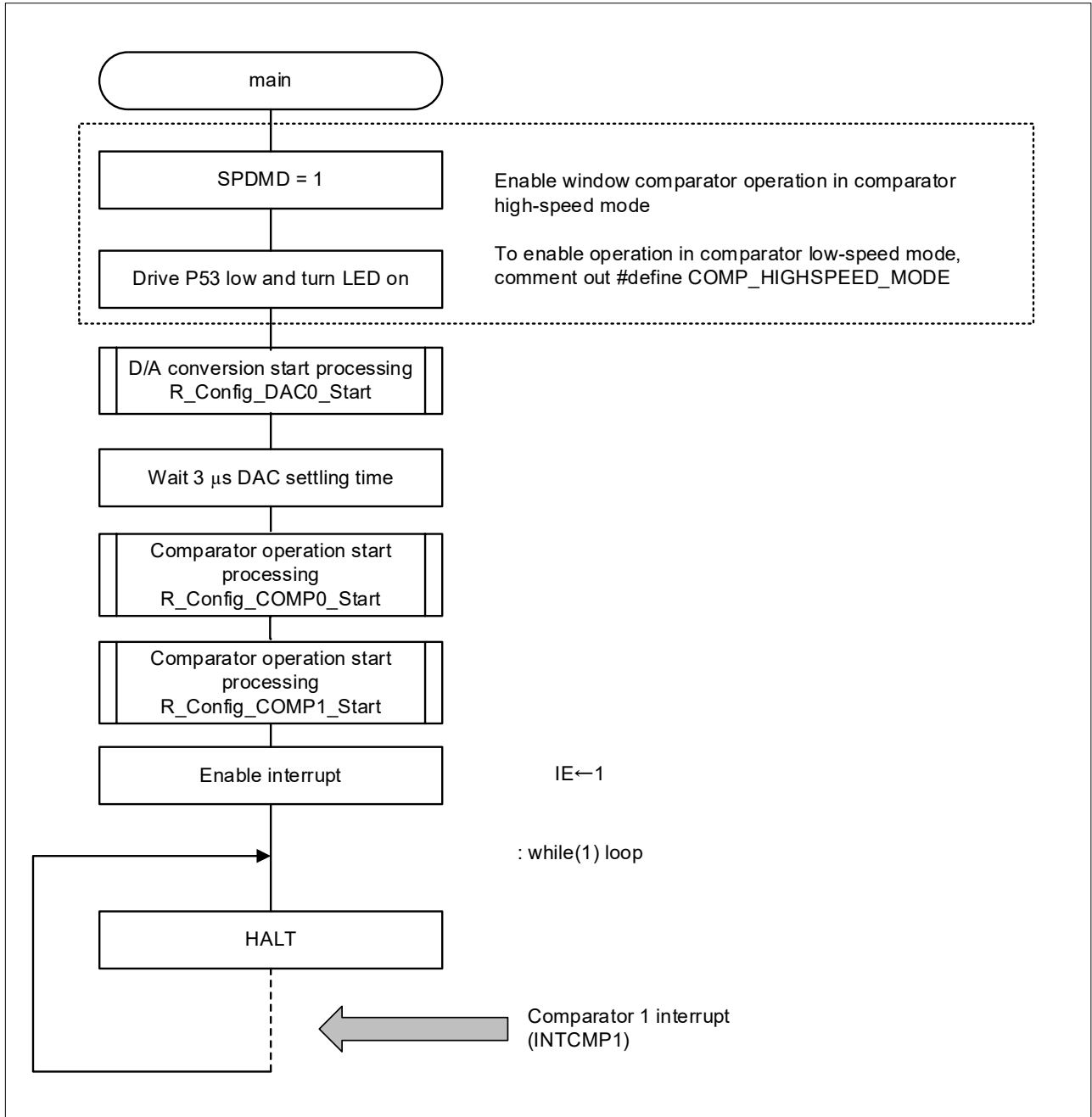
r_Config_COMP1_interrupt	
Outline	Comparator 1 interrupt processing
Header	Config_COMP1.h
Declaration	static void __near r_Config_COMP1_interrupt(void);
Description	Changes the setting value for VCOUT0 output polarity selection depending on the value of the comparator 1 monitor flag.
Argument	None
Return Value	None

4.5 Flowcharts

4.5.1 Main Processing

Figure 4-1 shows the flowchart of the main processing.

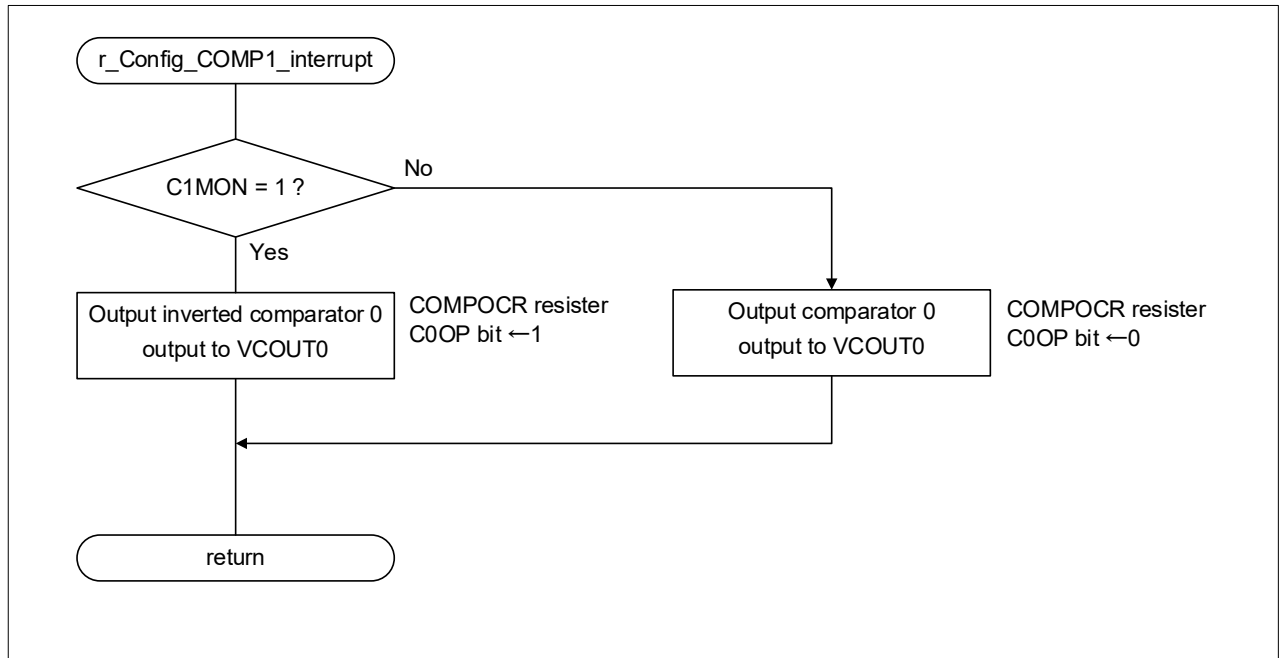
Figure 4-1 Main Processing



4.5.2 Comparator 1 Interrupt Processing

Figure 4-2 shows the flowchart of the comparator 1 interrupt processing.

Figure 4-2 Comparator 1 Interrupt Processing



5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

RL78/G23 User's Manual: Hardware (R01UH0896)

RL78 family user's manual software (R01US0015)

The latest versions can be downloaded from the Renesas Electronics website.

Technical update

The latest versions can be downloaded from the Renesas Electronics website.

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2021.04.13	—	First Edition

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A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

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The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

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After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

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