RL78/G14, M16C/62P Group

Migration Guide from M16C/62P to RL78/G14: I/O Ports

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Abstract

This application note explains how to migrate I/O ports of the M16C/62P Group to port functions of RL78/G14 (100-pin products).

Target Device

RL78/G14, M16C/62P Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

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1. Differences between M16C/62P Group and RL78/G14

Table 1.1 shows differences in I/O ports.

Table 1.1 Differences in I/O Ports

Item	M16C/62P Group	RL78/G14
Number of ports	80-pin products: 70 ports 100-pin products: 87 ports 128-pin products: 113 ports	30-pin products: 26 ports 32-pin products: 28 ports 36-pin products: 32 ports 40-pin products: 36 ports 44-pin products: 40 ports 48-pin products: 44 ports 52-pin products: 48 ports 64-pin products: 58 ports 80-pin products: 74 ports 100-pin products: 92 ports
I/O buffer power supply	V_{CC1} (Note 3) V_{CC2} (Note 4)	• V_{DD} (Note 1) • EV_{DD0} (Note 2) • EV_{DD1} (Note 2)
Ground for port pins	V_{SS}	• V_{SS} (Note 1) • EV_{SS0} (Note 2) • EV_{SS1} (Note 2)
External bus connection	Available	None
Through-current preventing function for input buffers	None	Available
Controlling the input threshold value	None	Either of the two kinds of threshold values may be selected by the PIMxx register.
Protection function against write to the direction register	Available (Port 9 only)	None

PIMxx: xx = 0, 1, 3 to 5, 8, 14

Notes

1. Applies to ports P20 to P27, P121 to P124, P137, P150 to P156 and pins without port function.
2. Applies to ports other than P20 to P27, P121 to P124, P137, P150 to P156
3. Applies to ports P60 to P67, P70 to P77, P80 to P83, P85, P90 to P97, P100 to P107
4. Applies to ports P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57

2. Register Compatibility

Table 2.1 and Table 2.2 are comparison tables of registers regarding I/O ports.

Table 2.1 Register Compatibility (1/2)

Item	M16C/62P Group	RL78/G14
Port level control	Pxx register	Pxx register
Port direction selection	PDxx register	PMxx register
Port assignment control	–	• PIOR0 register • PIOR1 register
Clock port connection	– Fixed to XIN, XOUT ports	Select by the OSCSEL and EXCLK bits in the CMC register
Sub-clock port connection	– CM04 bit in the CM0 register	Select by the OSCSELS and EXCLKS bits in the CMC register
Port input function selection	–	PMS register
Port latch read function	PCR register	–
Pull-up control	• PUR0 register • PUR1 register • PUR2 register	PUxx register
Direction register write protection	PRC2 bit in the PRCR register	–
Input threshold value control	–	PIMxx register

– : No register is applicable.
Pxx: xx = 0 to 10
PDxx: xx = 0 to 10
PMxx: xx = 0 to 8, 10 to 12, 14, 15
Pxx: xx = 0 to 8, 10 to 15
PUxx: xx = 0, 1, 3 to 8, 10 to 12, 14
PIMxx: xx = 0, 1, 3 to 5, 8, 14

Table 2.2 Comparison of Registers (2/2)

Item	M16C/62P Group	RL78/G14
Port output mode selection	–	POMxx register
Digital I/O/analog I/O selection	–	• PMCxx register • ADPC register
Through-current preventing setting	–	GDIDIS register

– : No register is applicable.
POMxx: xx = 0, 1, 3 to 5, 7, 8, 14
PMCxx: xx = 0, 1, 10, 12, 14

3. Comparison of I/O Port Functions

3.1 Port Direction Selection

3.1.1 M16C/62P Group

In the M16C/62P Group, the port input/output mode is set by the PDxx register. Table 3.1 shows the PDxx register functions.

Table 3.1 PDxx Register Functions

PDxx	Direction bit selection of the port Pxx
0	Input mode (the pin functions as an input port)
1	Output mode (the pin functions as an output port)

PDxx: xx = 0 to 10
Pxx: xx = 0 to 10

3.1.2 RL78/G14

In RL78/G14, the port I/O is set by using the PMxx register. Table 3.2 shows the PMxx register functions.

Table 3.2 PMxx Register Functions

PMxx	PMxx pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

PMxx: xx = 0 to 8, 10 to 12, 14, 15

3.1.3 RL78/G14 Only

In RL78/G14, the digital I/O/analog input port mode can be selected by setting the PMCxx register. Table 3.3 shows the PMCxx register functions.

Table 3.3 PMCxx Register Functions

PMCxx	PMCxx pin I/O mode selection
0	Digital I/O (alternate function other than analog input)
1	Analog input

PMCxx: xx = 0, 1, 10, 12, 14

3.2 Port I/O Data

3.2.1 M16C/62P Group

In the M16C/62P Group, the port status is read from the port data register Pxx and the data set to the Pxx register is output from the port according to the mode set by the port direction select register PDxx. Contents read from the port data register P1 differ depending on the setting of the port control register PCR. Table 3.4 lists the PCR register functions. Table 3.5 shows relationship of registers PRC, PDxx, and Pxx.

Table 3.4 PCR Register Functions

PCR	P1 register read mode selection
0	When the port is set for input, the input levels of P1_0 to P1_7 pins are read. When set for output, the port latch is read.
1	The port latch is read regardless of whether the port is set for input or output.

Table 3.5 Relationship of PCR, PDxx, and Pxx Registers

PCR	PDxx	Pxx	Description
0	0	X	When read, the port status is read.
0	1	0	When writing 0, output from the port is set to low. When read, the Pxx register value is read.
0	1	1	When writing 1, output from the port is set to high. When read, the Pxx register value is read.
1 (Note 1)	0	X	When reading P1, the P1 register value is read.
1 (Note 1)	1	0	When writing 0, output from the port is set to low. When reading P1, the P1 register value is read.
1 (Note 1)	1	1	When writing 1, output from the port is set to high. When reading P1, the P1 register value is read.

Note
1. Only P1 in the PCR register is valid.

PDxx: xx = 0 to 10
Pxx: xx = 0 to 10

3.2.2 RL78/G14

In RL78/G14, according to the mode set by the port direction selection register PMxx, the port status is read from the port data register Pxx and the data set to Pxx is output from the port. The read contents of the port data register Pxx vary depending on the port mode selection register PMS. Table 3.6 shows the functions of the PMS register and Table 3.7 describes a relationship of PMS, PMxx, and Pxx registers.

Table 3.6 PMS Register Functions

PMS0	Selection of data to be read when pin is output mode
0	Pxx register value is read.
1	Digital output level of the pin is read.

Notes
1. While the PMS0 bit in the PMS register is set to 1, do not change the value of the port register (Pxx) using a bit manipulation instruction. To change the value of the port register (Pxx), use an 8-bit data manipulation instruction.
2. When the digital output level of a pin that is held in the high-impedance state by the timer RD pulse output forced cutoff function, the read value is 0.

Table 3.7 Relationship of PMS, PMxx, and Pxx Registers

PMS0	PMxx	Pxx	Description
0	1	X	When read, the port status is read.
0	0	0	When writing 0, output from the port is set to low. When read, the Pxx register value is read.
0	0	1	When writing 1, output from the port is set to high. When read, the Pxx register value is read.
1	1	X	When read, the port status is read.
1	0	0	When writing 0, output from the port is set to low. When read, the digital output level of the port is read.
1	0	1	When writing 1, output from the port is set to high. When read, the digital output level of the port is read.

PMxx: xx = 0 to 8, 10 to 12, 14, 15
Pxx: xx = 0 to 8, 10 to 15

3.3 On-chip Pull-up Control

3.3.1 M16C/62P Group

In the M16C/62P Group, the PUR0 to PUR3 register bits can be used to select whether or not to pull the corresponding port up in 4 bit units. The port chosen to be pulled up has a pull-up resistor connected to it when the direction bit is set for input mode. Table 3.8 shows the PUR0 register functions.

Table 3.8 PUR0 Register Functions

PUR0		Description
PU00	Pull-up resistor for P0_0 to P0_3	0: On-chip pull-up resistor not connected 1: On-chip pull-up resistor connected
PU01	Pull-up resistor for P0_4 to P0_7	
PU02	Pull-up resistor for P1_0 to P1_3	
PU03	Pull-up resistor for P1_4 to P1_7	
PU04	Pull-up resistor for P2_0 to P2_3	
PU05	Pull-up resistor for P2_4 to P2_7	
PU06	Pull-up resistor for P3_0 to P3_3	
PU07	Pull-up resistor for P3_4 to P3_7	

3.3.2 RL78/G14

In RL78/G14, whether to use a pull-up resistor or not can be selected in 1-bit units by setting each bit of the PUxx register. To the ports with setting to connect pull-up resistor, a pull-up resistor is connected when the direction bit is set to input mode. Table 3.9 shows the PUxx register functions.

Table 3.9 PUxx Register Functions

PUxx	On-chip pull-up resistor selection of Pxx
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

PUxx: xx = 0, 1, 3 to 8, 10 to 12, 14

3.4 Direction Register Write Protection Control

3.4.1 M16C/62P Only

The M16C/62P Group has a function to protect the port direction register not to be rewritten easily. The target is the port 9 only. To enable write to the port 9 direction register PD9, set the PRC2 bit in the protect register PRCR to “1” (write enabled). The PRC2 bit is set to “0” (write protected) by writing to any address after setting it to “1” (write enabled). The registers protected by the PRC2 bit should be changed in the next instruction after setting the PRC2 bit to “1”. Make sure no interrupts or DMA transfers will occur between the instruction in which the PRC2 bit is set to “1” and the next instruction. Table 3.10 shows the PRCR register functions.

Table 3.10 PRCR Register Functions

PRCR	Selection as to whether to protect or enable write
0	Write protected
1	Write enabled

3.5 Ports Commonly Used for Peripheral Functions

3.5.1 Switching between Digital I/O and Analog I/O (RL78/G14 Only)

In RL78/G14, the ADPC register is used to switch between digital I/O of ports and analog input of the A/D converter, and to switch between digital I/O of ports and analog output of D/A converter. Reset signal generation sets this register to analog I/O.

Target ports to switch between digital I/O of ports and analog input of the A/D converter are P20/ANI0, P21/ANI1, P22/ANI2/ANO0, P23/ANI3/ANO1, P24/ANI4 to P27/ANI7, and ANI8/P150 to ANI14/P156.

Target ports to switch between digital I/O of ports and analog output of the D/A converter are P22/ANI2/ANO0 and P23/ANI3/ANO1.

As the ADPC register switches pins ANI0 to ANIxx to analog input, careful consideration should be given to which analog input pins are used in the user system before setting them (xx: 1 to 14).

Symbol	7	6	5	4	3	2	1	0
ADPC	0	0	0	0	ADPC3	ADPC2	ADPC1	ADPC0

ADPC3	ADPC2	ADPC1	ADPC0	Switch between Analog I/O (A) and Digital I/O (D)													
				ANI14/P156	ANI13/P155	ANI12/P154	ANI11/P153	ANI10/P152	ANI9/P151	ANI8/P150	ANI7/P27	ANI6/P26	ANI5/P25	ANI4/P24	ANI3/ANO1/P23	ANI2/ANO0/P22	ANI1/P21	ANI0/P20
0	0	0	0	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
0	0	0	1	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
0	0	1	0	D	D	D	D	D	D	D	D	D	D	D	D	D	D	A
0	0	1	1	D	D	D	D	D	D	D	D	D	D	D	D	D	A	A
0	1	0	0	D	D	D	D	D	D	D	D	D	D	D	D	A	A	A
0	1	0	1	D	D	D	D	D	D	D	D	D	D	D	A	A	A	A
0	1	1	0	D	D	D	D	D	D	D	D	D	D	A	A	A	A	A
0	1	1	1	D	D	D	D	D	D	D	D	D	A	A	A	A	A	A
1	0	0	0	D	D	D	D	D	D	D	D	A	A	A	A	A	A	A
1	0	0	1	D	D	D	D	D	D	D	A	A	A	A	A	A	A	A
1	0	1	0	D	D	D	D	D	D	A	A	A	A	A	A	A	A	A
1	0	1	1	D	D	D	D	D	A	A	A	A	A	A	A	A	A	A
1	1	0	0	D	D	D	D	A	A	A	A	A	A	A	A	A	A	A
1	1	0	1	D	D	D	A	A	A	A	A	A	A	A	A	A	A	A
1	1	1	0	D	D	A	A	A	A	A	A	A	A	A	A	A	A	A
1	1	1	1	D	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Other than above				Do not set.														

3.5.2 Other Peripheral Functions

For details of differences in the ports commonly used for peripheral functions, refer to M16C/62P Group Hardware Manual and RL78/G14 User's Manual: Hardware.

4. Connection of Unassigned Pins

4.1 M16C/62P Group

Table 4.1 shows an example of connection of the M16C/62P Group unassigned pins.

Table 4.1 Connection Example of Unassigned Pins of M16C/62P Group

Port name	Recommended connection of unassigned pins
Ports P0 to P7, P8_0 to P8_4, P8_6 to P8_7, P9 to P10	Input: Set to input mode and independently connect to V_{SS} via a resistor (pull-down) Output: Set to output mode and leave the port open.
XOUT	Leave open.
NMI (P8_5)	Connect to V_{CC1} via a resistor (pull-up).
AV_{CC}	Connect to V_{CC1}.
AV_{SS}, VREF, BYTE	Connect to V_{SS}.

4.2 RL78/G14

Table 4.2 describes an example of connection of RL78/G14 unused pins

Table 4.2 Connection Example of Unassigned Pins of RL78/G14

Port name	Recommended connection of unused pins
P00 to P06, P10 to P17, P30, P31, P41 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	Input: Independently connect to EV_{DD0}, EV_{DD1} or EV_{SS0}, EV_{SS1} via a resistor. Output: Leave open.
P20 to P27, P150 to P156	Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P40	Input: Independently connect to EV_{DD0} via a resistor, or leave open. Output: Leave open.
P130	Leave open.
P121 to P124, P137	Independently connect to V_{DD} or V_{SS} via a resistor.
$\overline{\text{RESET}}$	Connect to V_{DD} directly or via a resistor.
REGC	Connect to V_{SS} via a capacitor (0.47 to 1 µF).

5. Notes

5.1 Notes on Pin Setting of RL78/G14 Products Other Than 100-pin Products

The P15 pin in RL78/G14 (except 100-pin products) may be multiplexed with other output functions. For details on the multiplexed functions and pin handling, refer to the RL78/G14 User's Manual: Hardware.

6. Reference Documents

RL78/G14 User's Manual: Hardware Rev. 2.00
M16C/62P Group Hardware Manual Rev.2.41

The latest versions can be downloaded from the Renesas Electronics website.

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1.00	Dec.10,2013	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Colophon 3.0