RL78/G14, M16C/62P Group

Migration Guide from M16C to RL78: A/D Converter

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Abstract

This application note describes how to migrate from the M16C/62P Group A/D converter to the RL78/G14 A/D converter.

Target Devices

RL78/G14, M16C/62P Group

For details on the A/D converter and the electrical specifications, refer to User's Manuals: Hardware and technical updates.

Contents

1. Differences between RL78/G14 and the M16C/62P Group

Table 1.1 the differences between the RL78/G14 A/D converter and the H8/3687 Group A/D converter.

Table 1.1 Differences in the A/D Converters

Item	M16C/62P Group	RL78/G14
Reference voltage	V_{REF} (2.0 V to V_{CC1})	Select from V_{DD}, AV_{REFP} (1.6 V to V_{DD}), or internal reference voltage (1.45 V)
Analog input voltage	0 V to V_{REF}	• Reference voltage = AV_{REFP} ANI2 to ANI14: 0 V to AV_{REFP} ANI16 to ANI20: 0 V to AV_{REFP} and EV_{DD0} • Reference voltage = V_{DD} ANI0 to ANI14: 0 V to V_{DD} ANI16 to ANI20: 0 V to EV_{DD0} • Reference voltage = internal reference voltage 0 to V_{BGR}
Operating clocks (conversion clocks)	fAD, divide-by-2 of fAD, divide-by-3 of fAD, divide-by-4 of fAD, divide-by-6 of fAD, or divide-by-12 of fAD (The fAD clock is produced from the main clock, PLL clock or on-chip oscillator clock, and is used for the A/D converter.)	f_{CLK}/64, f_{CLK}/32, f_{CLK}/16, f_{CLK}/8, f_{CLK}/6, f_{CLK}/5, f_{CLK}/4, f_{CLK}/2 (f_{CLK}: CPU/peripheral hardware clock frequency)
Resolution	8-bit or 10-bit	8-bit or 10-bit
Operating mode (A/D conversion mode)	One-shot mode, repeat mode, single sweep mode, repeat sweep mode 0, and repeat sweep mode 1	Specify by the combination of A/D channel selection mode (select mode, scan mode) and A/D conversion operating mode (sequential conversion mode, one-shot conversion mode)
Analog input pins	8 (AN0 to AN7) + 2 (ANEX0 and ANEX1) + 8 (AN0_0 to AN0_7) + 8 (AN2_0 to AN2_7)	8 channels (30-, 32-, 36-pin), 9 channels (40-pin), 10 channels (44-, 48-pin), 12 channels (52-, 64-pin), 17 channels (80-pin), 20 channels (100-pin)
A/D conversion trigger	• Software trigger • External trigger (retriggerable)	• Software trigger • Hardware trigger (Note 1)
Hardware trigger operating mode	N/A	Available (Hardware trigger no-wait mode, hardware trigger wait mode)
A/D conversion time	• Without sample and hold function 8-bit resolution: 49 ϕAD cycles, 10-bit resolution: 59 ϕAD cycles • With sample and hold function 8-bit resolution: 28 ϕAD cycles, 10-bit resolution: 33 ϕAD cycles	Specified by the ADM0 register
Number of pins used simultaneously	1, 2, 4, 6, or 8 pins (Note 2)	1 or 4 pins (Note 2)
Number of A/D conversion result registers	8 (AD0 to AD7)	1 (Note 3)
Availability in STOP mode	N/A	Available (SNOOZE mode)
On-chip reference voltage/ internal reference voltage	N/A	1.45 V (TYP.)
Temperature sensor	N/A	Available
Test mode	N/A	Available

Notes

1. Hardware trigger can be selected from (a) timer channel 1 count end or capture end interrupt signal (INTTM01), (b) event signal selected by the ELC, (c) real-time clock interrupt signal (INTRTC), or (d) 12-bit interval timer interrupt signal (INTIT).
2. Number of pins used simultaneously varies depending on the specified operating mode.
3. The RL78/G14 MCU holds one A/D conversion result only. To perform A/D conversion sequentially, use the DTC to read the A/D conversion result before the next conversion is completed.
   For details on reading the A/D conversion result using the RL78/G14 DTC, refer to the application note “RL78/G14 Transferring the A/D Conversion Result Using the DTC”.

2. Register Compatibility

Register compatibility between the M16C/62P Group and RL78/G14 is listed in Table 2.1.

Table 2.1 Register Compatibility

Item	M16C/62P Group	RL78/G14
On-chip reference voltage	—	• ADM2 register Bits ADREFP1 and ADREFP0 ADREFM bit • ADS register
A/D conversion result	• Registers AD0 to AD7	• ADCR register (10 bits) • ADCRH register (8 bits)
Clock division	• ADCON0 register CKS0 bit • ADCON1 register CKS1 bit • ADCON2 register CKS2 bit	• ADM0 register Bits FR2 to FR0
A/D operating mode	• ADCON0 register Bits MD1 and MD0	• ADM0 register ADMD bit • ADM1 register ADSCM bit
A/D conversion trigger mode	• ADCON0 register TRG bit	• ADM1 register Bits ADTMD1 and ADTMD0 Bits ADTRS1 and ADTRS0
Analog input pin	• ADCON0 register Bits CH2 and CH0 • ADCON1 register Bits SCAN1 and SCAN0 • ADCON2 register Bits ADGSEL1 and ADGSEL0	• ADS register • ADPC register • PMC0 register • PMC10 register • PMC12 register • PMC14 register
A/D conversion operation control	• ADCON0 register ADST bit	• ADM0 register ADCS bit ADCE bit
Resolution	• ADCON1 register BITS bit	• ADM2 register ADTYP bit
A/D input clock control	—	• PER0 register ADCEN bit
A/D conversion time mode	—	• ADM0 register Bits LV1 and LV0
Check the upper and lower limit values of conversion result	—	• ADM2 register ADRCK bit
SNOOZE mode	—	• ADM2 register AWC bit
Temperature sensor output	—	ADS register
Set the upper and lower limits of A/D conversion result comparison values	—	• ADUL register • ADLL register
A/D test function	—	• ADTES register Bits ADTES1 and ADTES0

– : No register is applicable.

3. A/D Converter Operation

3.1 A/D Operating Mode

In the RL78/G14 MCU, select the A/D conversion mode by the combination of A/D channel selection mode and A/D conversion operating mode.
Table 3.1 lists the combination of the RL78/G14 channel selection mode and conversion operating mode compatible with the M16C/62P Group operating mode.

Table 3.1 A/D Operating Mode Compatibility

M16C/62P Group	RL78/G14	
	Channel selection mode	Conversion Operating Mode
Repeat mode	Select mode	Sequential conversion mode
One-shot mode		One-shot conversion mode
Repeat sweep mode 0	Scan mode	Sequential conversion mode
Single sweep mode		One-shot conversion mode
Repeat sweep mode 1 (Note 1)	Select mode	One-shot conversion mode

Note
1. This mode is handled by software sequencing.

3.2 Absolute Accuracy

RL78/G14 defines the overall error instead of the absolute accuracy defined in the M16C/62P Group.

3.2.1 M16C/62P Group Characteristics

Table 3.2 lists the absolute accuracy of the M16C/62P Group.

Table 3.2 M16C/62P Group Absolute Accuracy

Item		Measurement conditions		Standard			Unit
				Min.	Typ.	Max.	
Absolute accuracy	10-bit mode	V_{ref} = V_{CC1} = 5.0 V	AN0 to AN7 input AN0_0 to AN0_7 input AN2_0 to AN2_7 input ANEX0, ANEX1 input	—	—	± 3	LSB
			External operation amplifier connection mode	—	—	± 7	LSB
		V_{ref} = V_{CC1} = 3.3 V	AN0 to AN7 input AN0_0 to AN0_7 input AN2_0 to AN2_7 input ANEX0, ANEX1 input	—	—	± 5	LSB
			External operation amplifier connection mode	—	—	± 7	LSB
	8-bit mode	V_{ref} = V_{CC1} = 5.0 V, 3.3 V		—	—	± 2	LSB

3.2.2 RL78/G14 Characteristics

Table **3.3** lists the RL78/G14 overall error under the following conditions:

When AVREF (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), and AVREF (−) = AVREFM/ANI1 (ADREFM = 1), then the target ANI pins are ANI2 to ANI14 (ANI pins whose power is supplied from VDD).

Table 3.3 RL78/G14 Overall Error

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Overall error	AINL	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V		1.2	± 3.5	LSB
		AV_{REFP} = V_{DD}	1.6 V ≤ V_{DD} ≤ 5.5 V		1.2	± 7.5	LSB

3.3 Analog Input Pins

When using the M16C/62P Group MCU in the single sweep mode or repeat sweep mode, the number of analog input pins used can be specified as 2, 4, 6, or 8. However, only four input pins can be specified when using the RL78/G14 MCU in scan mode.

3.3.1 M16C/62P Group

Analog input pins available in each operating mode for the M16C/62P Group are listed in Table 3.4.

Table 3.4 Analog Input Pins for the M16C/62P Group

Operating mode	Analog input pin
One-shot mode Repeat mode	Select one pin from AN0 to AN7, AN0_0 to AN0_7, AN2_0 to AN2_7, ANEX0 to ANEX1 (Note 1)
Single sweep mode Repeat sweep mode 0 Repeat sweep mode 1	Select from AN0 to AN1 (2 pins), AN0 to AN3 (4 pins), AN0 to AN5 (6 pins), AN0 to AN7 (8 pin) (Note 2)

Notes
1. If VCC2 < VCC1, do not use AN0_0 to AN0_7 and AN2_0 to AN2_7 as analog input pins.
2. AN0_0 to AN0_7 and AN2_0 to AN2_7 can be used in the same way as AN0 to AN7.

3.3.2 RL78/G14

Analog input pins available in each channel selection mode for the RL78/G14 are listed in Table 3.5.

Table 3.5 Analog Input Pins for RL78/G14

Channel selection mode	Analog input pin
Select mode	Select one pin from pins AN0 to AN14, ANI16 to ANI20, internal reference voltage pin, or temperature sensor output pin
Scan mode	Pins ANI0 to ANI3, ANI1 to ANI4, ANI2 to ANI5, ANI3 to ANI6, ANI4 to ANI7, ANI5 to ANI8, ANI6 to ANI9, ANI7 to ANI10, ANI8 to ANI11, ANI9 to ANI12, ANI10 to ANI 13, ANI11 to ANI14

When using the RL78/G14 MCU, ports which are used as analog input pins must be switched to analog inputs by setting registers ADPC or PMC. Note that the ADPC register switches pins ANI0 to ANI14 to analog inputs in sequence. Careful consideration is required before setting analog input pins.

Symbol	7	6	5	4	3	2	1	0
ADPC	0	0	0	0	ADPC3	ADPC2	ADPC1	ADPC0

ADPC3	ADPC2	ADPC1	ADPC0	Switch between analog input (A) and digital I/O (D)														
				ANI14/P156	ANI13/P155	ANI12/P154	ANI11/P153	ANI10/P152	ANI9/P151	ANI8/P150	ANI7/P27	ANI6/P26	ANI5/P25	ANI4/P24	ANI3/P23	ANI2/P22	ANI1/P21	ANI0/P20
0	0	0	0	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
0	0	0	1	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
0	0	1	0	D	D	D	D	D	D	D	D	D	D	D	D	D	D	A
0	0	1	1	D	D	D	D	D	D	D	D	D	D	D	D	D	A	A
0	1	0	0	D	D	D	D	D	D	D	D	D	D	D	D	A	A	A
0	1	0	1	D	D	D	D	D	D	D	D	D	D	D	A	A	A	A
0	1	1	0	D	D	D	D	D	D	D	D	D	D	A	A	A	A	A
0	1	1	1	D	D	D	D	D	D	D	D	D	A	A	A	A	A	A
1	0	0	0	D	D	D	D	D	D	D	D	A	A	A	A	A	A	A
1	0	0	1	D	D	D	D	D	D	D	A	A	A	A	A	A	A	A
1	0	1	0	D	D	D	D	D	D	A	A	A	A	A	A	A	A	A
1	0	1	1	D	D	D	D	D	A	A	A	A	A	A	A	A	A	A
1	1	0	0	D	D	D	D	A	A	A	A	A	A	A	A	A	A	A
1	1	0	1	D	D	D	A	A	A	A	A	A	A	A	A	A	A	A
1	1	1	0	D	D	A	A	A	A	A	A	A	A	A	A	A	A	A
1	1	1	1	D	A	A	A	A	A	A	A	A	A	A	A	A	A	A

When selecting any one pin from pins ANI0 to ANI14 and ANI16 to ANI20 to perform A/D conversion, do not access ports P20 to P27, P03, P02, P147, P120, P100, P150 to P156 during A/D conversion. Doing so may decrease the accuracy of the conversion.

3.4 Interrupts

When using the M16C/62P Group MCU in single sweep mode, an interrupt is generated after A/D conversion for all pins selected is completed. However, when using the RL78/G14 MCU, an interrupt is generated when the A/D conversion for each pin is completed.

4. Sample Program

4.1 Specifications

This chapter explains a sample program for RL78/G14 for migration of the M16C/62P Group in the single sweep mode, repeat sweep mode 0, or repeat sweep mode.

Table 4.1 lists the combination of the RL78/G14 channel selection mode and conversion operating mode compatible with the M16C/62P Group operating mode when using this sample program.

Table 4.1 Operating Mode Compatibility When Using the Sample Program

M16C/62P Group	RL78/G14	
	Channel selection mode	Conversion Operating Mode
Single sweep mode	Scan mode	One-shot conversion mode
Repeat sweep mode 0	Scan mode	Sequential conversion mode
Repeat sweep mode 1 (Note 1)	Select mode	One-shot conversion mode

Note
1. This mode is handled by software sequencing.

Table 4.2 lists the peripheral functions used and their applications.
Figure 4.1 shows the operation overview.

Table 4.2 Peripheral Functions Used and Their Applications

Peripheral function	Application
DTC	Transfer the A/D converted result to the RAM
A/D converter	Perform A/D conversion on analog input voltage

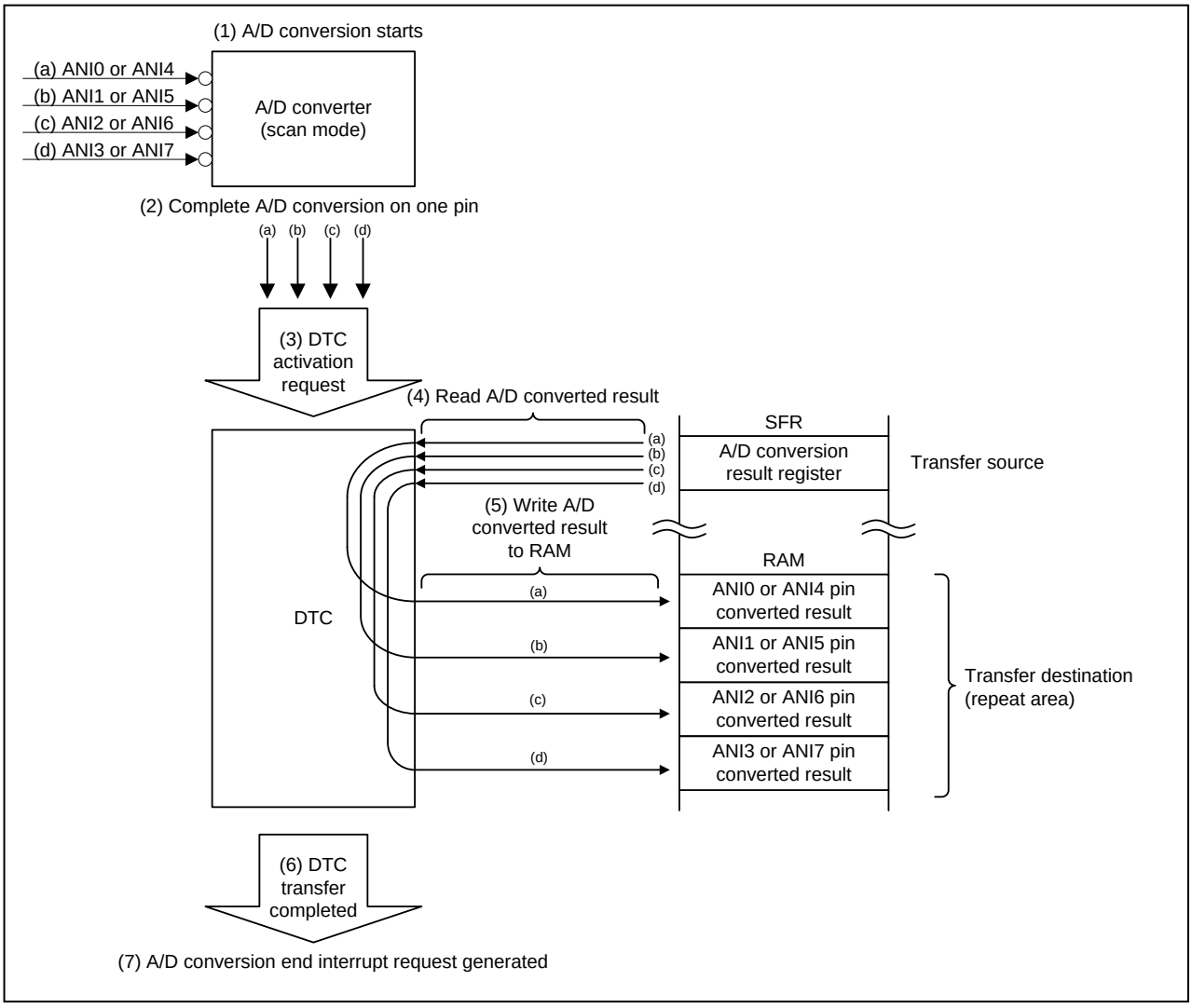


Figure 4.1 Operation Overview

4.1.1 Example of Migration from the Single Sweep Mode

To handle the single sweep mode function of the M16C/62P Group by RL78/G14, DTC transfer (repeat mode) and the AD converter (software trigger, scan mode for channel selection mode, and one-shot conversion mode for conversion operating mode) are used.
A/D conversion is performed on analog input voltage which is input to pins P20/ANI0 to P23/ANI3 and P24/ANI4 to P27/ANI7 in scan mode and one-shot conversion mode. DTC transfer is used to store the A/D converted value assigned to each pin to the RAM.
A/D conversion is performed for individual pins successively. Every time A/D conversion for a pin is completed, the converted result is stored to the 10-bit A/D conversion result register (ADCR), the DTC is activated, and the A/D converted result is transferred from the ADCR register to the RAM. When A/D conversion and DTC transfer for all of the above pins are completed, an A/D conversion end interrupt request is generated.

4.1.2 Example of Migration from the Repeat Sweep Mode 0

To adapt the repeat sweep mode 0 function of the M16C/62P Group to RL78/G14, DTC transfer (repeat mode) and the AD converter (software trigger, scan mode for channel selection mode, and sequential conversion mode for conversion operating mode) are used.
A/D conversion is performed on analog input voltage which is input to pins P20/ANI0 to P23/ANI3 and P24/ANI4 to P27/ANI7 in scan mode and sequential conversion mode. DTC transfer is used to store the A/D converted value assigned to each pin to the RAM.
A/D conversion is performed for individual pins successively. Every time A/D conversion for a pin is completed, the converted result is stored to the 10-bit A/D conversion result register (ADCR), the DTC is activated, and the A/D converted result is transferred from the ADCR register to the RAM. When A/D conversion and DTC transfer for all of the above pins are completed, an A/D conversion end interrupt request is generated.

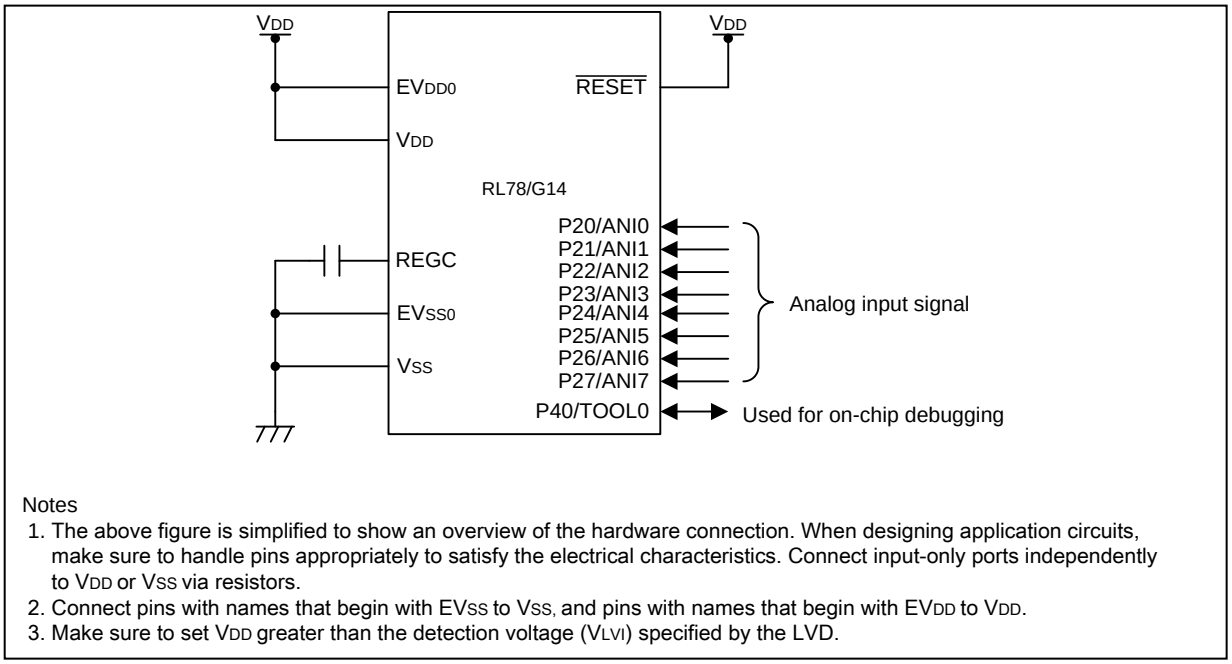
4.1.3 Example of Migration from the Repeat Sweep Mode 1

To accommodate the repeat sweep mode 1 function of the M16C/62P Group to RL78/G14, software sequencing should be performed by using the AD converter (software trigger, select mode for channel selection mode, and one-shot conversion mode for conversion operating mode).
A/D conversion is performed on analog input voltage which is input to pins P20/ANI0 to P27/ANI7 in select mode and one-shot conversion mode. Every time A/D conversion for a pin is completed, the conversion result is stored in the 10-bit AD conversion result register (ADCR) corresponding to the pin and an A/D conversion end interrupt is generated.
A/D conversion is executed in the order of ANI0, ANI1, ANI0, ANI2 through to ANI0, ANI7, and then the conversion is repeated in the same order starting again from ANI0, ANI1.

4.2 Hardware

4.2.1 Hardware Configuration

Figure 4.2 shows the hardware configuration used for this sample program.



Notes
1. The above figure is simplified to show an overview of the hardware connection. When designing application circuits, make sure to handle pins appropriately to satisfy the electrical characteristics. Connect input-only ports independently to VDD or VSS via resistors.
2. Connect pins with names that begin with EVSS to VSS, and pins with names that begin with EVDD to VDD.
3. Make sure to set VDD greater than the detection voltage (VLVI) specified by the LVD.

Figure 4.2 Hardware Configuration

4.2.2 Pins Used

Table 4.3 lists the pins used and their functions.

Table 4.3 Pins Used and Their Functions

Pin name	I/O	Function
P20/ANI0	Input	A/D converter input (ANI0)
P21/ANI1	Input	A/D converter input (ANI1)
P22/ANI2	Input	A/D converter input (ANI2)
P23/ANI3	Input	A/D converter input (ANI3)
P24/ANI4	Input	A/D converter input (ANI4)
P25/ANI5	Input	A/D converter input (ANI5)
P26/ANI6	Input	A/D converter input (ANI6)
P27/ANI7	Input	A/D converter input (ANI7)

4.3 Software

4.3.1 Operation Overview

(1) Example of Migration from the Single Sweep Mode

For example of migration from the single sweep mode of the M16C/62P Group, in this sample program, the results of eight pins that are A/D converted in the scan mode are stored to RAM using DTC transfer. The transfer destination (ad_value[0] to ad_value[3]) is set as a repeat area by using DTC in its repeat mode, and the A/D converted results of the eight pins are stored to RAM successively.
When A/D conversion of the ANI0 pin is completed, the first DTC transfer from the transfer source address (ADCR register (FFFF1EH and FFFF1FH)) to the transfer destination address (ad_value[0] (FFF500H to FFF501H)) is performed. When A/D conversion of the ANI1 pin is completed, the second DTC transfer is performed. Since the transfer destination is set as a repeat area, the A/D converted result is transferred to ad_value[1] (FFF502H to FFF503H). In the same procedure, DTC transfer for the A/D converted results of pins ANI3 and ANI4 is performed. When the fourth DTC transfer is completed, an A/D conversion end interrupt is generated.
After the A/D converted results for four times are stored using the A/D conversion end interrupt, the ADS register is changed to set ANI4 to 7 pins as conversion targets and A/D conversion is started again. After that, when A/D conversion of the ANI4 pin is completed, DTC transfer is performed in the same way as above. When the fourth DTC transfer is completed, the A/D conversion end interrupt is generated.

Table 4.4 lists the DTC settings and Table 4.5 lists the A/D converter settings.

Table 4.4 DTC Settings

Function name	Setting value
	Control data 0
Transfer mode	Repeat mode
Repeat mode interrupt	Enabled
Source address control	Fixed
Destination address control	Repeat area
Chain transfer	Disabled
Transfer block size	2 bytes
Number of DTC transfers	4
Transfer source address	ADCR register address (FFF1EH)
Transfer destination address	Start address of ad_value[] (FF500H)

Table 4.5 A/D Converter Settings

Setting item	Setting value
Conversion clock (f_{AD})	f_{CLK}/64
A/D conversion modes	• A/D conversion trigger mode: Software trigger mode • A/D conversion channel selection mode: Scan mode • A/D conversion operating mode: One-shot conversion mode
Resolution	10 bits
Analog input channels	• Set ANI0 to 3 as conversion targets for initial setting and after A/D conversion for ANI4 to 7 is completed. • Scan 0: ANI0 • Scan 1: ANI1 • Scan 2: ANI2 • Scan 3: ANI3 • Set ANI4 to 7 as conversion targets when an A/D conversion end interrupt is generated. • Scan 0: ANI4 • Scan 1: ANI5 • Scan 2: ANI6 • Scan 3: ANI7
Conversion result comparison upper limit (ADUL register)	FFH
Conversion result comparison lower limit (ADLL register)	00H
Conversion result upper limit/lower limit check	INTAD is generated when ADLL register ≤ ADCR register ≤ ADUL register

(1) Perform the initial setting for the A/D converter and DTC.
(2) Set the ADCS bit in the ADM0 register to 1 (conversion operation enabled) to start A/D conversion.
(3) When A/D conversion of pins ANI0, ANI1, ANI2, and ANI3 is completed, DTC is activated.
(4) DTC reads the A/D converted results from the ADCR register and transfers them to RAM (ad_value[0] to ad_value[3]) corresponding to each pin.
(5) When the fourth DTC transfer is completed, an A/D conversion end interrupt is generated. The A/D converted results of ad_value[0] to ad_value[3] are right-shifted 6 bits in an interrupt handling routine and stored to variables an0_value to an3_value.
(6) After the A/D converted results are stored, change the ADS register to set pins ANI4 to 7 as conversion targets.
(7) Set the ADCS bit in the ADM0 register to 1 (conversion operation enabled) to start A/D conversion.
(8) When A/D conversion of pins ANI4, ANI5, ANI6, and ANI7 is completed, DTC is activated.
(9) DTC reads the A/D converted results from the ADCR register and transfers them to RAM (ad_value[0] to ad_value[3]) corresponding to each pin.
(10) When the fourth DTC transfer is completed, an A/D conversion end interrupt is generated. The A/D converted results of ad_value[0] to ad_value[3] are right-shifted 6 bits in an interrupt handling routine and stored to variables an4_value to an7_value.

Figure 4.3 shows a timing diagram of DTC transfer and A/D conversion. Figure 4.4 illustrates the relationship between the ADCR register and RAM.

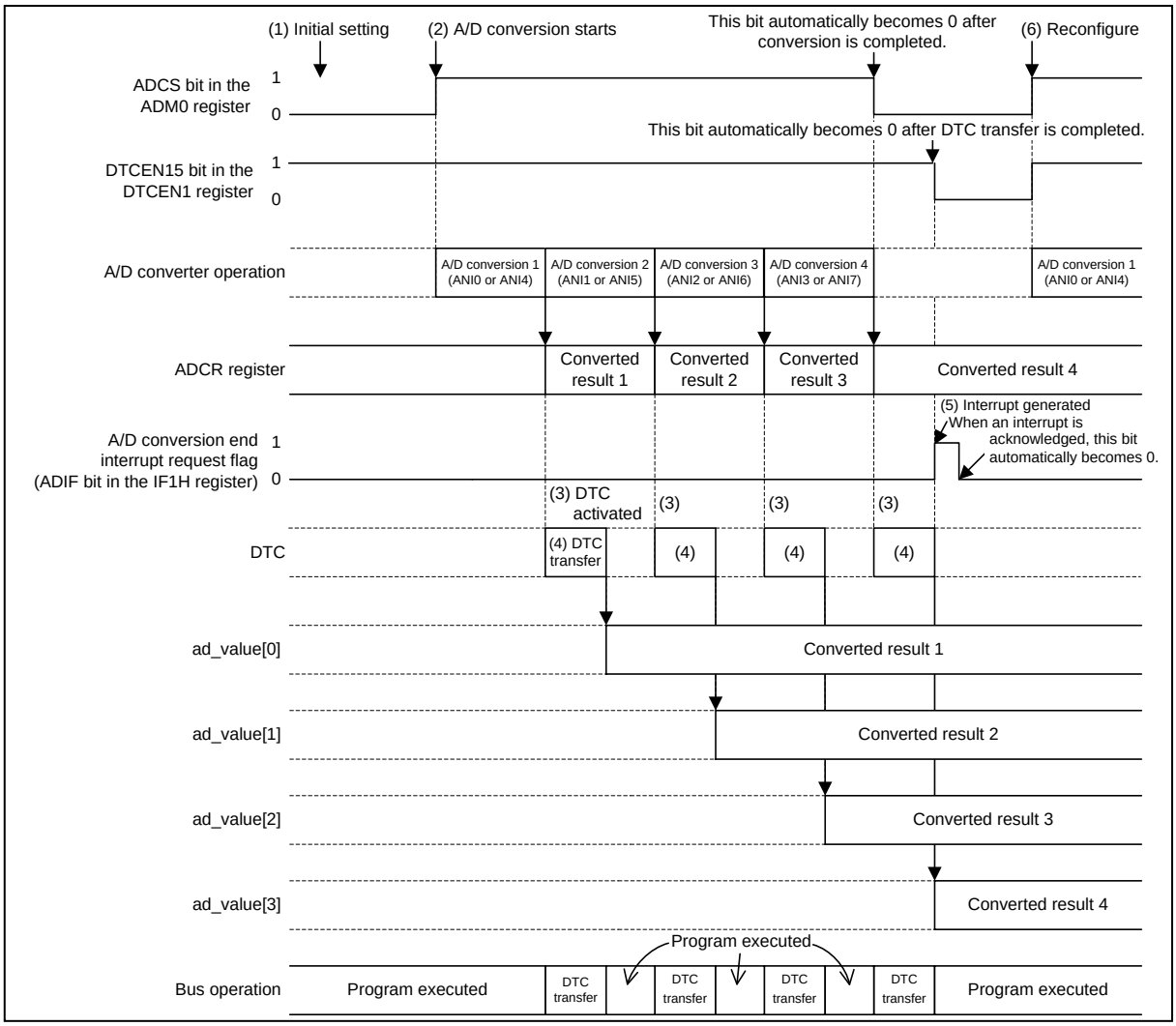


Figure 4.3 Timing Diagram of DTC Transfer and A/D Conversion (Example of Migration from the Single Sweep Mode)

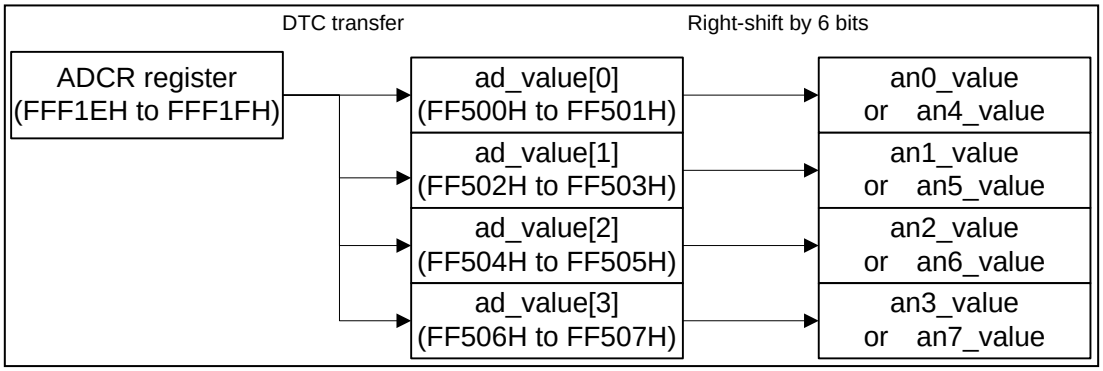


Figure 4.4 Relationship between the ADCR Register and RAM (Example of Migration from the Single Sweep Mode)

(2) Example of Migration from the Repeat Sweep Mode 0

For example of migration from the repeat sweep mode 0 of the M16C/62P Group, in this sample program, the results of eight pins that are A/D converted in the scan mode are stored to RAM using DTC transfer. The transfer destination (ad_value[0] to ad_value[3]) is set as a repeat area by using DTC in its repeat mode, and the A/D converted results of the eight pins are stored to RAM successively.
When A/D conversion of the ANI0 pin is completed, the first DTC transfer from the transfer source address (ADCR register (FFFF1EH and FFFF1FH) to the transfer destination address (ad_value[0] (FFF500H to FFF501H)) is performed. When A/D conversion of the ANI1 pin is completed, the second DTC transfer is performed. Since the transfer destination is set as a repeat area, the A/D converted result is transferred to ad_value[1] (FFF502H to FFF503H). In the same procedure, DTC transfer for the A/D converted results of pins ANI3 and ANI4 is performed. When the fourth DTC transfer is completed, an A/D conversion end interrupt is generated.
After the A/D converted results for four times are stored using the A/D conversion end interrupt, the ADS register is changed to set ANI4 to 7 pins as conversion targets and A/D conversion is started again. After that, when A/D conversion of the ANI4 pin is completed, DTC transfer is performed in the same way as above. When the fourth DTC transfer is completed, the A/D conversion end interrupt is generated.

Table 4.6 lists the DTC settings and Table 4.7 lists the A/D converter settings.

Table 4.6 DTC Settings

Function name	Setting value
	Control data 0
Transfer mode	Repeat mode
Repeat mode interrupt	Enabled
Source address control	Fixed
Destination address control	Repeat area
Chain transfer	Disabled
Transfer block size	2 bytes
Number of DTC transfers	4
Transfer source address	ADCR register address (FFF1EH)
Transfer destination address	Start address of ad_value[] (FF500H)

Table 4.7 A/D Converter Settings

Setting item	Setting value
Conversion clock (f_{AD})	f_{CLK}/64
A/D conversion modes	• A/D conversion trigger mode: Software trigger mode • A/D conversion channel selection mode: Scan mode • A/D conversion operating mode: Sequential conversion mode
Resolution	10 bits
Analog input channels	Switch input channels every time an AD conversion end interrupt is generated. • ANI0 to 3 • Scan 0: ANI0 • Scan 1: ANI1 • Scan 2: ANI2 • Scan 3: ANI3 • ANI4 to 7 • Scan 0: ANI4 • Scan 1: ANI5 • Scan 2: ANI6 • Scan 3: ANI7
Conversion result comparison upper limit (ADUL register)	FFH
Conversion result comparison lower limit (ADLL register)	00H
Conversion result upper limit/lower limit check	INTAD is generated when ADLL register ≤ ADCR register ≤ ADUL register

(1) Perform the initial setting for the A/D converter and DTC.
(2) Set the ADCS bit in the ADM0 register to 1 (conversion operation enabled) to start A/D conversion.
(3) When A/D conversion of pins ANI0, ANI1, ANI2, and ANI3 is completed, DTC is activated
(4) DTC reads the A/D converted results from the ADCR register and transfers them to RAM (ad_value[0] to ad_value[3]) corresponding to each pin.
(5) When the fourth DTC transfer is completed, DTC is stopped and an A/D conversion end interrupt is generated. The A/D converted results of ad_value[0] to ad_value[3] are right-shifted 6 bits in an interrupt handling routine and stored to variables an0_value to an3_value.
(6) After the A/D converted results are stored, change the ADS register to set pins ANI4 to 7 as conversion targets.
(7) Set the DTCEN15 bit in the DTCEN1 register to 1 (activation enabled) to enable activation of DTC again.
(8) When A/D conversion of pins ANI4, ANI5, ANI6, and ANI7 is completed, DTC is activated.
(9) DTC reads the A/D converted results from the ADCR register and transfers them to RAM (ad_value[0] to ad_value[3]) corresponding to each pin. D
(10) When the fourth DTC transfer is completed, an A/D conversion end interrupt is generated. The A/D converted results of ad_value[0] to ad_value[3] are right-shifted 6 bits in an interrupt handling routine and stored to variables an4_value to an7_value.
(11) After the A/D converted results are stored, change the ADS register to set pins ANI0 to 3 as conversion targets.
(12) Set the DTCEN15 bit in the DTCEN1 register to 1 (activation enabled) to enable activation of DTC again.
(13) After that, repeat procedures (3) to (12).

Figure 4.5 shows a timing diagram of DTC transfer and A/D conversion. Figure 4.6 illustrates the relationship between the ADCR register and RAM.

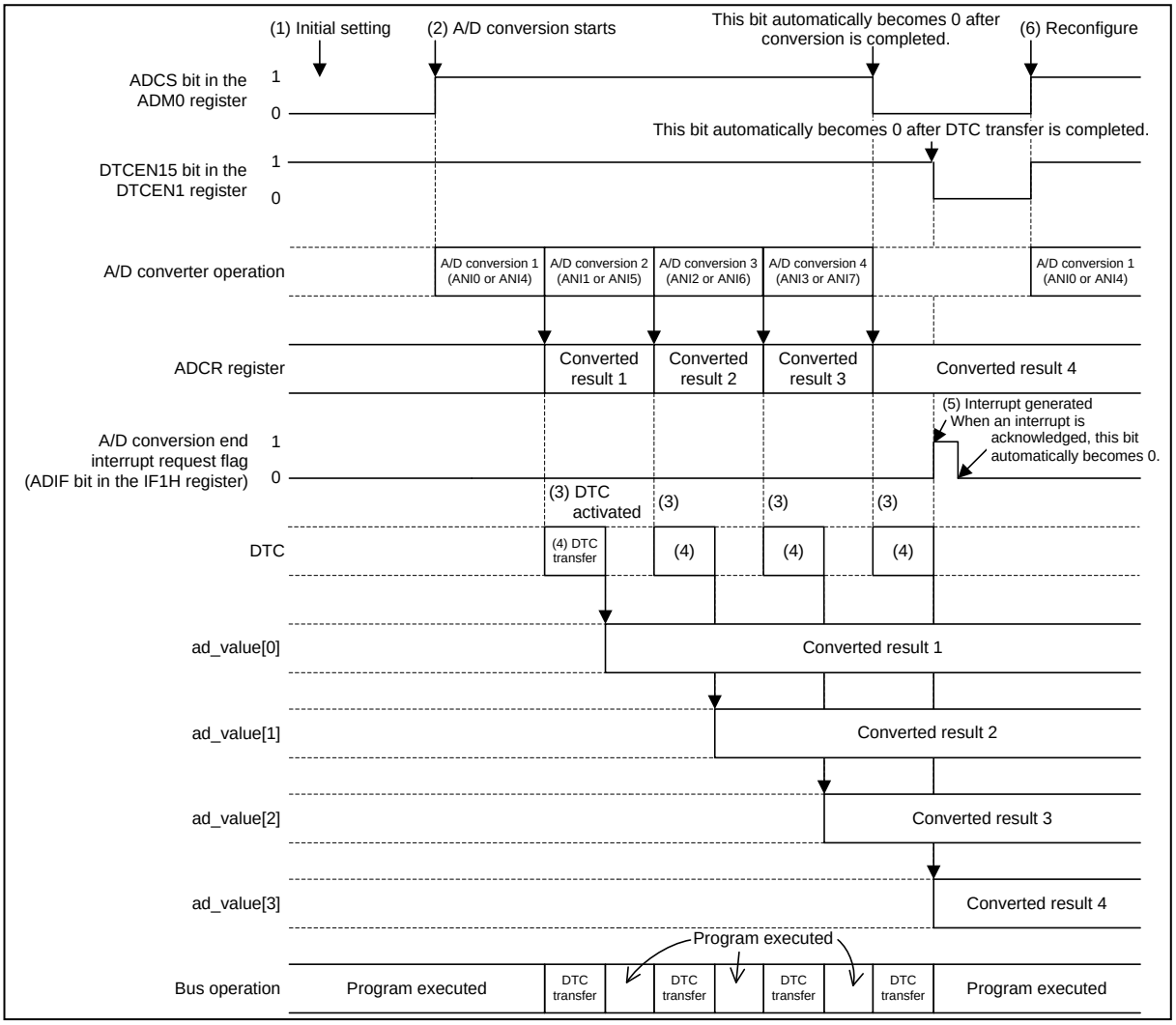


Figure 4.5 Timing Diagram of DTC Transfer and A/D Conversion (Example of Migration from the Repeat Sweep Mode 0)

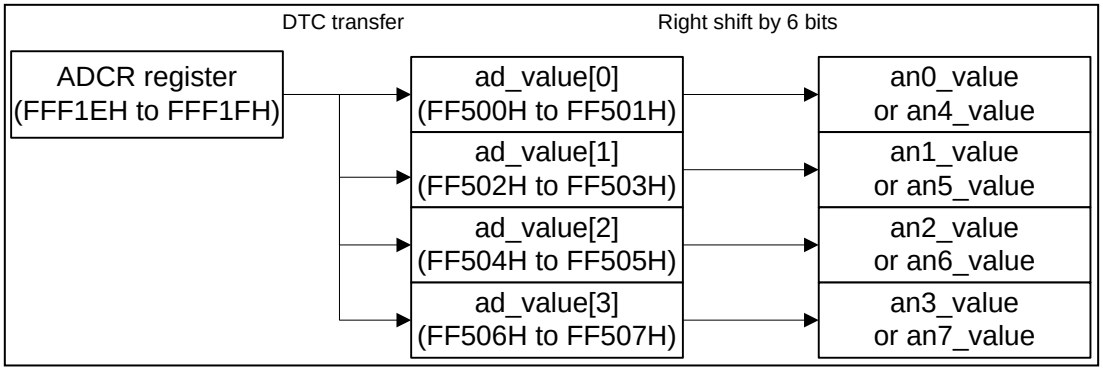


Figure 4.6 Relationship between the ADCR Register and RAM (Example of Migration from the Repeat Sweep Mode 0)

(11) Example of Migration from the Repeat Sweep Mode 1

For example of migration from the repeat sweep mode 1 of the M16C/62P Group, in this sample program, the A/D converted results of the pins specified in the select mode are stored using A/D conversion end interrupts. When A/D conversion of the ANI0 pin is completed, an A/D conversion end interrupt is generated. After the A/D converted result is stored to ad_value[0] by using the A/D conversion end interrupt, the ADS register is changed to set the ANI1 pin as conversion target and A/D conversion is started again.
When A/D conversion of the ANI1 pin is completed, an A/D conversion end interrupt is generated in the same way as above. After the A/D converted result is stored to ad_value[1], the ADS register is changed to set the ANI0 pin as conversion target and A/D conversion is started again. After the A/D converted result is stored to ad_value[0] by using the next A/D conversion end interrupt, the ADS register is changed to set the ANI2 pin as conversion target.
The above procedures are repeated in the order of ANI0, ANI1, ANI0, ANI2 through to ANI0, ANI7, and then the conversion is repeated in the same order starting again from ANI0, ANI1. That is, this order of ANI0, ANI1, ANI0, ANI2 through to ANI0, ANI7 is defined as a set of operations to be repeated.

Table 4.8 lists the A/D converter settings.

Table 4.8 A/D Converter Settings

Setting item	Setting value
Conversion clock (f_{AD})	f_{CLK}/64
A/D conversion modes	• A/D conversion trigger mode: Software trigger mode • A/D conversion channel selection mode: Select mode • A/D conversion operating mode: One-shot conversion mode
Resolution	10 bits
Analog input channels	Every time an AD conversion end interrupt is generated, input channels are switched in the order of ANI0, ANI1, ANI0, ANI2 through to ANI0, ANI7 (and then repeated in the same order starting again from ANI0, ANI1.)
Conversion result comparison upper limit (ADUL register)	FFH
Conversion result comparison lower limit (ADLL register)	00H
Conversion result upper limit/lower limit check	INTAD is generated when ADLL register ≤ ADCR register ≤ ADUL register

(1) Perform the initial setting for the A/D converter and DTC.
(2) Set the ADCS bit in the ADM0 register to 1 (conversion operation enabled) to start A/D conversion.
(3) When A/D conversion of ANI0 pin is completed, an A/D conversion end interrupt is generated. The A/D converted result is stored to ad_value[0] in an interrupt handling routine.
(4) After the A/D converted results are stored, change the ADS register to set the ANI1 pin as conversion target.
(5) Set the ADCS bit in the ADM0 register to 1 (conversion operation enabled) to start A/D conversion.
(6) When A/D conversion of ANI1 pin is completed, an A/D conversion end interrupt is generated. The A/D converted result is stored to ad_value[1] in an interrupt handling routine.
(7) After the A/D converted results are stored, change the ADS register to set the ANI0 pin as conversion target.
(8) Set the ADCS bit in the ADM0 register to 1 (conversion operation enabled) to start A/D conversion.
(9) In the same way as (3), when A/D conversion of ANI0 pin is completed, an A/D conversion end interrupt is generated. The A/D converted result is stored to ad_value[0] in an interrupt handling routine.
(10) After the A/D converted results are stored, change the ADS register to set the ANI2 pin as conversion target.
(11) Set the ADCS bit in the ADM0 register to 1 (conversion operation enabled) to start A/D conversion.
(12) When A/D conversion of ANI2 pin is completed, an A/D conversion end interrupt is generated. The A/D converted result is stored to ad_value[2] in an interrupt handling routine.
(13) After the A/D converted results are stored, change the ADS register to set the ANI0 pin as conversion target.
(14) Repeat procedures (2) to (13) in the order of ANI0, ANI1, ANI0, ANI2 through to ANI0, ANI7, and then in the same order starting again from ANI0, ANI1.
(15) The A/D converted results of ad_value[0] to ad_value[7] are right-shifted 6 bits in an interrupt handling routine and stored to variables an0_value to an7_value.

Figure 4.7 illustrates the relationship between the ADCR register and RAM.

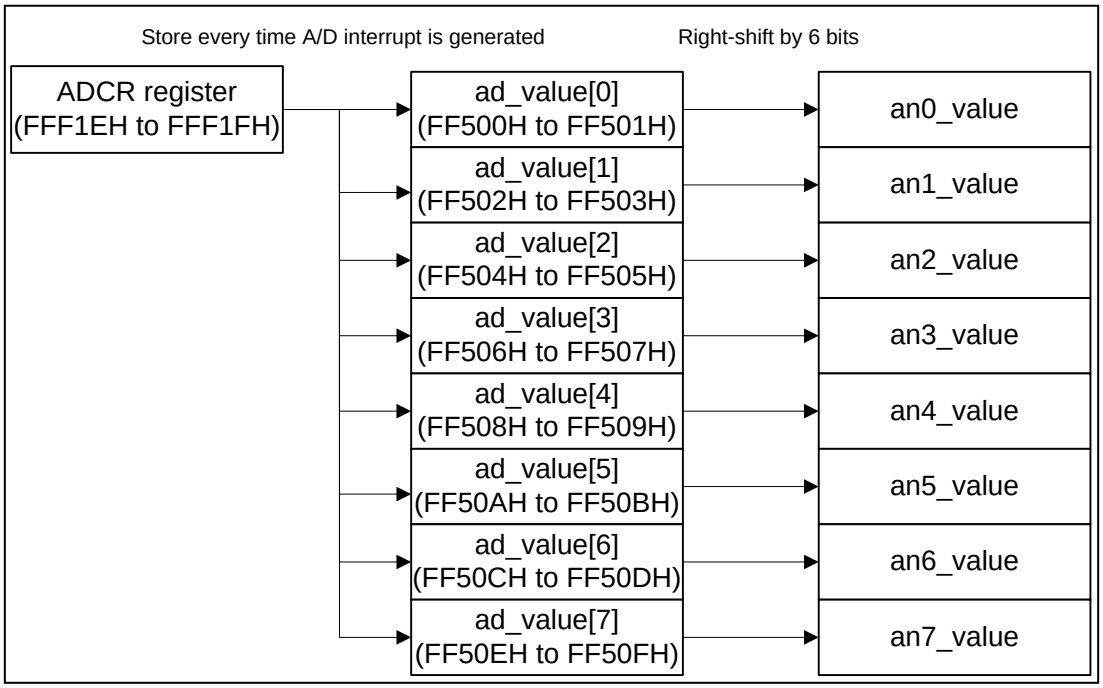


Figure 4.7 Relationship between the ADCR Register and RAM (Example of Migration from the Repeat Sweep Mode 1)

4.3.2 Option Byte Setting

Table 4.9 lists the option byte setting.

Table 4.9 Option Byte Setting

Address	Setting value	Content
000C0H/010C0H	11101111B	Stops the watchdog timer (counting is stopped after a reset is released)
000C1H/010C1H	01111111B	Sets the LVD in reset mode Detection voltage: 2.81 V at the rising edge, 2.75 V at the falling edge
000C2H/010C2H	11101000B	High-speed on-chip oscillator HS mode 32 MHz
000C3H/010C3H	10000100B	Enables on-chip debugging

4.3.3 Constant

Table 4.10 lists constants used in the sample code.

Table 4.10 Constant Used in the Sample Code

Constant name	Setting value	Content
ad_value	0FF500H	DTC transfer destination address
AD_MODE_SEL	Any value	Select an operating mode from below. 0: Setting for migration from single sweep mode 1: Setting for migration from repeat sweep mode 0 2: Setting for migration from repeat sweep mode 2

4.3.4 Variables

Table 4.11 lists the global variables.

Table 4.11 Global Variables

Type	Variable name	Content	Function used
unsigned short	ad_value[8]	A/D converted result storage address of ANI0 to ANI7	r_adc_interrupt
unsigned short	an0_value	Store A/D converted result of ANI0	r_adc_interrupt
unsigned short	an1_value	Store A/D converted result of ANI1	r_adc_interrupt
unsigned short	an2_value	Store A/D converted result of ANI2	r_adc_interrupt
unsigned short	an3_value	Store A/D converted result of ANI3	r_adc_interrupt
unsigned short	an4_value	Store A/D converted result of ANI4	r_adc_interrupt
unsigned short	an5_value	Store A/D converted result of ANI5	r_adc_interrupt
unsigned short	an6_value	Store A/D converted result of ANI6	r_adc_interrupt
unsigned short	an7_value	Store A/D converted result of ANI7	r_adc_interrupt
unsigned char	ad_ch_sel	A/D conversion target channel	r_adc_ram_init r_adc_int_repeat_mode_1
unsigned char	ad_ch_tgr	A/D conversion target switch flag	r_adc_ram_init r_adc_int_oneshot r_adc_int_repeat_mode_0 r_adc_int_repeat_mode_1
unsigned char	ad_mode	A/D conversion mode	r_adc_ram_init r_adc_interrupt R_ADC_Func_Init

4.3.5 Functions

Table 4.12 lists the functions.

Table 4.12 Function

Function name	Outline
hdwinit	Initial setting
R_Systeminit	Initial setting of peripheral functions
R_CGC_Create	Initial setting of CPU
R_ADC_Create	Initial setting of the A/D converter
R_ADC_Func_Init	Initial setting depending on A/D conversion functions
R_ADC_Create_ONESHOT	Initial setting for migration from the single sweep mode
R_ADC_Create_REPEAT_MODE_0	Initial setting for migration from the repeat sweep mode 0
R_ADC_Create_REPEAT_MODE_1	Initial setting for migration from the repeat sweep mode 1
r_adc_ram_init	Initialization of variables associated with A/D conversion
R_DTC_Create	Initial setting of DTC
main	Main processing
R_DTCD0_Start	DTC activation
R_ADC_Start	A/D conversion start
r_adc_interrupt	A/D conversion interrupt
r_adc_int_oneshot	Interrupt handling for migration from the single sweep mode
r_adc_int_repeat_mode_0	Interrupt handling for migration from the repeat sweep mode 0
r_adc_int_repeat_mode_1	Interrupt handling for migration from the repeat sweep mode 1

4.3.6 Flowcharts

(1) Overall Flowchart

Figure 4.8 is an overall flowchart.

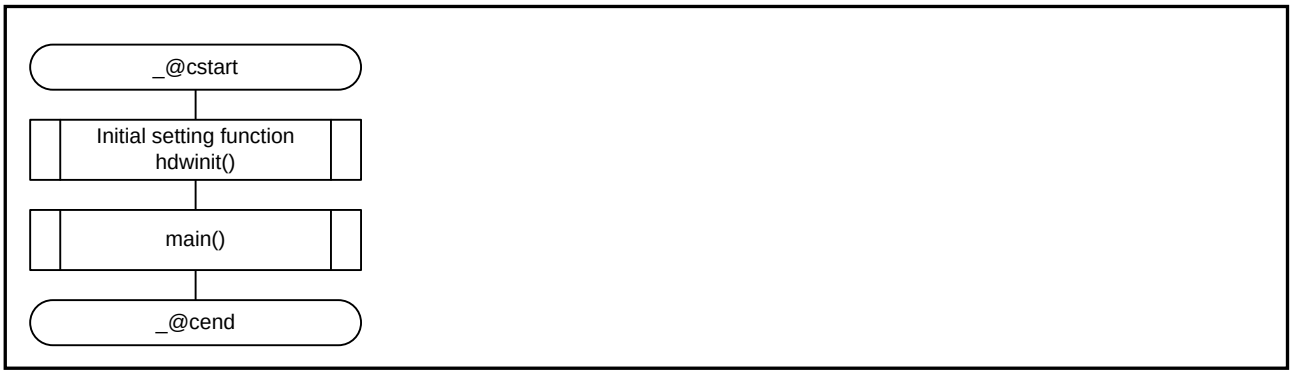


Figure 4.8 Overall Flowchart

(2) Initial Setting

Figure 4.9 shows the initial setting.

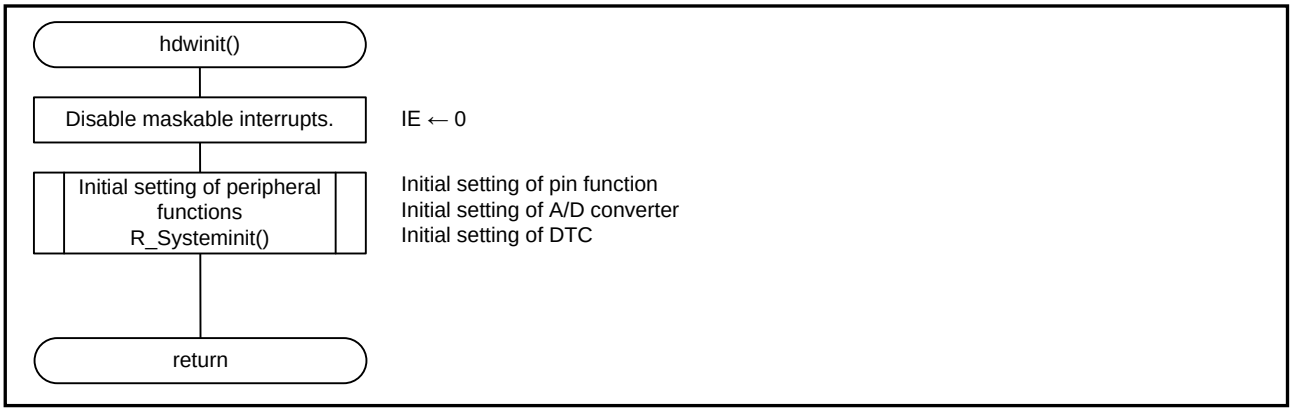


Figure 4.9 Initial Setting

(3) Initial Setting of Peripheral Functions

Figure 4.10 shows the initial setting of peripheral functions.

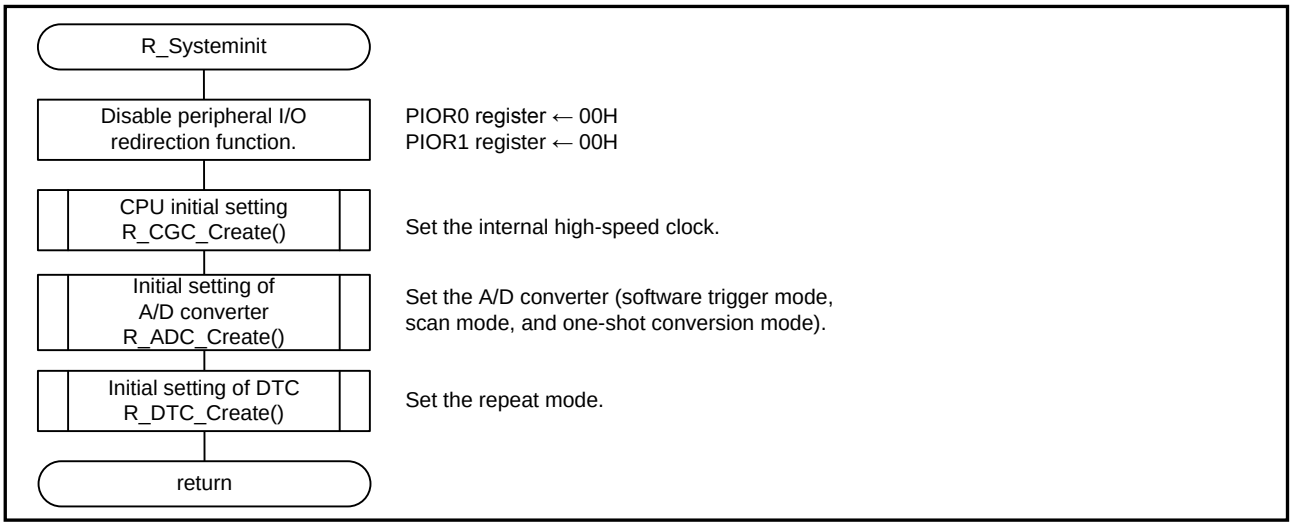


Figure 4.10 Initial Setting of Peripheral Functions

(4) Initial Setting of CPU

Figure 4.11 shows the initial setting of CPU.

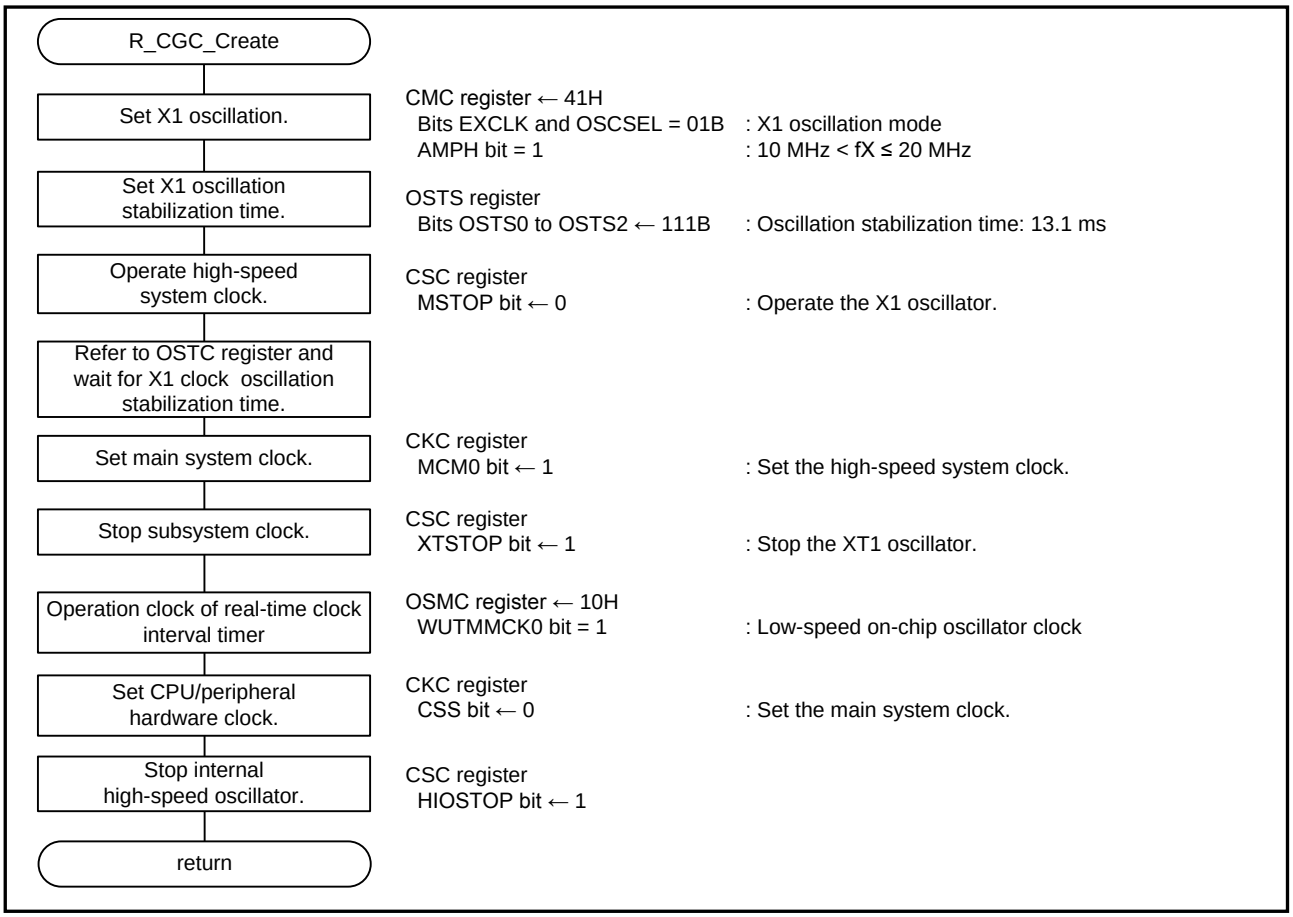


Figure 4.11 Initial Setting of CPU

(5) Initial Setting of the A/D Converter

Figure 4.12 shows the initial setting of the A/D converter.

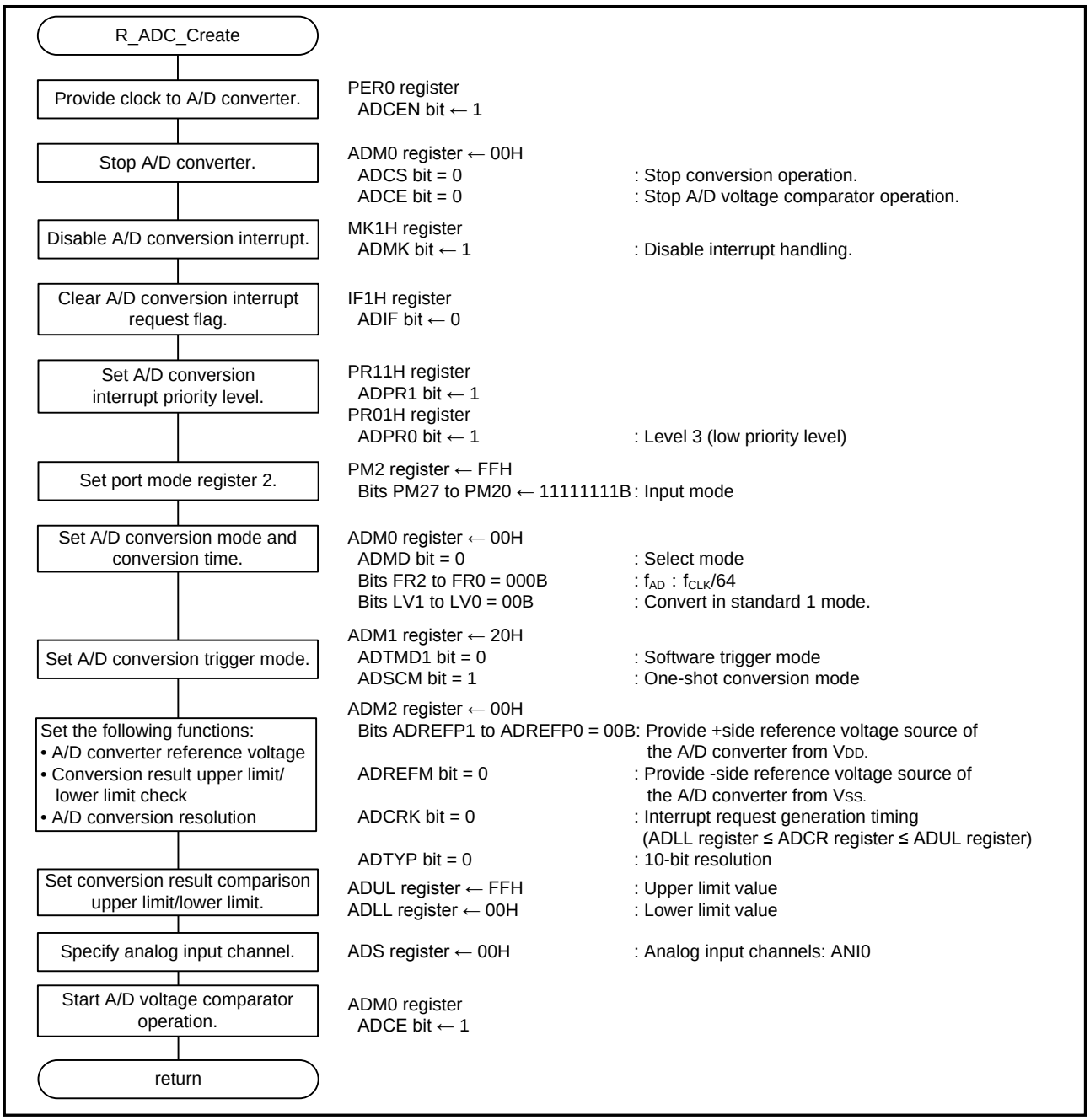


Figure 4.12 Initial Setting of the A/D Converter

(6) Initial Setting Depending on A/D Conversion Functions

Figure 4.13 is a flowchart for initial setting depending on A/D conversion functions.

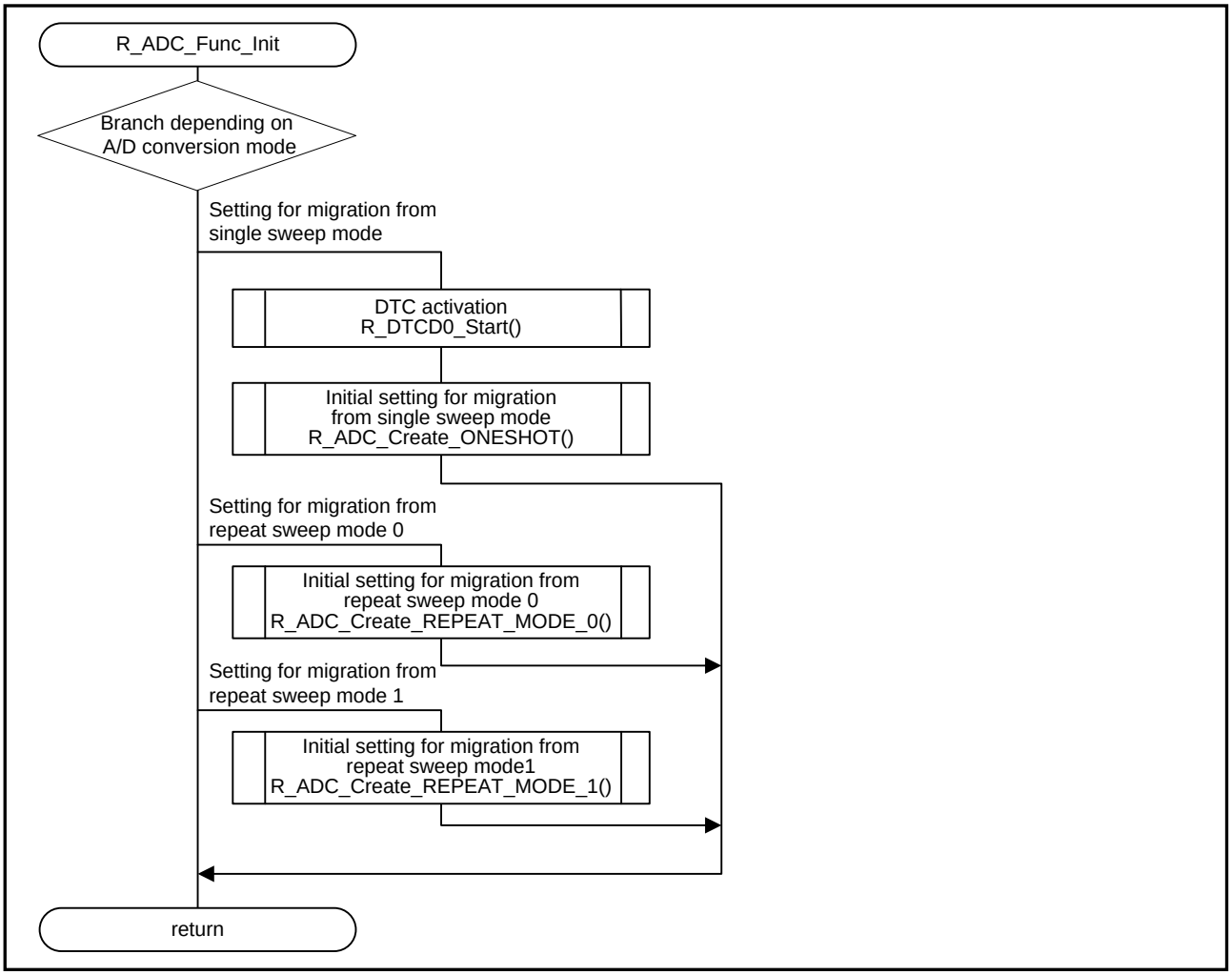


Figure 4.13 Initial Setting Depending on A/D Conversion Functions

(7) Initial Setting for Migration from the Single Sweep Mode

Figure 4.14 is a flowchart for initial setting for migration from the single sweep mode.

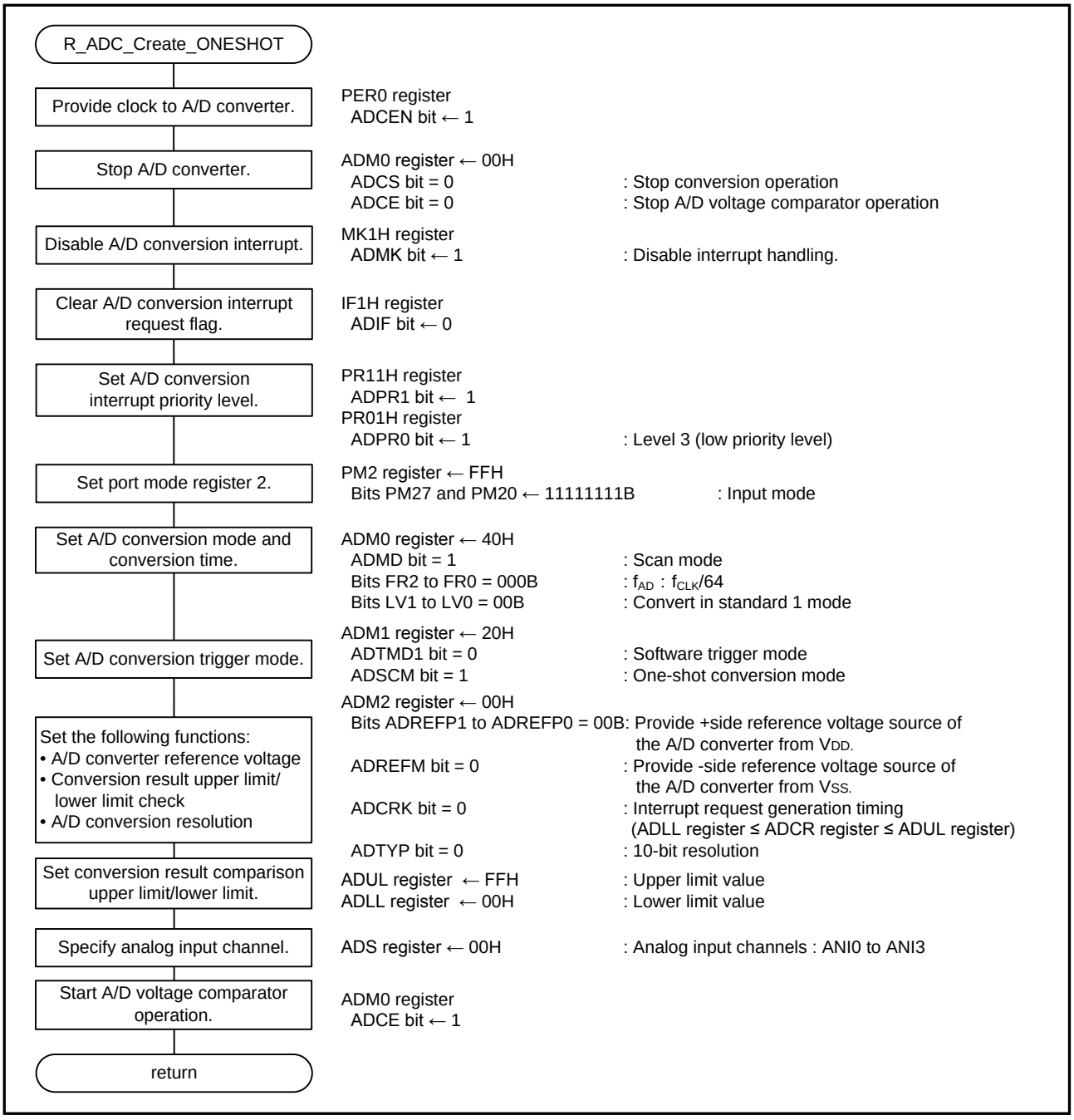


Figure 4.14 Initial Setting for Migration from the Single Sweep Mode

(8) Initial Setting for Migration from the Repeat Sweep Mode 0

Figure 4.15 is a flowchart for initial setting for migration from the repeat sweep mode 0.

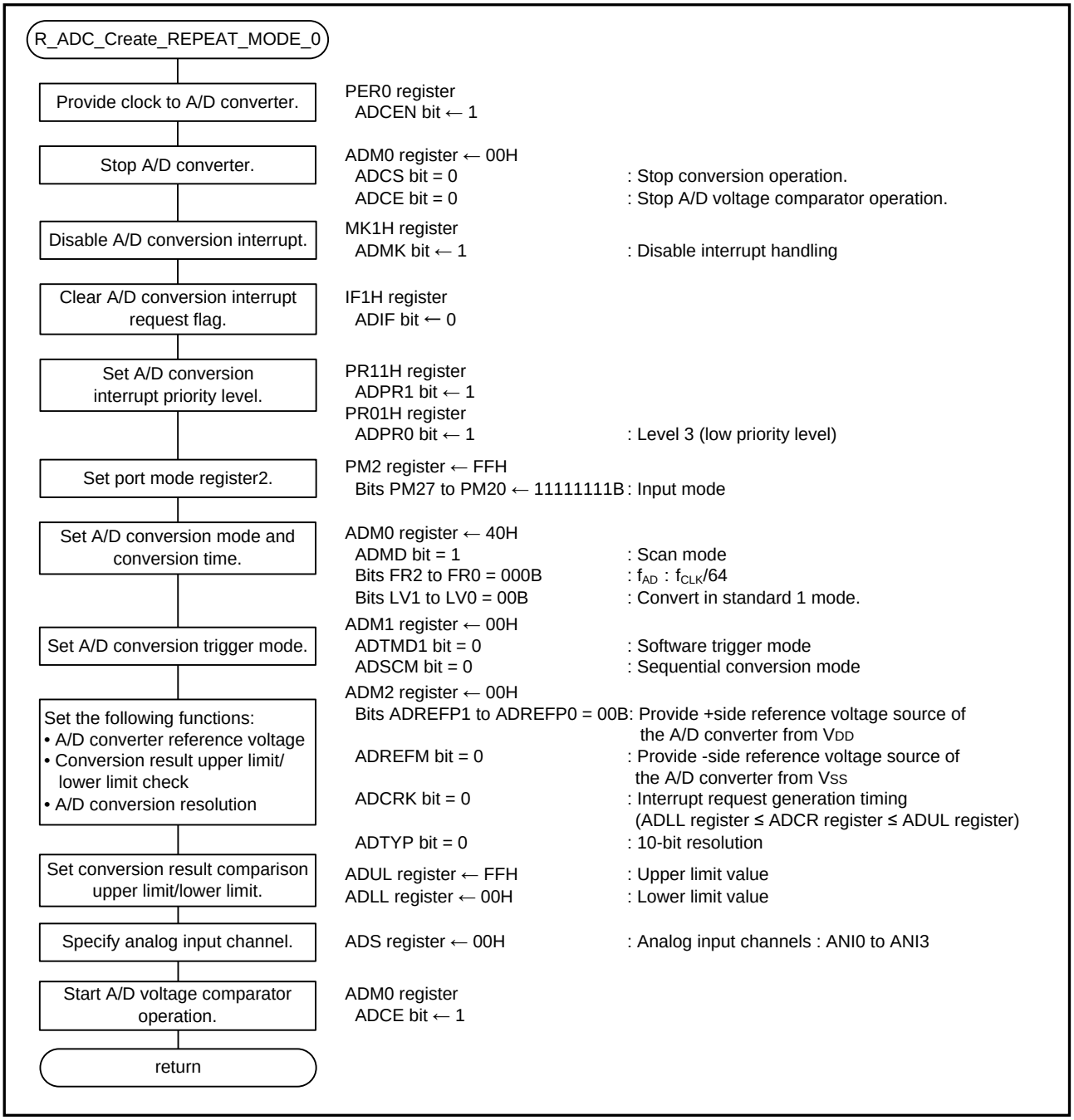


Figure 4.15 Initial Setting for Migration from the Repeat Sweep Mode 0

(9) Initial Setting for Migration from the Repeat Sweep Mode 1

Figure 4.16 is a flowchart for initial setting for migration from the repeat sweep mode 1.

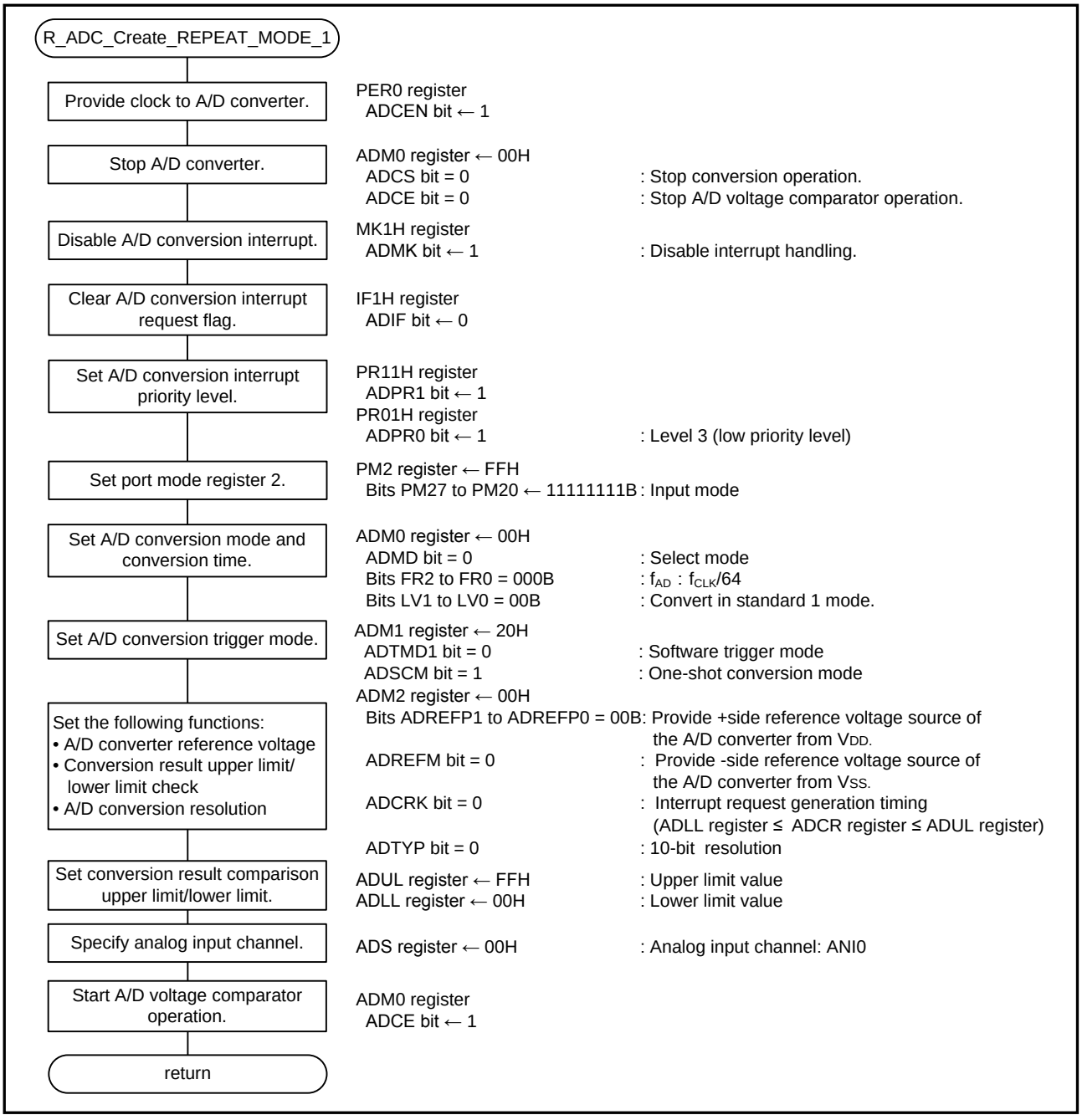


Figure 4.16 Initial Setting for Migration from the Repeat Sweep Mode 1

(10) Initialization of Variables Associated with A/D Conversion

Figure 4.17 shows initialization of variables associated with A/D conversion.

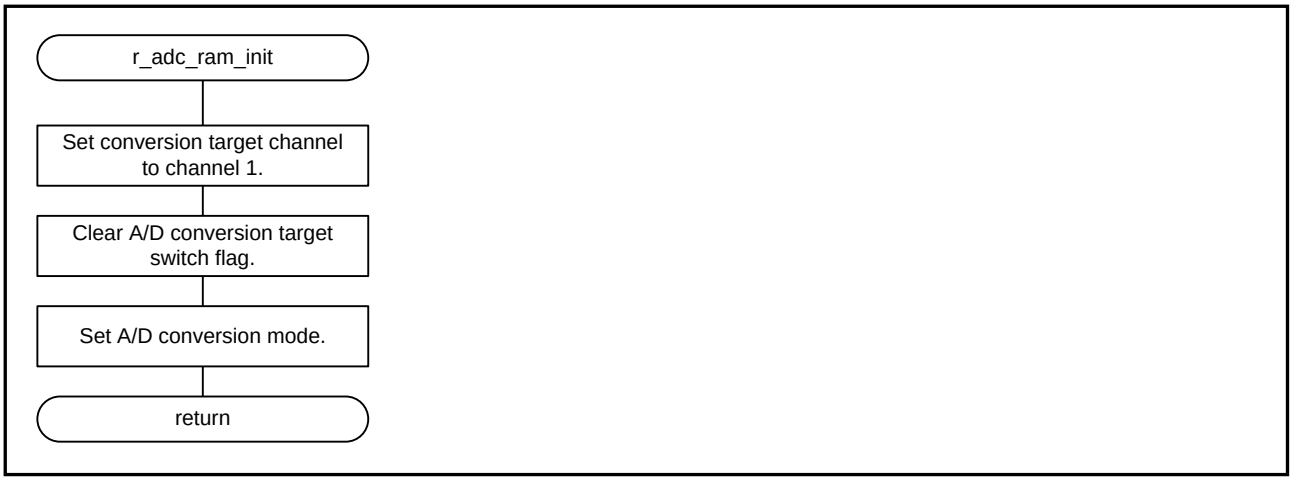


Figure 4.17 Initialization of Variables Associated with A/D Conversion

(11) Initial Setting of DTC

Figure 4.18 is the DTC initial setting flowchart, and Figure 4.19 shows the memory map of the DTC used area.

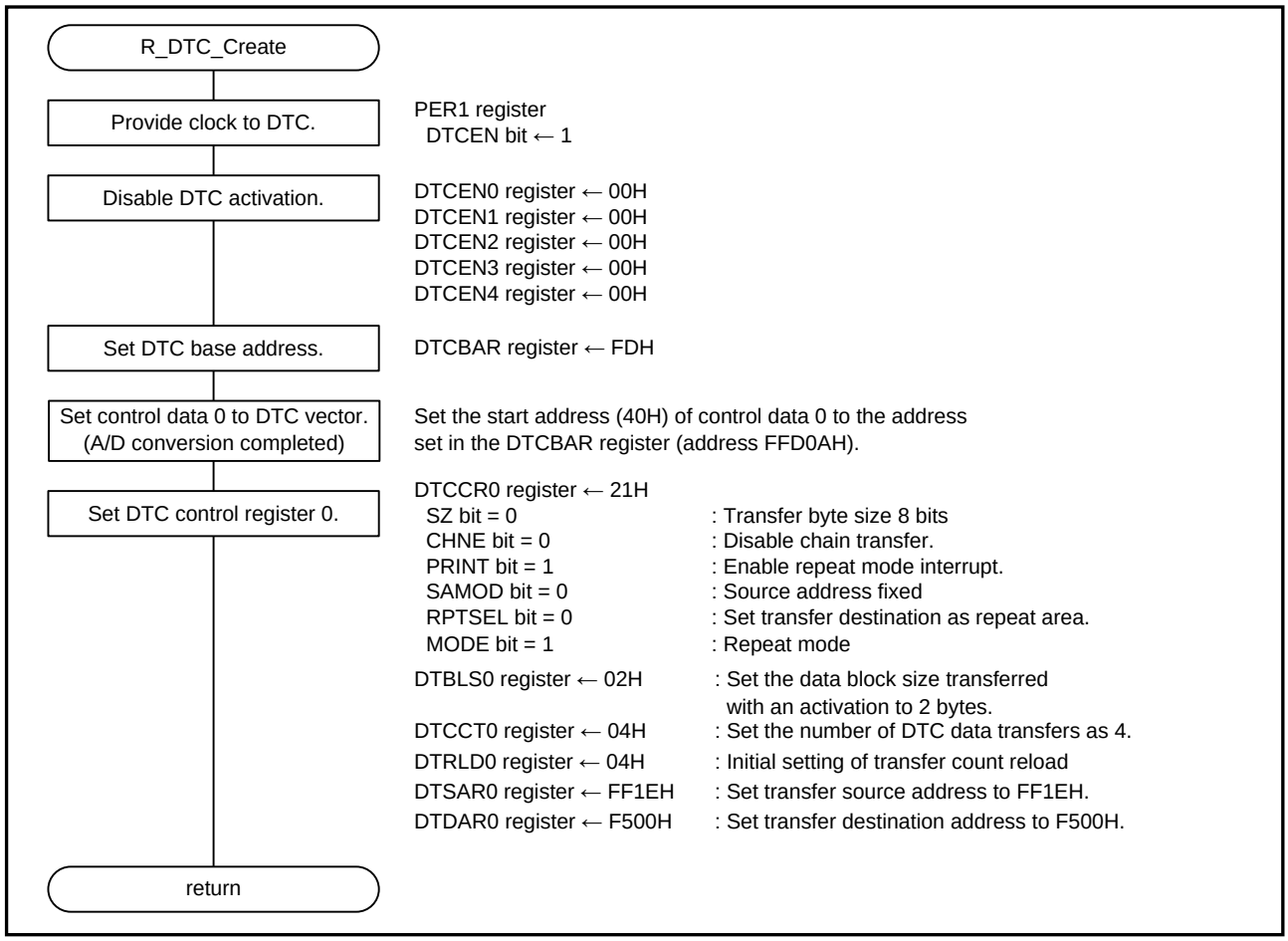


Figure 4.18 Initial Setting of DTC

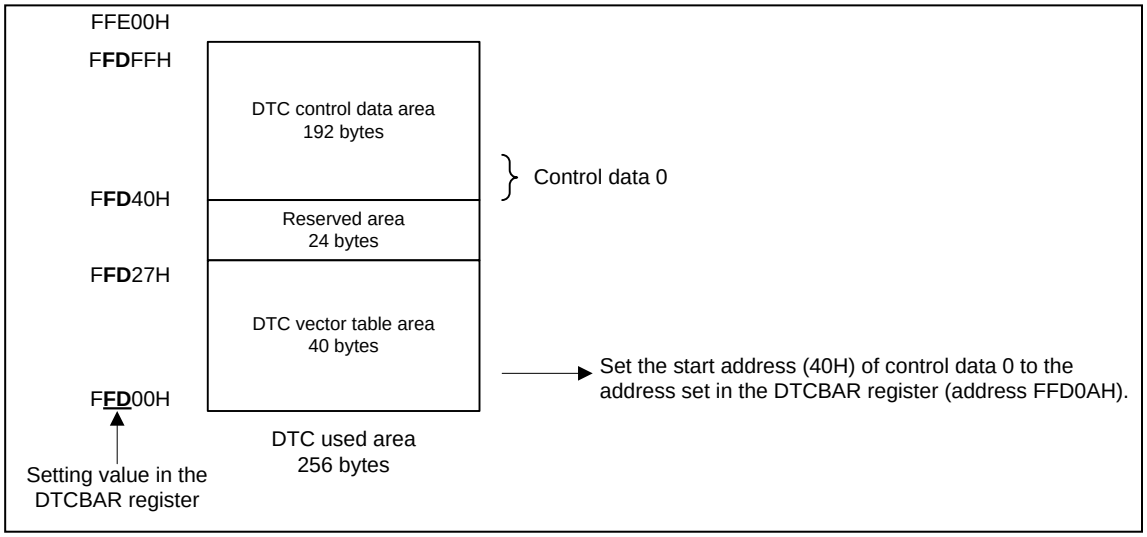


Figure 4.19 Memory Map of the DTC Used Area

(12) Main Processing

Figure 4.20 shows the main processing.

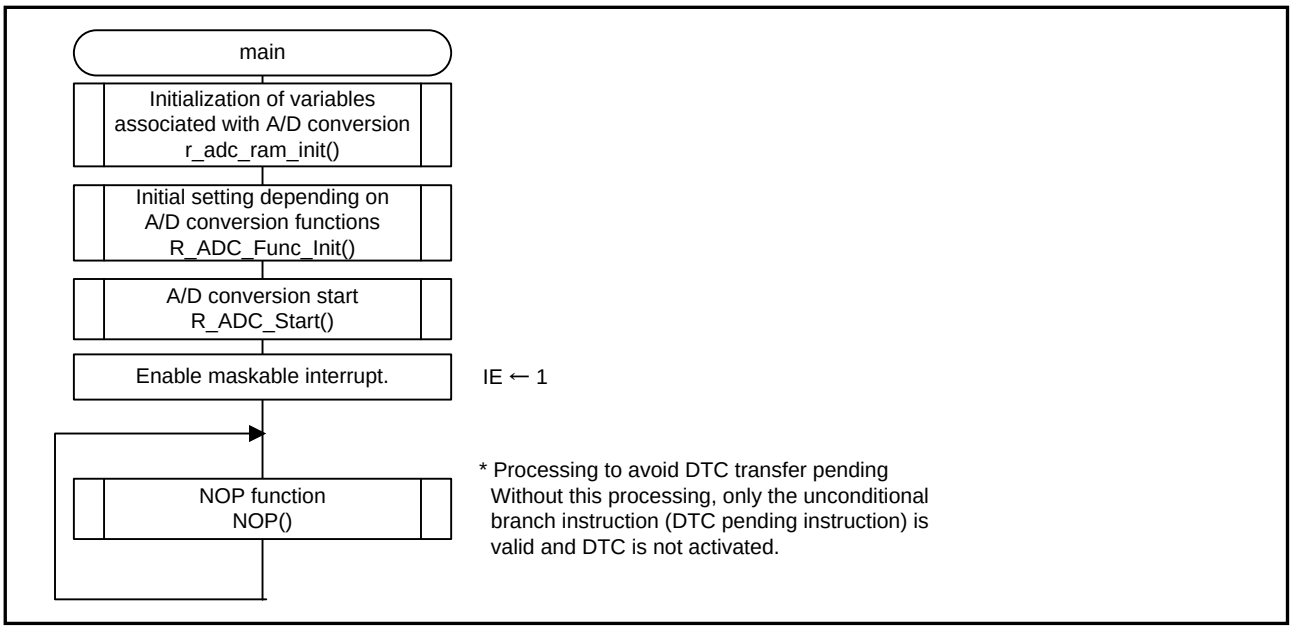


Figure 4.20 Main Processing

*DTC Pending Instruction

Even if a DTC transfer request is generated, DTC transfer is held immediately after the instructions below. Also, the DTC is not activated between PREFIX instruction code and the instruction immediately after that code.

- Call/return instruction
- Unconditional branch instruction
- Conditional branch instruction
- Read access instruction for code flash memory
- Bit manipulation instructions for IFxx, MKxx, PRxx, and PSW, and 8-bit manipulation instruction that has the ES register as operand
- Instruction for accessing the data flash memory

Notes:

1. When a DTC transfer request is acknowledged, all interrupt requests are held until DTC transfer is completed.
2. While the DTC is held pending by the DTC pending instruction, all interrupt requests are held.

(13) DTC Activation

Figure 4.21 is the DTC activation flowchart.

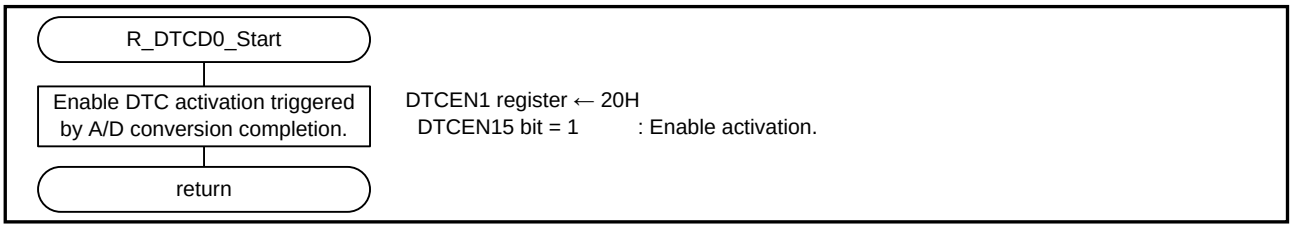


Figure 4.21 DTC Activation

(14) A/D Conversion Start

Figure 4.22 is a flowchart to start A/D conversion.

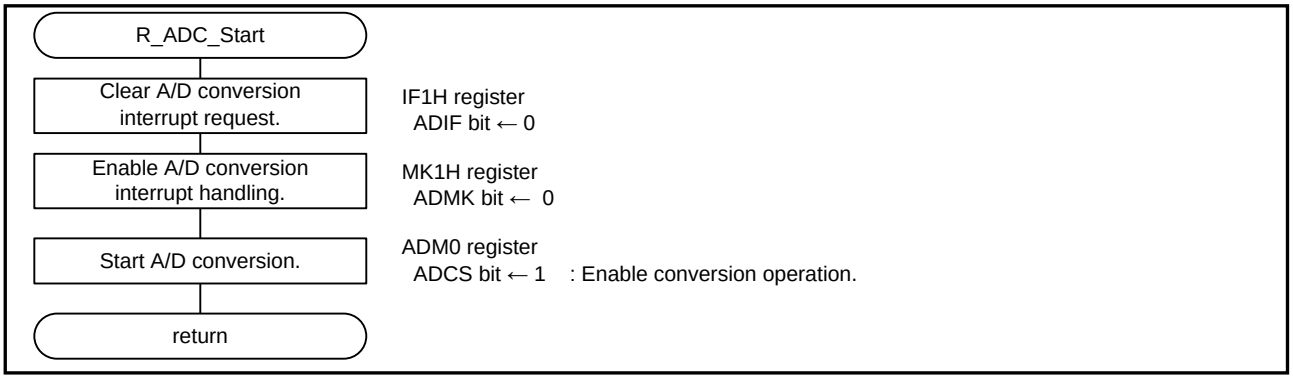


Figure 4.22 A/D Conversion Start

(15) A/D Conversion Interrupt

Figure 4.23 is a flowchart for A/D conversion interrupt.

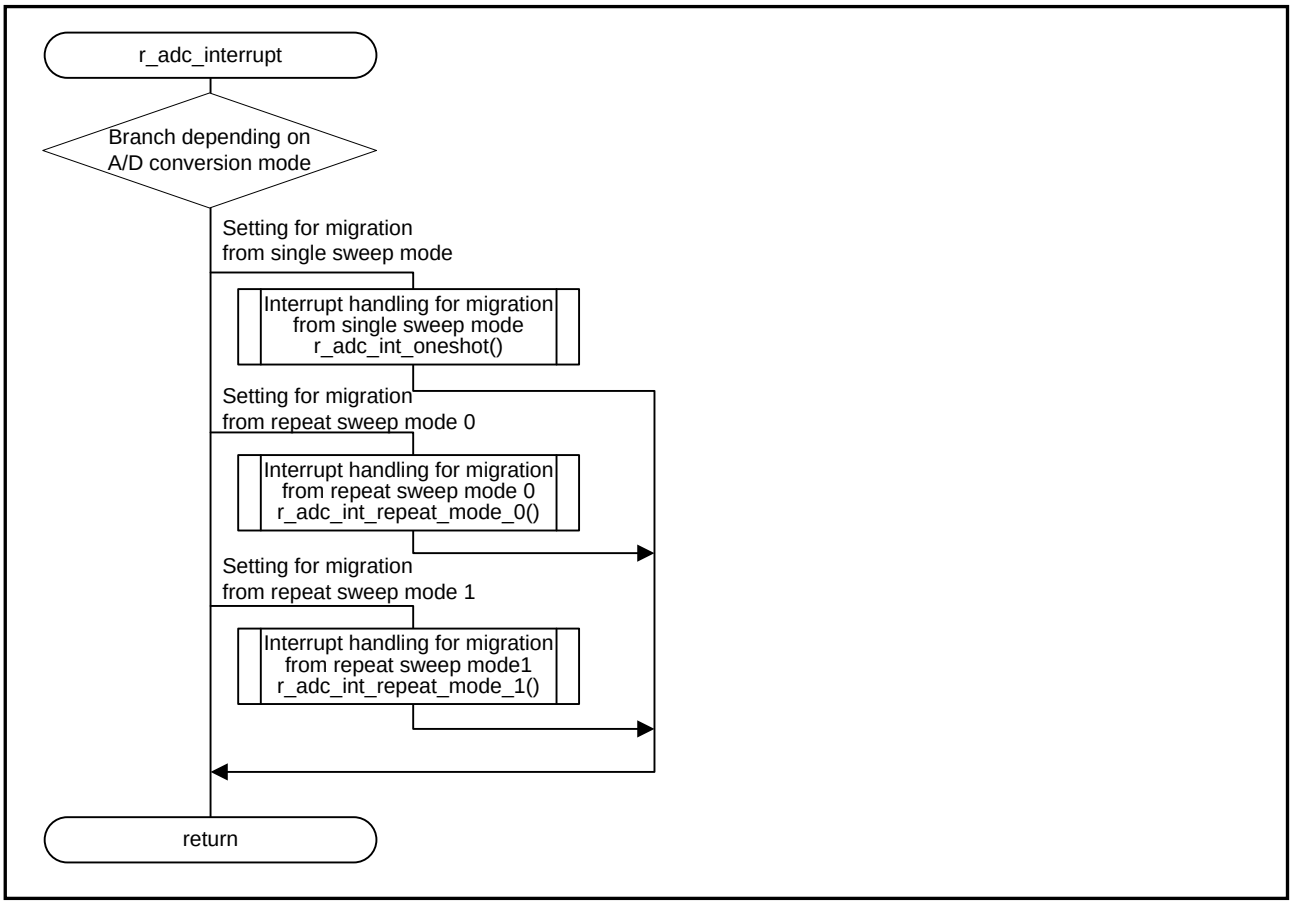


Figure 4.23 A/D Conversion Interrupt

(16) Interrupt Handling for Migration from the Single Sweep Mode

Figure 4.24 shows interrupt handling for migration from the single sweep mode.

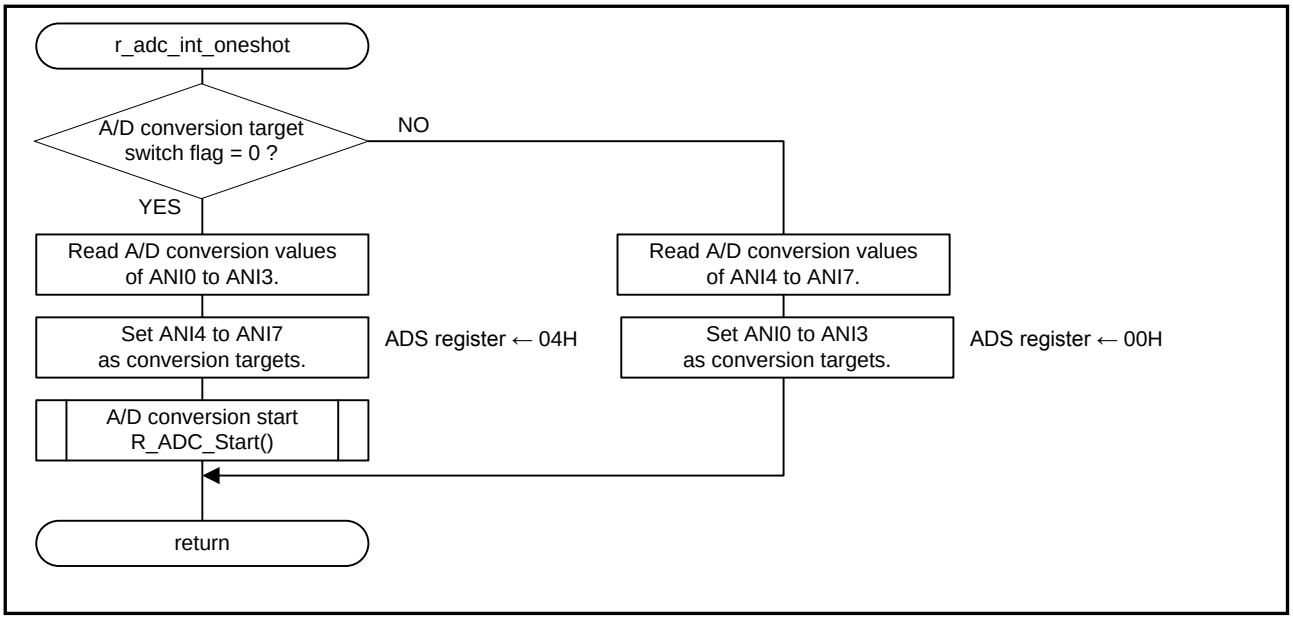


Figure 4.24 Interrupt Handling for Migration from the Single Sweep Mode

(17) Interrupt Handling for Migration from the Repeat Sweep Mode 0

Figure 4.25 shows interrupt handling for migration from the repeat sweep mode 0.

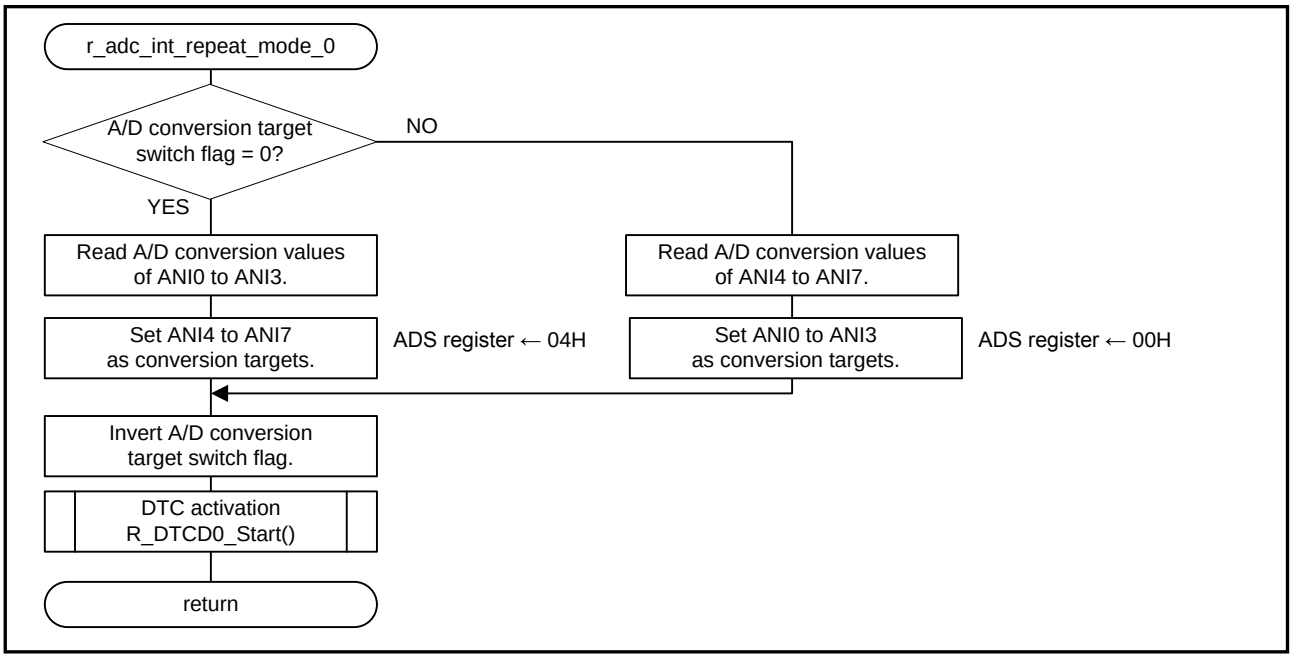


Figure 4.25 Interrupt Handling for Migration from the Repeat Sweep Mode 0

(18) Interrupt Handling for Migration from the Repeat Sweep Mode 1

Figure 4.26 shows interrupt handling for migration from the repeat sweep mode 1.

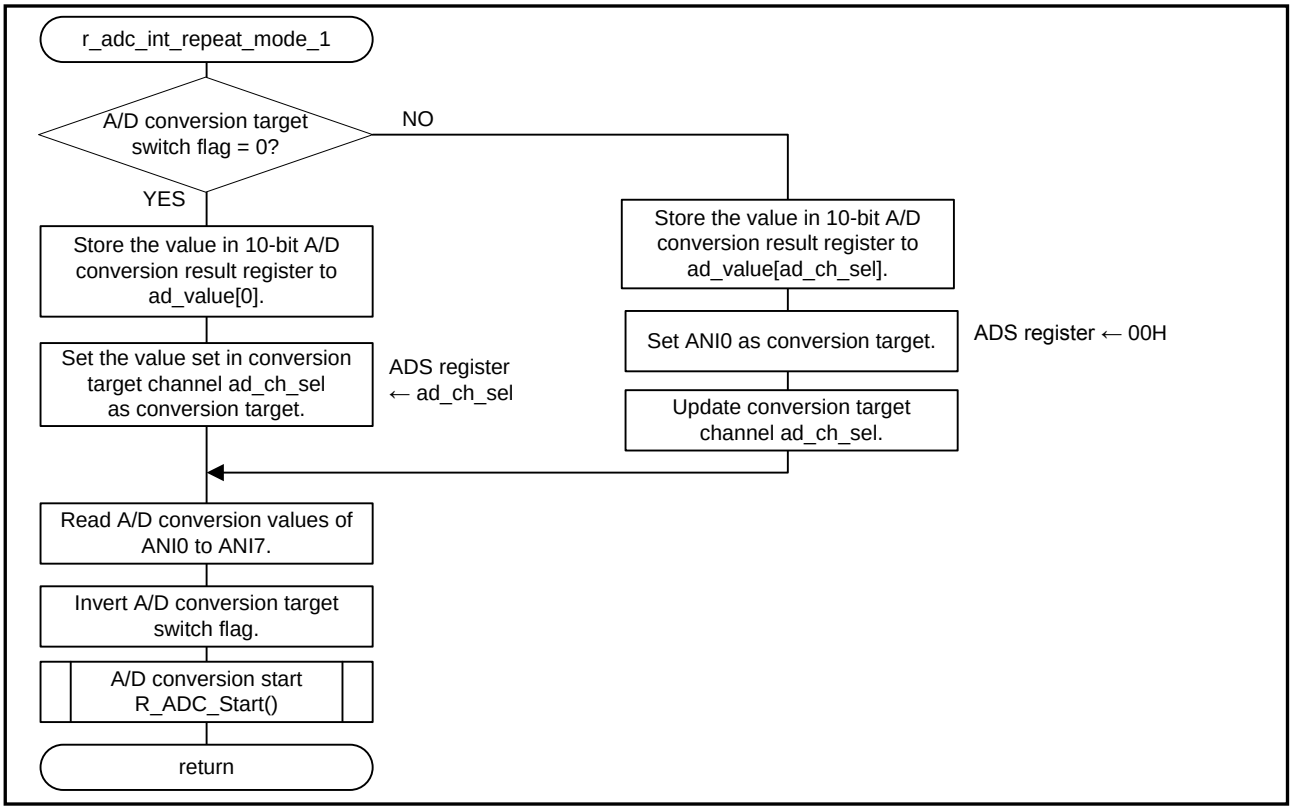


Figure 4.26 Interrupt Handling for Migration from the Repeat Sweep Mode 1

5. Reference Application Note

RL78/G14 Transferring A/D Conversion Result Using the DTC Rev.2.00

6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents

RL78/G14 User's Manual: Hardware Rev. 2.00
M16C/62P Group Hardware Manual Rev.2.41
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/contact/

REVISION HISTORY	RL78/G14, M16C/62P Group Application Note Migration Guide from M16C to RL78: A/D Converter

Rev.	Date of issue	Description	
		Page	Summary
1.00	Mar.6,2014	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

- 1. Handling of Unused Pins

  Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

  — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

- 2. Processing at Power-on

  The state of the product is undefined at the moment when power is supplied.

  — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
  In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

- 3. Prohibition of Access to Reserved Addresses

  Access to reserved addresses is prohibited.

  — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

- 4. Clock Signals

  After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

  — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

- 5. Differences between Products

  Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

  — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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