

RL78/G14

Haptic Feedback Control by a Piezoelectric Actuator CC-RL

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Introduction

This application note describes an example to drive piezoelectric haptic actuators. The timer array unit and D/A converter of the RL78/G14 are used in this application note.

Target Device

RL78/G14

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.



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1. Specifications

In this application note, a timer array unit (TAU), a D/A converter (DAC), and an amplifier are used to control a piezoelectric actuator of a type consisting of a piezoelectric element and a vibrating plate. A square wave generated by the timer array unit is amplitude-modulated by the D/A converter to generate a control waveform. Moreover, a voltage obtained by amplifying the control waveform using the amplifier is applied to the piezoelectric actuator.

Table 1.1 shows the required peripheral functions and their uses.

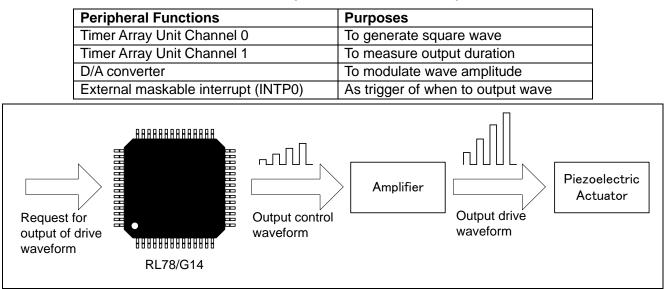


Table 1.1 Used Peripheral Functions and Purposes

Figure 1.1 Outline to drive piezoelectric actuator

1.1 Method of driving the piezoelectric actuator

When a voltage is applied to a piezoelectric element, the element is warped or deformed according to the applied voltage. Moreover, a piezoelectric element has a polarity; when the direction of application of the voltage is reversed, the element is deformed in the opposite direction.

This piezoelectric effect can be utilized to cause the piezoelectric element to vibrate, by repeatedly changing an electrical potential applied across to two electrodes in a short period of time.

In this application note, to obtain stronger haptic feedback, a square wave that has larger voltage change than other waveforms per unit time is used as the driving waveform. A timer array unit and a D/A converter are used to change the control waveform frequency and amplitude over time. Moreover, the control waveform is amplified up to a voltage at which the piezoelectric element can generate vibrations that can be felt by a human. In this application note, voltages up to a maximum ± 12 V are applied to the electrodes of the piezoelectric element, in accordance with the characteristics of the piezoelectric element used.



1.2 Method of generation of control waveform

The interval timer/square wave output function of the timer array unit is used. Using the square wave output, a waveform with a duty ratio of 50% is output. Moreover, the D/A converter is used to modulate the amplitude of the square wave.

In this application note, the tactile receptor characteristics of humans are considered. The control wave frequency can be varied in the range 1 to 1000 Hz. The control wave amplitude can be varied over 256 levels, which is the resolution of the 8-bit D/A converter. By changing the amplitude, the intensity of vibrations of the piezoelectric element can be adjusted.

1.3 Driving waveform frequencies and amplitude modulation patterns

As indicated in equations (1.1) to (1.6) and , Figure 1.2 as the driving waveform frequencies and the amplitude modulation patterns, patterns a to c were prepared. The parameters used are indicated in Table 1.2 below.

Table 1.2 parameters	used in calculation	of output frequence	v and amplitude
		or output nequent	y and amplitude

parameters	contents
f _{FROM}	Frequency of waveform at the start of output
f _{TO}	Frequency of waveform at the end of output
A _{FROM}	Amplitude of waveform at the start of output
A _{TO}	Amplitude of waveform at the end of output
t _{DRIVE}	Output duration of square wave

Pattern a: linear modulation

frequency(t) =
$$(\mathbf{f}_{TO} - \mathbf{f}_{FROM}) \frac{t}{t_{DRIVE}} + \mathbf{f}_{FROM}, \quad 0 \le t \le t_{DRIVE}$$
 (1.1)

amplitude(t) =
$$(A_{TO} - A_{FROM}) \frac{t}{t_{DRIVE}} + A_{FROM}, \quad 0 \le t \le t_{DRIVE}$$
 (1.2)

Pattern b: square modulation

frequency(t) =
$$(\mathbf{f}_{TO} - \mathbf{f}_{FROM}) \left(\frac{t}{t_{DRIVE}}\right)^2 + \mathbf{f}_{FROM}, \quad 0 \le t \le t_{DRIVE}$$
 (1.3)

amplitude(t) =
$$(A_{TO} - A_{FROM}) \left(\frac{t}{t_{DRIVE}}\right)^2 + A_{FROM}, \quad 0 \le t \le t_{DRIVE}$$
 (1.4)

Pattern c: square root modulation

frequency(t) =
$$(\mathbf{f}_{TO} - \mathbf{f}_{FROM}) \sqrt{\frac{t}{t_{DRIVE}}} + \mathbf{f}_{FROM}, \quad 0 \le t \le t_{DRIVE}$$
 (1.5)

amplitude(t) =
$$(A_{TO} - A_{FROM}) \sqrt{\frac{t}{t_{DRIVE}}} + A_{FROM}, \quad 0 \le t \le t_{DRIVE}$$
 (1.6)



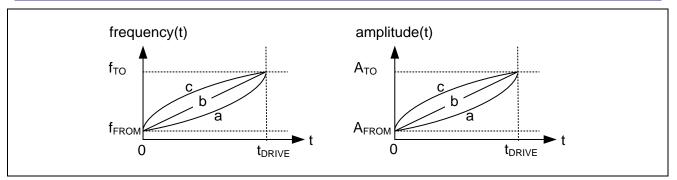


Figure 1.2 image of each modulation pattern

1.4 Method of calculation of device frequency and amplitude

In order to measure the time t in equations (1.1) to (1.6), channel 1 of the timer array unit 0 is used, and t

is set to

$$1 - \frac{TCR01}{TDR01}$$

t_{DRIVE}

to calculate the frequency and amplitude.

1.5 Examples of reproduction of tactile stimuli

Table 1.3 and Figure 1.3 indicate D/A converter output waveforms that reproduce pseudo-tactile stimuli when a button is pressed and is released.
Table 1.3 Setting parameters

parameters	press	release
fFROM	100 Hz	300 Hz
fTO	300 Hz	100 Hz
AFROM	0 V	VDD V
ATO	VDD V	0 V
tDRIVE	100 ms	125 ms
Modulation pattern	а	a

Press Release 100 ms 100 ms Press Release Release Release Release Release Release Release

Figure 1.3 Output waveform of tactile stimuli reproduction example.



2. Conditions of Operation Confirmation Test

The sample code with this application note runs properly under the conditions below.

Table 2.1 Operation	n Confirmation Conditio	ns
---------------------	-------------------------	----

Items	Contents
MCU	RL78/G14 (R5F104PJA)
Operating frequencies	High-speed on-chip oscillator clock: 32MHz
Operating voltage	5.0V
	LVD operations (VLVD): reset mode 2.81V (2.75V)
Integrated development environment (CS+)	CS+ for CC V7.00.00
C compiler (CS+)	CC-RL V1.07.00
Integrated development environment (e2 studio)	e2 studio V7.1.0
C compiler (e2 studio)	CC-RL V1.07.00

3. Hardware

3.1 Example of Hardware Configuration

Figure 3.1 shows an example of the hardware configuration used in this application note.

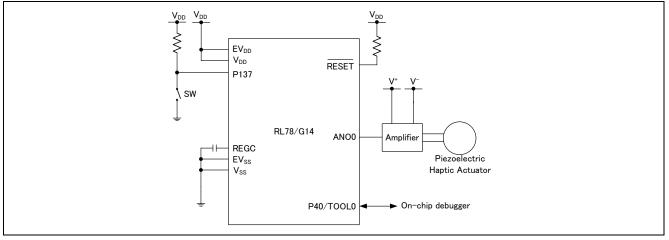


Figure 3.1 Hardware Configuration

Note: 1. This simplified circuit diagram was created to show an overview of connections only. When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements. (Connect each input-only port to V_{DD} or V_{SS} through a resistor.)

3.2 Used Pins

Table 3.1 shows list of used Pins and assigned functions.

Pin Name	Input/Output	Function
P137/INTP0	Input	Connected to switch
ANO0	Output	Output control waveform

Table 3.1 List of Pins and Functions



4. Software Explanation

4.1 Operation Outline

In the sample program with this application note, MCU shifts to STOP mode after initialization of Timer Array Unit, D/A Converter and External Maskable Interrupt.

MCU returns from STOP mode by external interrupt. And after outputting the control waveform to the piezoelectric element, shifts to STOP mode again.

The details are shown in ① to 9 below.

① Initialize the Timer Array Unit

<Conditions for setting channel 0>

- Timer operation mode is set to Interval Timer.
- Interval time is set to 10ms by the Timer data register (TDR).
- Timer output is disabled by the Timer output enable register (TOE).
- Interval time interrupt (INTTMOO) is enabled.

<Conditions for setting channel 1>

- Timer operation mode is set to Interval Timer.
- Interval time is set to 1000ms by the timer data register (TDR).
- Timer output is disabled by the Timer output enable register (TOE).
- Interval time interrupt (INTTMO1) is enabled.
- ② Initialize the External Maskable Interrupt

<Conditions for setting External Maskable Interrupt>

- Use P137/INTP0 pin.
- Select both rising and falling edges as valid edge.
- ③ Initialize the D/A Converter

 $<\!$ Conditions for setting D/A Converter>

- Set D/A converter operation mode to Normal mode
- Set D/A conversion value setting register to 0.
- ④ Enable the External maskable interrupt.
- (5) Enable maskable interrupts.
- ⑥ MCU is shifted to STOP mode.
- O MCU returns from STOP mode by external interrupt.
- (8) Judge whether the input signal is rising edge or falling edge, and output waveform pattern according to the result.
- (9) MCU is shifted to STOP mode after the output is done.

Steps $\ensuremath{\overline{\mathcal{O}}}$ to $\ensuremath{\overline{\mathcal{O}}}$ are repeated



4.2 Option Byte Settings

Table 4.1 lists the option byte settings.

Address	Setting Value	Contents	
000C0H/010C0H	1110 1111B	Operation of Watchdog timer is stopped (counting is stopped after reset.)	
000C1H/010C1H	0111 1111B	LVD operation (VLVD): reset mode Detection voltage: Rising edge = 2.81V, Falling edge = 2.75V	
000C2H/010C2H	1110 1000B	HS mode, High-speed on-chip oscillator clock: 32 MHz	
000C3H/010C3H	1000 0100B	On-chip debugging enabled	

Table 4.1 Option Byte Settings

4.3 Constants

Table 4.2 lists the constants that are used in this sample program.

Constant Name	Setting Value	Contents		
FREQ_TAU00	62500	Count clock frequency of TAU00		
FREQ_TAU01	62500	Count clock frequency of TAU01		
FREQ_OUTPUT_WAVE_MAX	1000	Max frequency of output square wave		
FREQ_OUTPUT_WAVE_MIN	1	Min frequency of output square wave		
TIME_OUTPUT_WAVE_MAX	1000	Max duration of output square wave		
TIME_OUTPUT_WAVE_MIN	1	Min duration of output square wave		
SW_ON	0	Port level when the switch is pressed		
SW_OFF	1	Port input level when the switch is released		

Table 4.2 Constants in the sample program



4.4 Global Variables

Table 4.3 lists the global variables.

Table 4.3 Global Variables

Туре	Variable Name	Contents	Functions used in
uint8_t	g_wave_output_enable	Whether a square wave is being output	r_main(), start_wave(), stop_wave(),
uint16_t	g_frequency_from	Frequency of waveform at the start of output	r_tau0_channel0_interrupt(), start_wave(),
uint16_t	g_frequency_to	Frequency of waveform at the end of output	r_tau0_channel0_interrupt(), start_wave(),
uint8_t	g_gain_from	Amplitude of waveform at the start of output	r_tau0_channel0_interrupt(), start_wave(),
uint8_t	g_gain_to	Amplitude of waveform at the end of output	r_tau0_channel0_interrupt(), start_wave(),
uint16_t	g_duration	Output duration	start_wave(),
uint8_t	g_transition_pattern		r_tau0_channel0_interrupt(), start_wave(),
uint8_t	g_wave_toggle	control variable for outputting square wave	r_tau0_channel0_interrupt(), start_wave(),

4.5 Functions

Table 4.4 lists the functions.

Function Name	Outline	
main	Main processing	
R_MAIN_UserInit	Main initial setting	
set_frequency	Set frequency of output waveform.	
set_duration	Set duration output waveform	
start_wave	Start output of square wave	
stop_wave	Stop output of square wave	
r_tau0_channel0_interrupt	Interrupt handler of TAU00	
r_tau0_channel1_interrupt	Interrupt handler of TAU01	
r_intc0_interrupt	Interrupt handler of INTC0	



4.6 Function Specifications

This part describes function specifications of the sample code.

[Function Name]	r_main
Outline	Main processing
Header	_
Declaration	_
Description	After calling R_MAIN_UserInit(), shift to STOP mode.
Arguments	None
Return value	None
Remarks	None
[Function Name]	R_MAIN_UserInit
Outline	Main initial setting
Header	_
Declaration	static void R_MAIN_UserInit(void);
Description	Enable interrupt processing by the EI instruction.
	Next, set initial value to the D/A conversion value setting register (DACS) and enabled/A conversion operation.
Arguments	None
Return value	None
Remarks	None



[Function Name]	sot froquency					
Outline	set_frequency	nov of output waveform				
Header	Function to set frequency of output waveform. r_cg_timer.h					
Declaration	- u -					
	void set_frequency(uint16_t frequency);					
Description	Set TDR00 register the value to the frequency designated by argument.					
Arguments	frequency	Output frequency (1 ~ 1000 [Hz])				
Return value	None					
Remarks	None					
[Function Name]	set_duration					
Outline	Function to set duration	on output waveform				
Header	r_cg_timer.h					
Declaration	void set_duration(uint	16_t duration);				
Description		e value to the duration designated by argument.				
Arguments	duration	Output duration (1 ~ 1000 [ms])				
Return value	None					
Remarks	None					
Remarks	None					
[Function Name]	start_wave					
Outline	Function to start output	utting square wave				
Header	r_cg_timer.h					
Declaration	void start_wave(uint16_t frequency_from, uint16_t frequency_to, uint16_t					
	gain_from, uint16_t ga	ain_to, uint16_t inteval, uint16_t transition_pattern);				
Description	start output square wa	ave with designated frequency, amplitude, and duration by				
	arguments.					
Arguments	frequency_from	Frequency of waveform at the start of output (1-1000				
	fra avera avera	[Hz])				
	frequcney_to	Frequency of waveform at the end of output (1 - 1000[Hz])				
	gain_from	Amplitude of waveform at the start of output (0-255)				
	gain_to	Amplitude of waveform at the end of output (0-255)				
	duration	Output duration (1 ~ 1000 [ms])				
	transition_pattern	Modulation pattern (LINEAR, SQUARE,				
		SQUARE_ROOT)				
Return value	None					
Remarks	None					
[Function Name]	stop_wave					
Outline	Function to stop output	It of square wave				

[i anonon namo]	
Outline	Function to stop output of square wave
Header	r_cg_timer.h
Declaration	void stop_wave(void);
Description	Stop output of square wave
Arguments	None
Return value	None
Remarks	None



[Function Name]	r_tau0_channel0_interrupt
Outline	Interrupt handler of TAU00
Header	None
Declaration	static voidnear r_tau0_channel0_interrupt(void);
Description	Interrupt handler of TAU00
Arguments	None
Return value	None
Remarks	None
[Function Name]	r_tau0_channel1_interrupt
Outline	Interrupt handler of TAU01
Header	None
Declaration	static voidnear r_tau0_channel1_interrupt(void);
Description	Interrupt handler of TAU01
Arguments	None
Return value	None
Remarks	None
[Function Name]	r_intc0_interrupt
Outline	Interrupt handler of INTC0
Header	None
Declaration	static voidnear r_intc0_interrupt(void);
Description	Interrupt handler of INTC0
Arguments	None
Return value	None

Return value Remarks None



4.7 Flowcharts

Figure 4.1 shows an overall flow of the sample code.

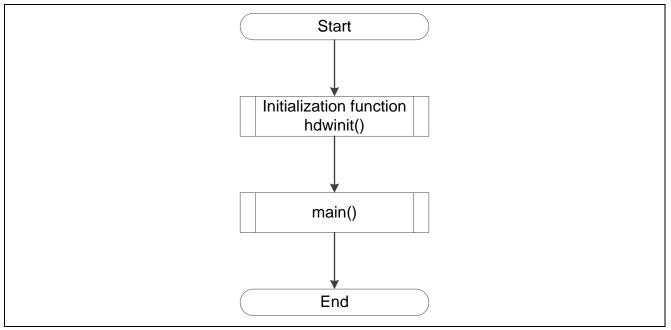


Figure 4.1 Overall Flow

4.7.1 Initialization Function

Figure 4.2 shows the flowchart of the initialization function.

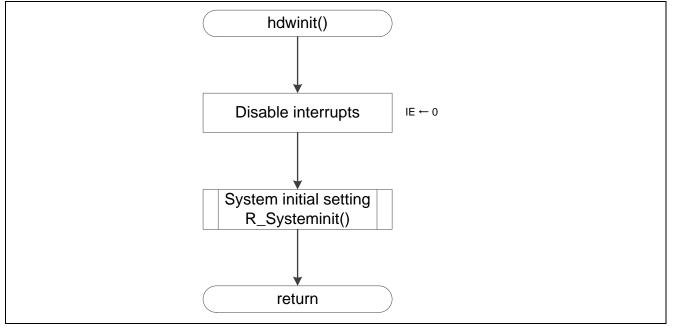


Figure 4.2 Initialization Function



4.7.2 System Initial Setting

Figure 4.3 shows the flowchart of the system initial setting.

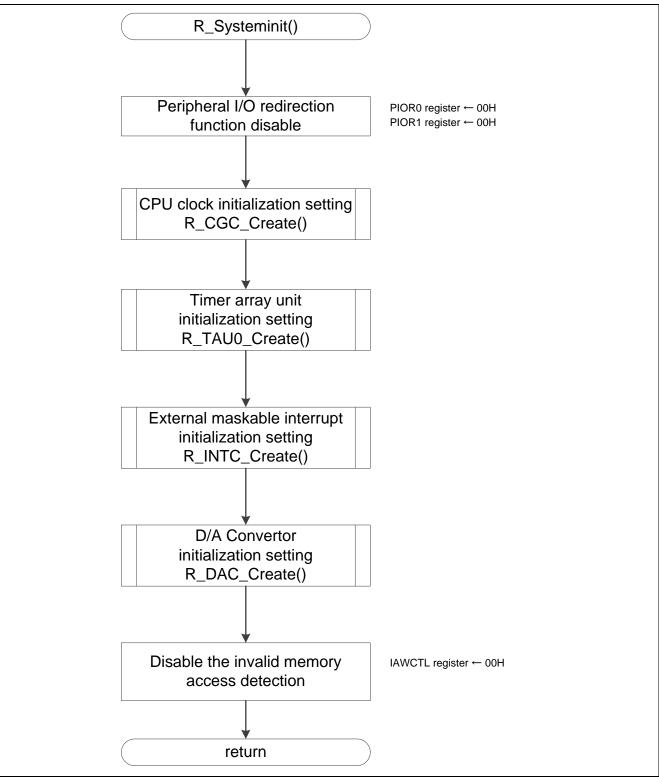


Figure 4.3 System initial setting



4.7.3 CPU Initial Setting

Figure 4.2 shows the flowchart of the CPU initial setting.

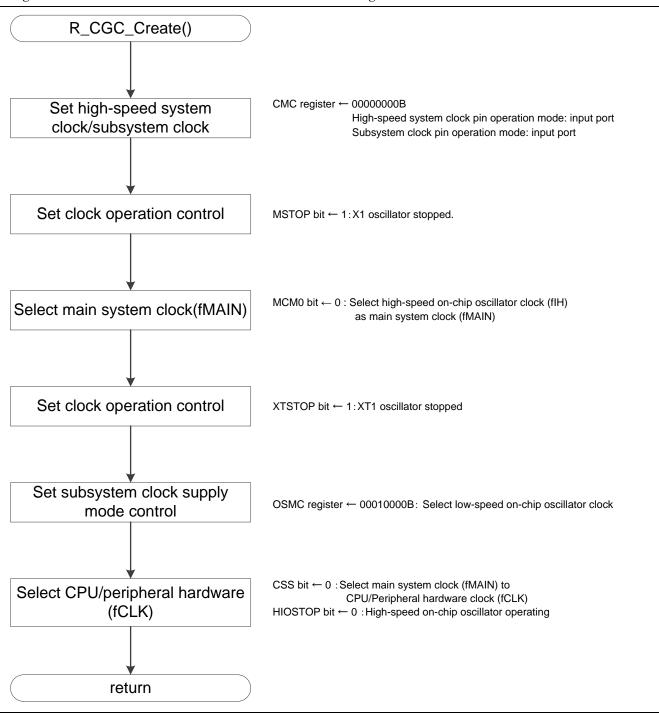


Figure 4.4 CPU Initial Setting



Clock operation mode setting

Clock operation mode control register (CMC)
 High-speed system clock pin operation mode: input port mode
 Subsystem clock pin operation mode: input port mode

Symbol: CMC

7	6	5	4	3	2	1	0
EXCLK	OSCSEL	EXCLKS	OSCSELS	0	AMPHS1	AMPHS0	AMPH
0	0	0	0	0	0	0	0

Bits 7-6

EXCLK	OSCSEL	High-seed oscillation clock pin operation mode	X1/P121 Port	X2/EXCLK/P122 Port	
0	0	Input port mode	Input port		
0	1	X1 oscillation mode	Crystal/ceramic resonator connection		
1	0	Input port mode	Input port		
1	1	External clock input mode	Input port	External clock input	

Bits 5-4

EXCLKS	OSCSELS	Subsystem clock pin operation mode	n operation XT1/P123 Pin XT2/EXCLKS/P		
0	0	Input port mode	Input port		
0	1	XT1 oscillation mode	Crystal resonator connection		
1	0	Input port mode	Input port		
1	1	External clock input mode	Input port	External clock input	

Bits 2-1

AMPHS1	AMPHS0	T1 oscillator oscillation mode selection			
0	0	Low-power consumption oscillation (default)			
0	1	Normal oscillation			
1	0	Ultra-low power consumption oscillation			
1	1	Setting prohibited			

Bit 0

AMPH	Control of X1 clock oscillation frequency			
0	$MHz \le f_X \le 10MHz$			
1	$10MHz < f_X \le 20MHz$			



Operation control of clocks

Clock operation status control register (CSC)
 High-speed system clock operation control: X1 oscillator stopped
 Subsystem clock operation control: XT1 oscillator stopped
 High-speed on-chip oscillator clock operation control: High-speed on-chip oscillator

Symbol: CSC

7	6	5	4	3	2	1	0
MSTOP	XTSTOP	0	0	0	0	0	HIOSTOP
1	1	0	0	0	0	0	0

Bit 7

METOD	High-speed system clock operation control					
MSTOP	X1 oscillation mode	External clock input mode	Input port mode			
0	X1 oscillator operating	External clock from EXCLK pin is valid	loovet a out			
1	X1 oscillator stopped External clock from EXCLK pin is invalid Input port		input port			

Bit 6

VICTOR	Subsystem clock oper	Subsystem clock operation control										
XTSTOP	XT1 oscillation mode	External clock input mode	Input port mode									
0	XT1 oscillator operating	External clock from EXCLKS pin is valid										
1	XT1 oscillator stopped	External clock from EXCLKS pin is invalid	Input port									

Bit 0

HIOSTOP	P High-speed on-chip oscillator clock operation control							
0	High-speed on-chip oscillator operating							
1	High-speed on-chip oscillator stopped							



System clock control setting

- System clock control register (CKC)

Select the high-speed on-chip oscillator clock as a CPU/peripheral hardware clock.

Symbol: CKC

7	6	5	4	3	2	1	0
CLS	CSS	MCS	MCM0	0	0	0	0
0	0	0	0	0	0	0	0

Bit 6

CSS Selection of CPU/peripheral hardware clock (fclk)						
0	Main system clock (f _{MAIN})					
1	Subsystem clock (f _{SUB})					

Bit 4

MCM0 Main system clock (f _{MAIN}) operation control						
0 Selects the high-speed on-chip oscillator clock (f _{IH}) as the main system clock (f _{MAIN})						
1	Selects the high-speed system clock (f_{MX}) as the main system clock (f_{MAIN})					



4.7.4 Timer Array Unit Initial Setting

Figure 4.5 and Figure 4.6 shows the flowchart for the timer array unit initial setting.

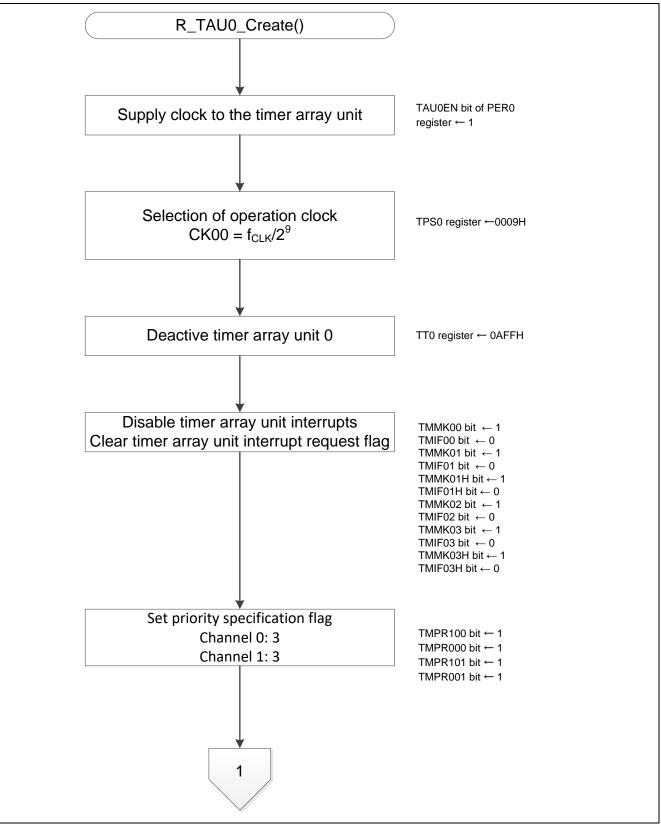


Figure 4.5 CPU Initial Setting

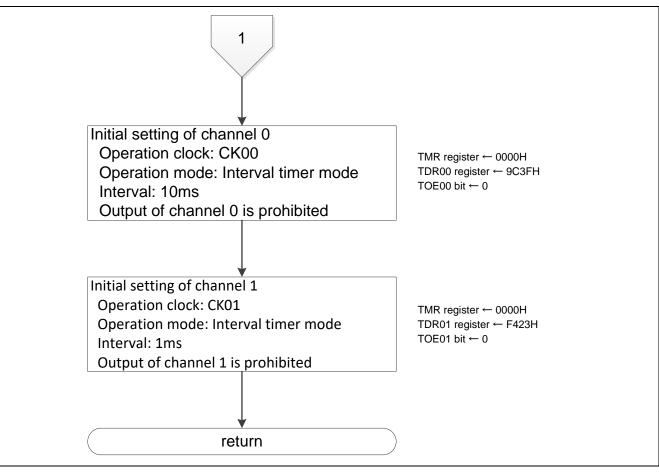


Figure 4.6 CPU Initial Setting



4.7.5 CPU Initial Setting

Figure 4.2 shows the flowchart of the CPU initial setting.

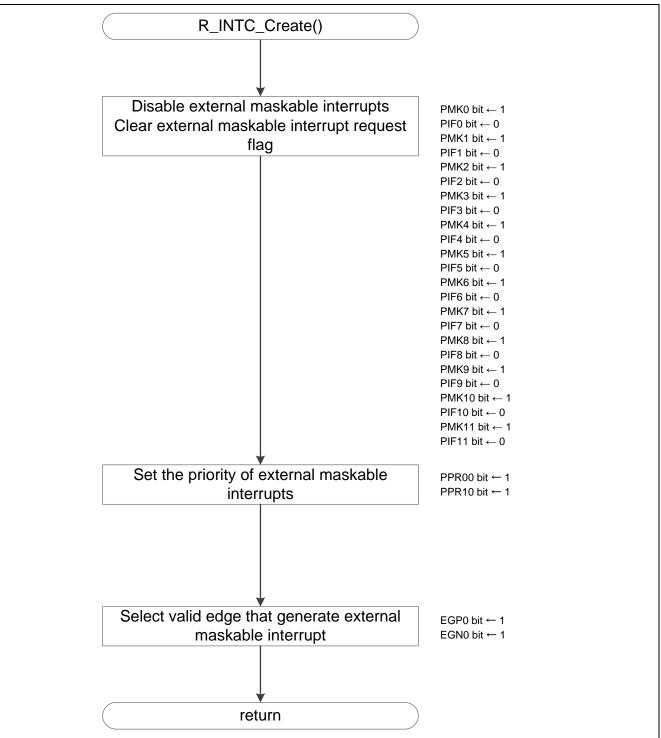


Figure 4.7 CPU Initial Setting



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Clock supply to timer array unit started

Peripheral enable register 0 (PER0)

Clock supply to timer array unit

Symbol: PER0

7	6	5	4	3	2	1	0
RTCEN	IICA1EN	ADCEN	IICA0EN	SAU1EN	SAU0EN	TAU1EN	TAU0EN
Х	Х	Х	Х	Х	Х	Х	1

Bit 0

TAU0EN	Control of timer array 0 unit input clock
0	Stops supply of input clock.
1	Supplies input clock.

Operation clock setting

- Timer clock select register 0 (TPS0)

Selection of operation clock (CK00)

Symbol: TPS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	PRS	PRS	0	0	PRS									
0	0	031	030	0	0	021	020	013	012	011	010	003	002	001	000
0	0	0	0	0	0	0	0	1	1	0	1	1	0	0	1

PRS	PRS	PRS	PRS	Operatio	n Clock (CK0	0) Selection			
003	002	001	000		f _{с∟к} = 2MHz	f _{с∟к} = 5MHz	f _{с∟к} = 10MHz	f _{clк} = 20MHz	f _{cLK} = 32MHz
0	0	0	0	f _{CLK}	2MHz	5MHz	10MHz	20MHz	32 MHz
0	0	0	1	f _{CLK} /2	1MHz	2.5MHz	5MHz	10MHz	16 MHz
0	0	1	0	$f_{CLK}/2^2$	500kHz	1.25MHz	2.5MHz	5MHz	8 MHz
0	0	1	1	f _{CLK} /2 ³	250kHz	625kHz	1.25MHz	2.5MHz	4 MHz
0	1	0	0	f _{CLK} /2 ⁴	125kHz	312.5kHz	625kHz	1.25MHz	2 MHz
0	1	0	1	$f_{CLK}/2^5$	62.5kHz	156.2kHz	312.5KHz	625KHz	1 MHz
0	1	1	0	f _{CLK} /2 ⁶	31.25kHz	78.1kHz	156.2kHz	312.5kHz	500 kHz
0	1	1	1	$f_{CLK}/2^7$	15.62kHz	39.1kHz	78.1kHz	156.2kHz	250 kHz
1	0	0	0	f _{CLK} /2 ⁸	7.81kHz	19.5kHz	39.1kHz	78.1kHz	125 kHz
1	0	0	1	f _{ськ} /2 ⁹	3.91kHz	9.76kHz	19.5kHz	39.1kHz	62.5 kHz
1	0	1	0	f _{CLK} /2 ¹⁰	1.95kHz	4.88kHz	9.76kHz	19.5kHz	31.25 kHz
1	0	1	1	f _{CLK} /2 ¹¹	976Hz	2.44kHz	4.88kHz	9.76kHz	15.6 kHz
1	1	0	0	f _{CLK} /2 ¹²	488Hz	1.22kHz	2.44kHz	4.88kHz	7.81 kHz
1	1	0	1	f _{CLK} /2 ¹³	244Hz	610Hz	1.22kHz	2.44kHz	3.91 kHz
1	1	1	0	f _{CLK} /2 ¹⁴	122Hz	305Hz	610Hz	1.22kHz	1.95 kHz
1	1	1	1	f _{CLK} /2 ¹⁵	61Hz	153Hz	305Hz	610Hz	977 Hz



Channel stop control

Stop the counting operation of each channel

Symbol: TT0

,															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TT	0	TT	0	TT							
				H03		H01		07	06	05	04	03	02	01	00
0	0	0	0	1	0	1	0	1	1	1	1	1	1	1	1

Bit 3

TT03	Operation stop trigger of channel 3
0	TE03 bit is cleared to 0 and the count operation is stopped.
1	Operation is stopped (stop trigger is generated).

Bit 2

TT02	Operation stop trigger of channel 2
0	TE02 bit is cleared to 0 and the count operation is stopped.
1	Operation is stopped (stop trigger is generated).

Bit 1

TT01	Operation stop trigger of channel 1
0	TE01 bit is cleared to 0 and the count operation is stopped.
1	Operation is stopped (stop trigger is generated).

Bit 0

TT00	Operation stop trigger of channel 0
0	TE00 bit is cleared to 0 and the count operation is stopped.
1	Operation is stopped (stop trigger is generated).



⁻ Timer channel stop register 0 (TT0)

Timer array unit 0 channel 0 initialization

- Timer mode register 00 (TMR00)
 - Selection of operation mode, Selection of start trigger, Selection of operation clock

Symbol: 1	MR00
-----------	------

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS	CKS	0	CCS	0	STS	STS	STS	CIS	CIS	0	0	MD	MD	MD	MD
001	000		00		002	001	000	001	000			003	002	001	000
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15-14

CKS001	KS001 CKS000 Selection of operation clock (f _{MCK}) for channel 0						
0	0	Operation clock CKm0 set in timer clock selection register m (TPSm)					
0	1	Operation clock CKm2 set in timer clock selection register m (TPSm)					
1	0	Operation clock CKm1 set in timer clock selection register m (TPSm)					
1	1	Operation clock CKm3 set in timer clock selection register m (TPSm)					

Bit 12

CCS00	Selection of channel 0 operation clock (f _{TCLK})
0	Operation clock (f _{MCK}) set in bits CKS000 and CKS001
1	Valid edge of input signal from TI00 pin

Bits 10-8

STS 002	STS 001	STS 000	Setting start or capture trigger of channel 0									
0	0	0	Only software trigger start is valid (other trigger sources are unselected)									
0	0	1	Valid edge of TI00 pin input is used as both the start trigger and capture trigger									
0	1	0	Both edges of TI00 pin input are used as the start trigger and capture trigger									
1	0	0	Interrupt signal of master channel is used (when using slave channel with simultaneous channel operation function)									
Oth	er than a	above	Setting prohibited									



Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS	CKS	0	CCS	0	STS	STS	STS	CIS	CIS	0	0	MD	MD	MD	MD
001	000		00		002	001	000	001	000			003	002	001	000
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 7-6

CIS CIS 001 000		Selection of TI00 pin input valid edge	
0	0	Falling edge	
0	1	Rising edge	
1	0	Both edges (when low-level width is measured)	
1	1	Both edges (when high-level width is measured)	

Bits 3-0

MD 003	MD 002	MD 001	MD 000	Operation mode of channel 0
0	0	0	0	Interval timer mode (Timer interrupt is not generated when counting is started).
U	Ŭ	Ŭ	1	Interval timer mode (Timer interrupt is generated when counting is started).
0	1	0	0	Capture mode (Timer interrupt is not generated when counting is started).
0	1	0	1	Capture mode (Timer interrupt is generated when counting is started).
0	1	1	0	Event counter mode (Timer interrupt is not generated when counting is started).
			0	One-count mode (Start trigger is invalid during counting operation).
1	0	0	1	One-count mode (Start trigger is valid during counting operation).
1	1	0	0	Capture & one-count mode (Timer interrupt is not generated when counting is started Start trigger is invalid during counting operation).
(Other th	ian abov	/e	Setting prohibited



Timer array unit 0 channel 1 initialization

- Timer mode register 01 (TMR01)

Selection of operation mode, Selection of start trigger, Selection of operation clock

Symbol: TMR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS	CKS	0	CCS	SPLIT	STS	STS	STS	CIS	CIS	0	0	MD	MD	MD	MD
011	010		01	01	012	011	010	011	010			013	012	011	010
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15-14

CKS011	CKS010	Selection of operation clock (f_{MCK}) for channel 1							
0	0	Operation clock CKm0 set in timer clock selection register m (TPSm)							
0	1	Operation clock CKm2 set in timer clock selection register m (TPSm)							
1	0	Operation clock CKm1 set in timer clock selection register m (TPSm)							
1	1	Operation clock CKm3 set in timer clock selection register m (TPSm)							

Bit 12

CCS01	Selection of channel 1 operation clock (f _{TCLK})
0	Operation clock (f _{MCK}) set in bits CKS010 and CKS011
1	Valid edge of input signal from TI01 pin

Bit 11

SPLIT01	Selection of 8 or 16-bit timer operation for channel 1
0	Operates as 16-bit timer.
1	Operates as 8-bit timer.

Bits 10-8

STS 012	STS 011	STS 010	Setting start or capture trigger of channel 1
0	0	0	Only software trigger start is valid (other trigger sources are unselected)
0	0	1	Valid edge of TI00 pin input is used as both the start trigger and capture trigger
0	1	0	Both edges of TI00 pin input are used as the start trigger and capture trigger
1	0	0	Interrupt signal of master channel is used (when using slave channel with simultaneous channel operation function)
Ot	her than	above	Setting prohibited



Symbol: TMR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS	CKS	0	CCS	SPLIT	STS	STS	STS	CIS	CIS	0	0	MD	MD	MD	MD
011	010		01	01	012	011	010	011	010			013	012	011	010
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 7-6

CIS 011	CIS 010	Selection of TI01 pin input valid edge
0	0	Falling edge
0	1	Rising edge
1	0	Both edges (when low-level width is measured)
1	1	Both edges (when high-level width is measured)

Bit 3-0

MD 013	MD 012	MD 011	MD 010	Operation mode of channel 1
0	0	0	0	Interval timer mode (Timer interrupt is not generated when counting is started).
U	U	U	1	Interval timer mode (Timer interrupt is generated when counting is started).
0	1	0	0	Capture mode (Timer interrupt is not generated when counting is started).
0	1	0	1	Capture mode (Timer interrupt is generated when counting is started).
0	1	1	0	Event counter mode (Timer interrupt is not generated when counting is started).
4	0	0	0	One-count mode (Start trigger is invalid during counting operation).
1	0	0	1	One-count mode (Start trigger is valid during counting operation).
1	1	0	0	Capture & one-count mode (Timer interrupt is not generated when counting is started Start trigger is invalid during counting operation).
(Other th	an abov	/e	Setting prohibited



Timer counter control

- Timer data register 00 (TMR00)

Set the compare value to "0270H" which can measure 10 milliseconds.

Symbol : TDR00

15						-	-	-	-	-	-	-	_	-	-
0	0	0	0	0	0	1	0	0	1	1	1	0	0	0	0

- Timer data register 00 (TMR00)

Set the compare value to "F423H" which can measure 1000 milliseconds.

Symbol : TDR01

	14					-	-	-	-	-	-	-	_	-	-
1	1	1	1	0	1	0	0	0	0	1	0	0	0	1	1

Configuring the output value for the timer output pin

- Timer output register 0 (TO0)

Configure the output value for the timer output pin for each channel.

Symbol: TO0

_	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0	TO07	TO06	TO05	TO04	TO03	TO02	TO01	TO00
	0	0	0	0	0	0	0	0	х	х	х	х	х	х	0	0

x: bits that do not change

Bits 1-0

TO0n	Channel n timer output
0	Timer output value is 0
1	Timer output value is 1

Note: Refer to the RL78/G14 user's manual (hardware) for details on individual registers.



Enabling the timer output

Timer output enable register 0 (TOE0)

Enable/disable the timer output for each channel.

Symbol: TOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	TOE							
0	0	0	0	0	0	0	0	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	х	х	х	х	х	х	0	0

x: bits that do not change

Bits 1-0

TOE0n	Timer output enable/disable of channel n
0	The TO0n operation stopped by count operation (timer channel output bit). Writing to the TO0n bit is enabled.
U	The TO0n pin functions as data output, and it outputs the level set to the TO0n bit. The output level of the TO0n pin can be manipulated be software.
	The TO0n operation enabled by count operation (timer channel output bit).
	Writing to the TO0n bit is disabled (writing is ignored).
1	The TO0n pin functions as timer output, and the TOE0n bit is set or reset depending on the
	timer operation.
	The TO0n pin outputs the square-wave or PWM depending on the timer operation.



4.7.6 External maskable interrupt Initial Setting

Figure 4.3 shows the flowchart of the external maskable interrupt initial setting.

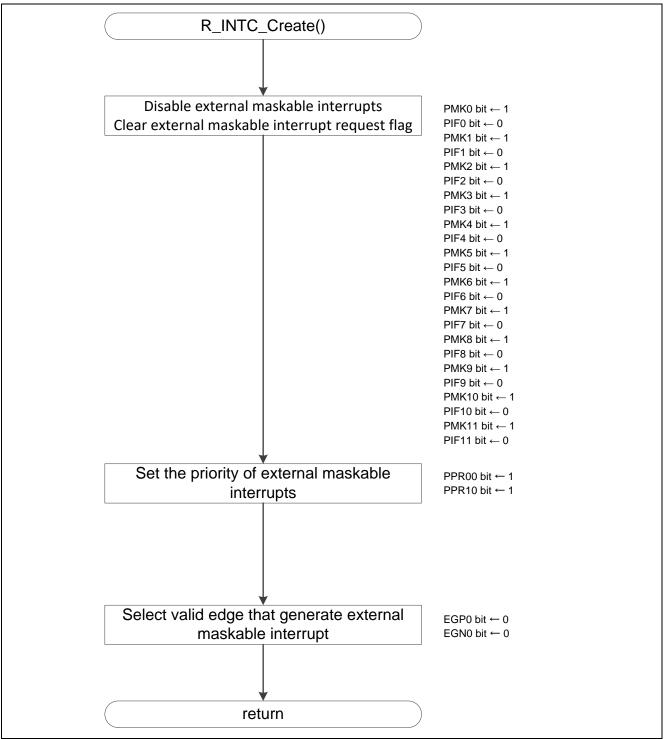


Figure 4.8 External maskable interrupt initial setting



-

Set edge detection of INTP0 pin

External interrupt rising edge enable register 0 (EGP0) Set valid edge of INTP0 pin.

Symbol: EGP0

7	6	5	4	3	2	1	0
EGP7	EGP6	EGP5	EGP4	EGP3	EGP2	EGP1	EGP0
0	0	0	0	0	0	0	1

Symbol: EGN0

7	6	5	4	3	2	1	0
EGN7	EGN6	EGN5	EGN4	EGN3	EGN2	EGN1	EGN0
0	0	0	0	0	0	0	1

Bit 0

EGP0	EGN0	INTP0 pin valid edge selection
0	0	Edge detection disabled
0	1	Falling edge
1	0	Rising edge
1	1	Both rising and falling edges



4.7.7 D/A Converter initial setting

Figure 4.3 shows the flowchart of the D/A Converter initial setting.

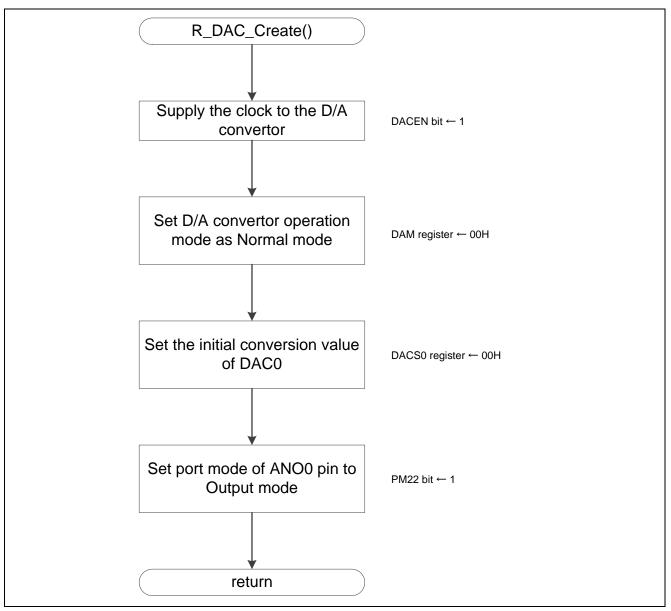


Figure 4.9 D/A converter initial setting



_

-

- Enable providing a clock to the D/A converter.
- Peripheral Enable Register 1 (PER1)

Symbol : PER1

7	6	5	4	3	2	1	0
DACEN	TRGEN	CMPEN	TRD0EN	DTCEN	0	0	TRJ0EN
1	х	х	х	х	Х	Х	x

x: bits that do not change

Bit 7

DACEN	Control of D/A converter input clock					
0	Stops input clock supply.					
1	Supplies input clock.					

Set the D/A converter to normal mode.

D/A Converter Mode Register (DAM)

Symbol: DAM

7	6	5	4	3	2	1	0
0	0	DACE1	DACE0	0	0	DAMD1	DAMD0
0	0	0	0	0	0	0	0

Bit 0

DAMD0	D/A converter operation mode selection				
0	Normal mode				
1	Real-time output mode				

Initialize the DAC0 conversion value.

- D/A Conversion Value Setting Register 0 (DACS0) Set 000H to the D/A conversion value.

Symbol: DACS0

7	6	5	4	3	2	1	0
DACS07	DACS06	DACS05	DACS04	DACS03	DACS02	DACS01	DACS00
0	0	0	0	0	0	0	0

	Function
Bits	The relation between the resolution and analog output voltage (VANO0) of the D/A converter are as follows.
7 to 0	VANO0 = Reference voltage for D/A converter × (DACS0) / 256

Note: Refer to the RL78/G14 user's manual (hardware) for details on individual registers.



Set the ANO0 pin function

- Port Mode Register 2 (PM2)

Symbol: PM2

7	6	5	4	3	2	1	0
PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20
х	x	х	х	х	1	х	х

x: bits that do not change

Bit 2

$DIU \Delta$	
PM22	P22 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Note: Refer to the RL78/G14 user's manual (hardware) for details on individual registers.



4.7.8 Main Processing

Figure 4.10 shows the flowchart of the main processing.

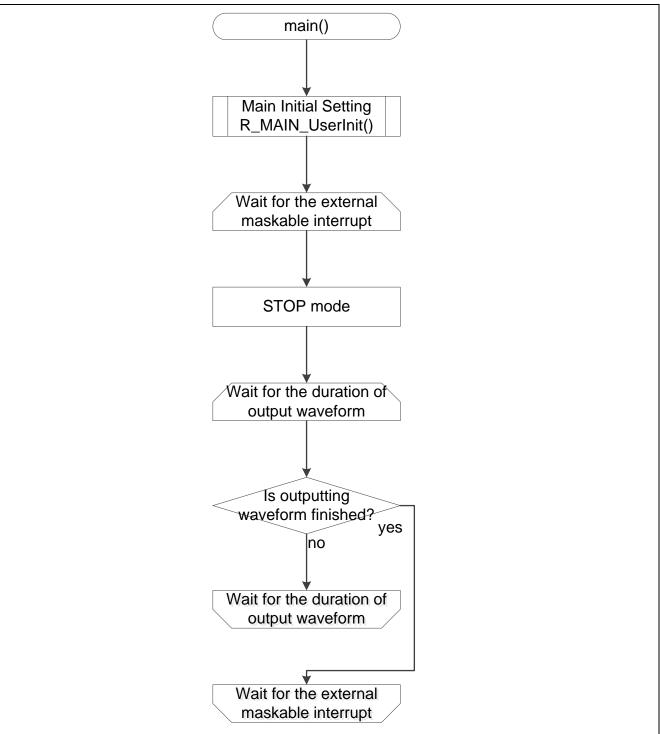


Figure 4.10 Main processing



4.7.9 Main Initial Setting

Figure 4.11 shows the flowchart of the main initial setting.

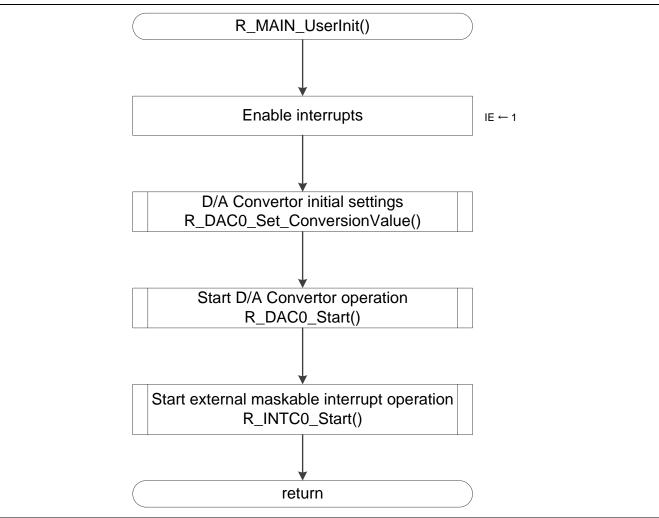


Figure 4.11 Main initial setting



4.7.10 External Maskable Interrupt Operation Start Function

Figure 4.12 shows the flowchart of the external maskable operation start function.

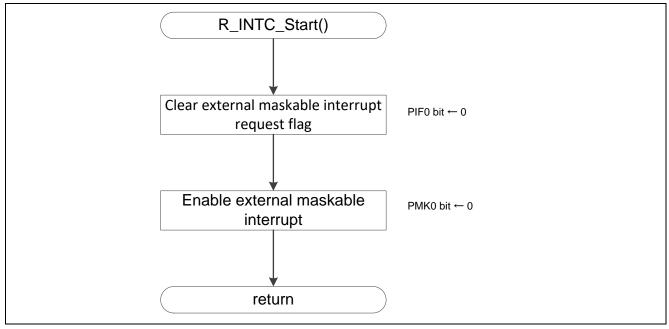


Figure 4.12 external maskable operation start function

4.7.11 D/A Conversion Value Setting Function

Figure 4.13 shows the flowchart of DAC0 conversion value setting.

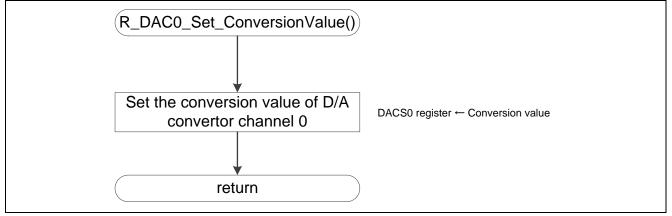


Figure 4.13 D/A conversion value setting function



4.7.12 D/A Converter Operation Start Function

Figure 4.14 shows the flowchart of D/A converter operation start function.

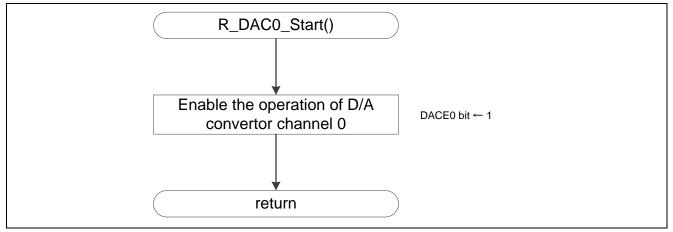


Figure 4.14 D/A converter operation start function

Enable D/A conversion

• D/A Converter mode register (DAM)

Symbol : DAM

7	6	5	4	3	2	1	0
0	0	DACE1	DACE0	0	0	DAMD1	DAMD0
Х	Х	Х	1	Х	Х	Х	Х

 $x \vdots$ bits that do not change

Bit	4	

DACE0	D/A conversion operation control
0	Stops D/A conversion operation
1	Enables D/A conversion operation

Note: Refer to the RL78/G14 User's Manual (Hardware version) for details on how to set registers.



4.7.13 INTC0 Interrupt

Figure 4.15 shows the flowchart of INTC0 interrupt.

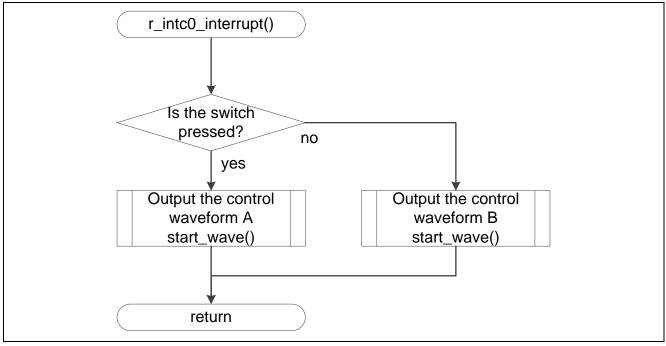


Figure 4.15 INTC0 interrupt



4.7.14 Starting output square wave

Figure 4.16 shows the flowchart of starting output square wave.

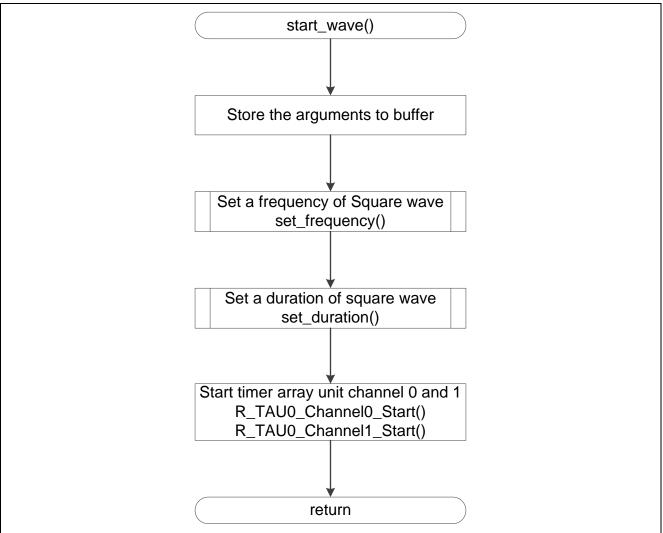


Figure 4.16 Starting output square wave



4.7.15 Frequency Setting of Output Wave

Figure 4.17 shows the flowchart of frequency setting of output wave.

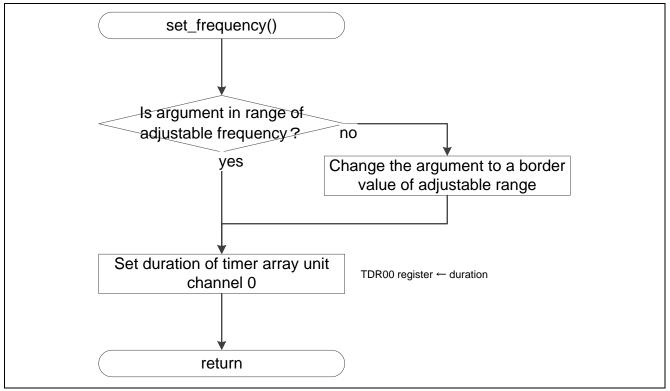


Figure 4.17 Frequency setting of output wave



4.7.16 Duration Setting of Output Wave

Figure 4.18 shows the flowchart of duration setting of output wave.

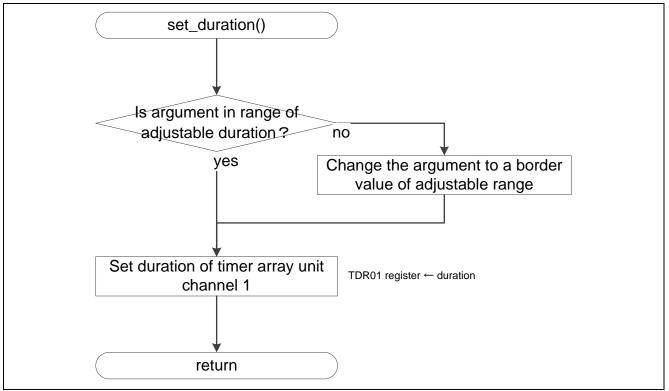


Figure 4.18 Duration setting of output wave



4.7.17 TAU00 Operation Start Function

Figure 4.19 shows the flowchart of TAU00 operation start function.

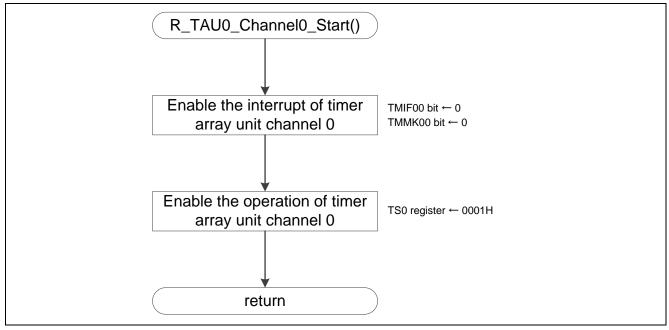


Figure 4.19 TAU00 operation start function

Start count operation

• Timer Channel Start Register (TS0)

Symbol : TS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TS	0	TS	0	0	0	0	0	TS	TS	TS	TS
				H03		H01						03	02	01	00
Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	1

x: bits that do not change

Bit O

DIUU	
TS00	Operation enable (start) trigger of channel 0
0	No trigger operation
1	The TE00 bit is set to 1 and the count operation becomes enabled. The TCR00 register count operation start in the count operation enabled state varies depending on each operation mode

Note: Refer to the RL78/G14 User's Manual (Hardware version) for details on how to set registers.



4.7.18 TAU01 Operation Start Function

Figure 4.20 shows the flowchart of TAU01 operation start function.

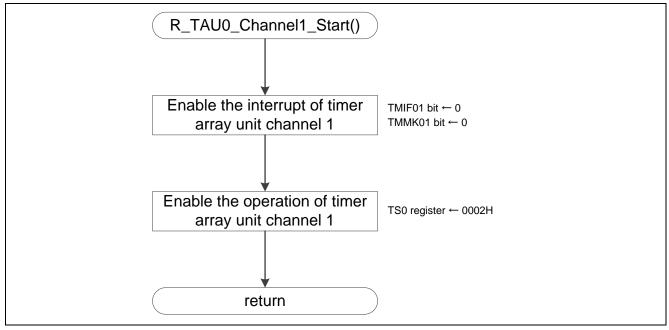
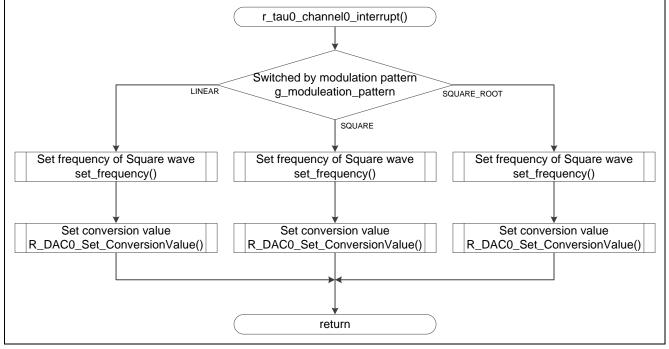


Figure 4.20 TAU01 operation start function

4.7.19 TAU00 Interrupt

Figure 4.21 shows the flowchart of TAU00 interrupt.







4.7.20 TAU01 Interrupt

Figure 4.22 shows the flowchart of TAU01 interrupt.

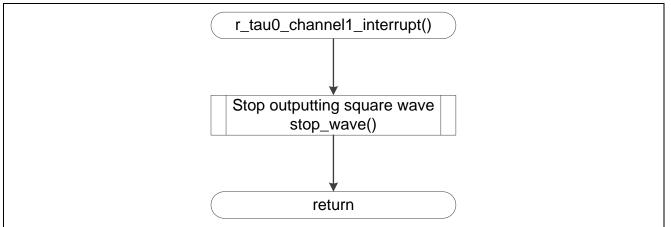


Figure 4.22 TAU01 interrupt

4.7.21 Stopping output square wave

Figure 4.23 shows the flowchart of stopping output square wave.

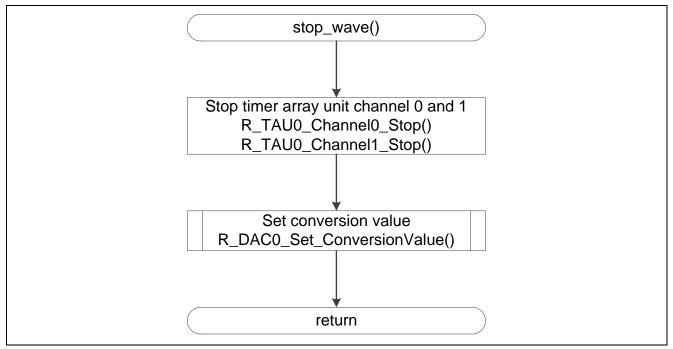


Figure 4.23 Stopping output square wave



4.7.22 TAU00 Operation Stop Function

Figure 4.24 shows the flowchart of TAU00 operation stop function

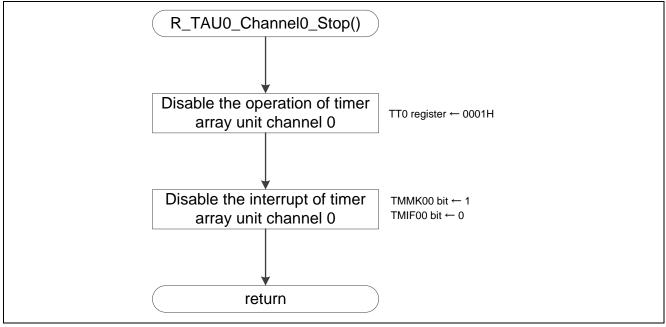


Figure 4.24 TAU00 operation stop function

4.7.23 TAU01 Operation Stop Function

Figure 4.25 shows the flowchart of TAU01 operation stop function.

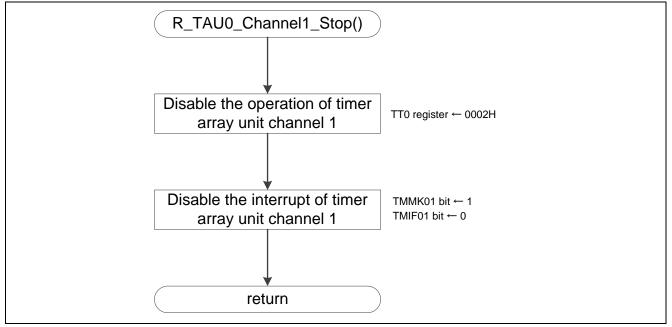


Figure 4.25 TAU01 operation stop function



5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

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Revision History

		Descript	tion	
Rev.	Date	Page	Summary	
1.00	Dec. 17, 2018	_	First edition	

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

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Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
- 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

 The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

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- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
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After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
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