RL78/G13

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Evening Out the Variations in Brightness of Multiple LEDs CC-RL

Introduction

This application note describes the procedures for adjusting LED drive current to even out the variations in brightness of multiple LEDs.

The timer array unit, A/D converter, and multiplier and divider/multiply-accumulator of the RL78/G13 are used in this application note.

Target Device

RL78/G13

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

The sample program covered in this application note evens out the variations in brightness of multiple LEDs by using the A/D converter, multiplier and divider/multiply-accumulator, and PWM output of the timer array unit.

There are some variations in LED forward voltage; therefore, even if the same voltage is applied to all LEDs, the brightness of all the LEDs may not become equal. Because of such variations in the LED forward voltage, the voltage applied to the resistor limiting the LED drive current (hereinafter called the current-limiting resistor) may not become equal, either. Therefore, to make the brightness of all the LEDs equal, it is necessary to adjust the drive current of each LED.

The sample program covered in this application note, to make the brightness of all the LEDs equal, first measures the forward voltage of each LED by using the A/D converter. In order that the average current flowing into each current-limiting resistor may become equal, the sample program adjusts the PWM output duty ratio of the timer array unit to control the drive current of each LED.

Table 1.1 shows the required peripheral functions and their uses.

Table 1.1 Peripheral Functions and Applications

Peripheral Function	Application
Timer Array Unit Channel 0	Sets the cycle of PWM output.
Timer Array Unit Channel 1	Used to output PWM to LED1.
Timer Array Unit Channel 2	Used to output PWM to LED2.
Timer Array Unit Channel 3	Used to output PWM to LED3.
A/D converter	Obtains an LED forward voltage value.
Multiplier and Divider/Multiply-Accumulator	Calculates the duty ratio of PWM output.

1.1 Evening Out the Variations in Brightness of LEDs

One of the methods for making the brightness of multiple LEDs equal is to adjust the resistance value of each current-limiting resistor. However, actually replacing resistors is a time-consuming task, impairing production efficiency. The sample program in this application note uses software to adjust the brightness of multiple LEDs for improved production efficiency.

A target LED forward current value is such that it will maximize the forward voltage (refer to the electrical specifications of LEDs). The sample program adjusts the PWM output (low active) duty ratio of the timer array unit so that the average current flowing into each limiting resistor may become the target value.

First, the LED drive circuit (Figure 1.1) used to output a low level from the output port to turn on the LED. Next, the A/D converter is used to measure the LED forward voltage. For LEDs with low forward voltage, the PWM output (low active) duty ratio is lowered to adjust the average current (LED forward current) flowing into each current-limiting resistor to the target value.

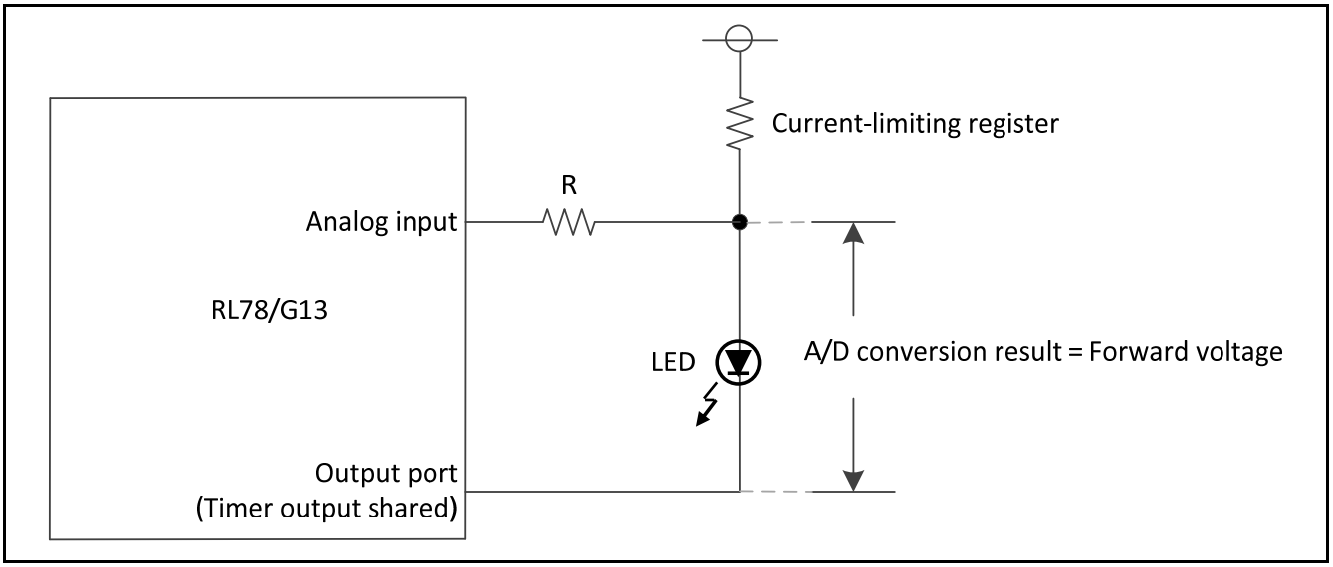

Figure 1.1 LED Drive Circuit

1.1.1 How to Calculate the Reference Value of Voltage Across Current-Limiting Resistor

The reference value is calculated of the voltage across the current-limiting resistor that achieves the target LED forward current value. Using this reference value, the duty ratio of the PWM output is determined.

The "supply voltage" and "maximum forward voltage value" are defined as constants in advance, and the reference value of the voltage across the current-limiting resistor is calculated by the following formula.

Reference value of voltage across current-limiting resistor
= Supply voltage – Maximum forward voltage value

The above value is replaced with the value equivalent to the A/D conversion result. When the maximum forward voltage value is 2.5 V and the supply voltage is 5.0 V:

Reference value of voltage across current-limiting resistor
= Maximum A/D conversion value – (Maximum A/D conversion value
** (Maximum forward voltage value / Supply voltage))*

*= 1024 – (1024 * (2.5 / 5))*

= 512

1.1.2 How to Measure the Voltage Across Current-Limiting Resistor

The LED drive circuit (Figure 1.1) is used to output a low level from the output port to turn on the LED. Next, the A/D converter is used to measure the LED forward voltage. The voltage across the current-limiting resistor is calculated by the following formula.

Measurement value of voltage across current-limiting resistor
= Supply voltage – Forward voltage
= Maximum A/D conversion value – A/D conversion result
= 1024 – A/D conversion result

1.1.3 How to Calculate the PWM Output Duty Ratio

The PWM output duty ratio is calculated as follows.

Duty ratio of PWM output
= (Reference value of voltage across current-limiting resistor) / (Measurement value of voltage across current-limiting resistor)

The setting value of the PWM output is calculated as follows.

*Setting value of PWM output = Cycle of PWM output * Duty ratio of PWM output*
*= Cycle of PWM output * (Reference value of voltage across current-limiting resistor) / (Measurement value of voltage across current-limiting resistor)*
*= Cycle of PWM output * 512 / (Measurement value of voltage across current-limiting resistor)*

The above calculation result is set to the TDR01 to TDR03 registers that correspond to the PWM outputs.

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	RL78/G13（R5F100LE）
Operating frequencies	● High-speed on-chip oscillator clock: 32MHz
Operating voltage	5.0V (operating range 2.7V to 5.5V) LVD operations (V_{LVD}): reset mode 2.81V (2.76V to 2.87V)
Integrated development environment (CS+)	CS+ for CC V6.00.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.05.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V5.4.0.018 from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.05.00 from Renesas Electronics Corp.

3. Related Application Notes

Application notes related to this document are shown below. Please refer to these as needed.

RL78/G13 A/D Converter (Software Trigger and Sequential Conversion Modes) CC-RL (R01AN2581EJ)
RL78/G13 Timer Array Unit (PWM Output) CC-RL (R01AN2589EJ)

4. Hardware Explanation

4.1 Hardware Configuration Example

Figure 4.1 shows an example of the hardware configuration used in this application note.

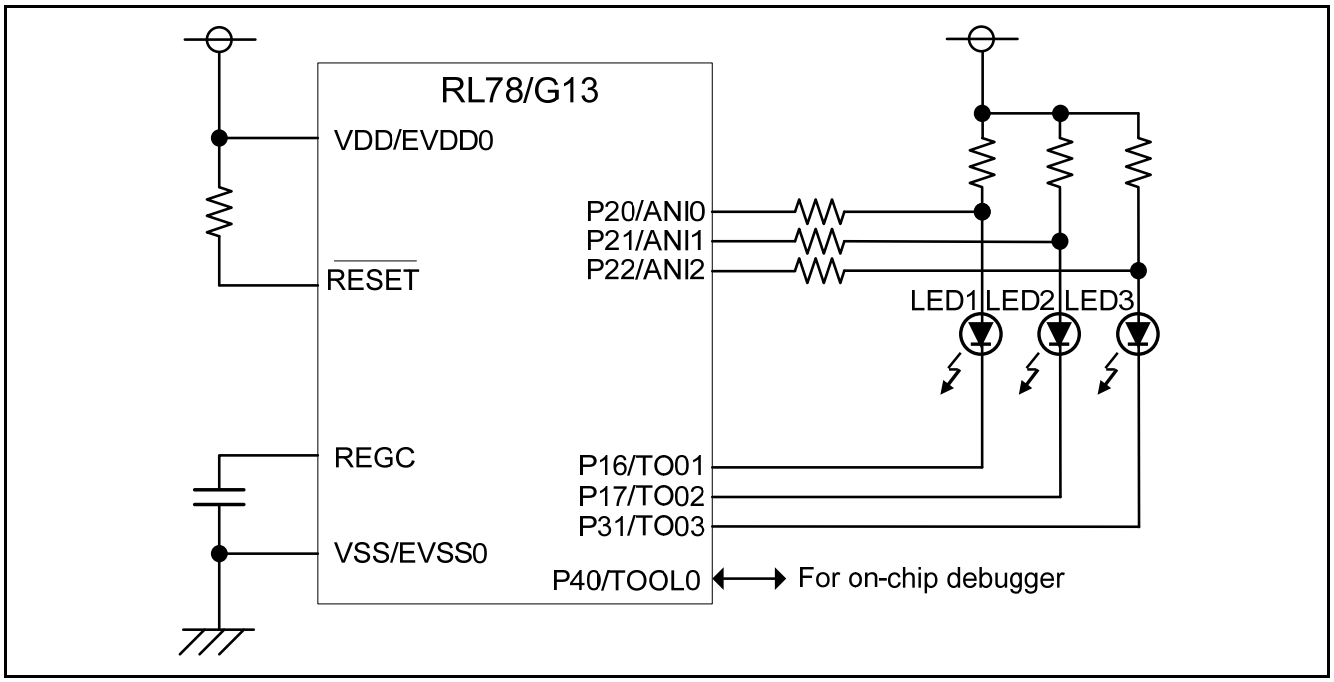

Figure 4.1 Hardware Configuration

Note: 1. This simplified circuit diagram was created to show an overview of connections only.
When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements. (Connect each input-only port to V_{DD} or V_{SS} through a resistor.)

4.2 Used Pin List

Table 4.1 provides List of Pins and Functions.

Table 4.1 List of Pins and Functions

Pin Name	Input/Output	Function
P16/TO01	Output	Outputs multiple PWM to LED1.
P17/TO02	Output	Outputs multiple PWM to LED2.
P20/ANI0	Input	Inputs the forward voltage of LED1 as an analog input port.
P21/ANI1	Input	Inputs the forward voltage of LED2 as an analog input port.
P22/ANI2	Input	Inputs the forward voltage of LED3 as an analog input port.
P31/TO03	Output	Outputs multiple PWM to LED3.

5. Software Explanation

5.1 Operation Outline

The sample program covered in this application note evens out the variations in brightness of LEDs by using the A/D converter, multiplier and divider/multiply-accumulator, and PWM output of the timer array unit.

The maximum forward voltage of the LEDs to be used is checked referring to the electrical specifications of the LEDs to define the "maximum forward voltage value" as a constant. The multiplier and divider/multiply-accumulator are used to calculate the reference voltage value across the current-limiting resistor.

Next, the forward voltages of the LEDs connected with the output ports are measured using the A/D converter, and the voltage across the current-limiting resistor (measurement value) is calculated.

The measured voltage across the current-limiting resistor is compared with the reference value and he PWM output duty ratio is calculated.

The details are shown in ① to ㉓ below.

① Initialize the A/D converter.

<Conditions for setting the A/D converter>

- The analog input channel is set to ANI0.
- A/D conversion channel selection mode is set to select mode.
- A/D conversion operation mode is set to one-shot conversion mode.
- Software trigger is set as an A/D conversion start condition.
- Set the A/D conversion time to 19 μs.

② Initialize the timer array unit.

<Conditions for setting channel 0>

- Timer operation mode is set to PWM output (master).
- Timer output enable register is set to disable operation.
- Timer interrupt (INTTM00) from timer channel 0 is not used.

<Conditions for setting channel 1>

- Timer operation mode is set to PWM output (slave).
- Timer output enable register is set to enable operation.
- Timer interrupt (INTTM01) from timer channel 1 is not used.

<Conditions for setting channel 2>

- Timer operation mode is set to PWM output (slave).
- Timer output enable register is set to enable operation.
- Timer interrupt (INTTM02) from timer channel 2 is not used.

<Conditions for setting channel 3>

- Timer operation mode is set to PWM output (slave).

- Timer output enable register is set to enable operation.
- Timer interrupt (INTTM03) from timer channel 3 is not used.

③ After initialization, maskable interrupts are disabled.

④ In order to measure LED forward voltage correctly, the wait time is inserted for the supply voltage to be stabilized.

⑤ By using the multiplier and divider/multiply-accumulator, "Maximum value of A/D conversion * Maximum value of forward voltage / Supply voltage" is calculated.

⑥ The value calculated in ⑤ is subtracted from the maximum A/D conversion value to calculate the reference voltage value across the current-limiting resistor.

⑦ The cycle of the PWM output of the timer array unit is set.

⑧ The output port where the LED is connected is set to a low level.

⑨ The A/D comparator of the A/D converter is set to enable operation, and wait time is inserted for the A/D power supply to be stabilized.

⑩ Analog input channels are changed according to the port to measure.

⑪ A/D conversion processing is started, the chip is placed in HALT mode to wait for an A/D conversion end interrupt request to be generated.

⑫ The A/D conversion end interrupt request flag is cleared, and then the A/D conversion result is stored in a variable.

⑬ Steps ⑨ to ⑪ are repeated until A/D conversion is finished for all the ports where the LEDs are connected.

⑭ The output ports where the LED is connected are set to a high level.

⑮ The clock supply to the A/D converter is stopped.

⑯ By using the multiplier and divider/multiply-accumulator, "Cycle of PWM output * Reference voltage value across the current-limiting resistor" is calculated.

⑰ The A/D conversion result is subtracted from the maximum A/D conversion value to calculate the measurement value voltage across the current-limiting resistor.

⑱ If the measurement voltage value across the current-limiting resistor is smaller than the reference value, the setting value of 100% duty ratio is set. If the measurement value is larger than the reference value, the calculation result in ⑯ is divided by the subtraction result in ⑰ by using the multiplier and divider/multiply-accumulator, and the division result is set as the setting value of the PWM output.

⑲ Steps ⑯ to ⑱ are repeated until the setting value of the PWM output is calculated for all the ports where the LEDs are connected.

⑳ The calculated cycle and setting value of the PWM output are set to the TDR00 to TDR03 registers of the timer array unit.

㉑ The output ports where the LED is connected are set to a low level.

㉒ The PWM output of the timer array unit are started.

㉓ The chip is placed in HALT mode.

5.2 Option Byte Settings

Table 5.1 lists the option byte settings.

Table 5.1 Option Byte Settings

Address	Setting Value	Contents
000C0H/010C0H	1110 1111B	Watchdog timer operation is stopped (count is stopped after reset)
000C1H/010C1H	0111 1011B	LVD operation (V_{LVD}): reset mode Detection voltage: 2.81V (2.76V to 2.87V)
000C2H/010C2H	1110 1000B	HS mode, High-speed on-chip oscillator clock: 32 MHz
000C3H/010C3H	1000 0100B	On-chip debugging enabled

5.3 Constants

Table 5.2 lists the constants that are used in this sample program.

Table 5.2 Constants for the Sample program

Constant Name	Setting Value	Contents
VF_MAX	2500	Maximum LED forward voltage value (mV)
VDD	5000	Supply voltage (mV)
AD_CONVERSION_RESULT_MAX	1024	Maximum A/D conversion value

5.4 Variables

Table 5.3 lists the variables.

Table 5.3 Variables

Type	Variable Name	Contents	Function Used
uint16_t	g_data[2]	Value of calculation process	Main, R_MAIN_UserInit, r_get_pwm_duty
uint16_t	g_vf_value[3]	Forward voltage value	Main, r_get_vf_value, r_get_pwm_duty
uint16_t	g_pwm_period	Cycle of PWM output	Main, R_MAIN_UserInit, r_get_pwm_duty
uint16_t	g_pwm_base	Reference value in calculation of PWM output duty ratio	R_MAIN_UserInit, r_get_pwm_duty
uint16_t	g_pwm_duty[3]	Setting value of PWM output	r_get_pwm_duty
uint8_t	g_ads[3]	Setting value to ADS register	r_get_vf_value

5.5 Functions

Table 5.4 lists the functions.

Table 5.4 Functions

Function Name	Outline
main	Main processing
R_MAIN_UserInit	Main initial setting
r_get_vf_value	Forward voltage value get function
r_get_pwm_duty	PWM output value calculation function
R_ADC_Start	A/D conversion operation start function
R_ADC_Stop	A/D conversion operation stop function

5.6 Function Specifications

This part describes function specifications of the sample code.

[Function Name]	main
Outline	Main processing
Header	r_cg_macrodriver.h, r_cg_cgc.h, r_cg_port.h, r_cg_adc.h, r_cg_timer.h, r_cg_userdefine.h
Declaration	―
Description	Executes the forward voltage value get function and the PWM output value calculation function after executing the main user initialization function. The setting value of the PWM output is calculated so that the average current flowing into each limiting resistor may become equal. The calculated setting value of the PWM output is set to the TDR00 to TDR03 registers of the timer array unit. PWM output is started to drive the LED. After that, the chip is placed in HALT mode.
Arguments	None
Remarks	None

[Function Name]	R_MAIN_UserInit
Outline	Main initial setting
Header	r_cg_macrodriver.h, r_cg_cgc.h, r_cg_port.h, r_cg_adc.h, r_cg_timer.h, r_cg_userdefine.h
Declaration	static void R_MAIN_UserInit(void);
Description	Disables interrupt processing by the DI instruction. Next, wait time is inserted for the supply voltage to be stabilized. After that, by using the multiplier and divider/multiply-accumulator, the reference voltage value across the current-limiting resistor is calculated.
Arguments	None
Remarks	None

[Function Name]	r_get_vf_value
Outline	Forward voltage value get function
Header	r_cg_macrodriver.h, r_cg_cgc.h, r_cg_port.h, r_cg_adc.h, r_cg_timer.h, r_cg_userdefine.h
Declaration	void r_get_vf_value(void);
Description	Outputs a low level from the output port to turn on the LED. Next, the LED forward voltage is measured by using the A/D converter. After the measurement, a high level is output from the output port to turn off the LED. The clock supply to the A/D converter is stopped.
Arguments	None
Remarks	None

[Function Name]	r_get_pwm_duty
Outline	PWM output value calculation function
Header	r_cg_macrodriver.h, r_cg_cgc.h, r_cg_port.h, r_cg_adc.h, r_cg_timer.h, r_cg_userdefine.h
Declaration	void r_get_pwm_duty(void);
Description	Calculates the setting value of the PWM output by using the multiplier and divider/multiply-accumulator.
Arguments	None
Remarks	None

[Function Name]	R_ADC_Start
Outline	A/D conversion operation start function
Header	r_cg_macrodriver.h, r_cg_adc.h
Declaration	void R_ADC_Start(void);
Description	Start the A/D conversion operation.
Arguments	None
Remarks	None

[Function Name]	R_ADC_Stop
Outline	A/D conversion operation stop function
Header	r_cg_macrodriver.h, r_cg_adc.h
Declaration	void R_ADC_Stop(void);
Description	Stops the A/D conversion operation.
Arguments	None
Remarks	None

5.7 Flowcharts

Figure 5.1 shows an overall flow of the sample code.

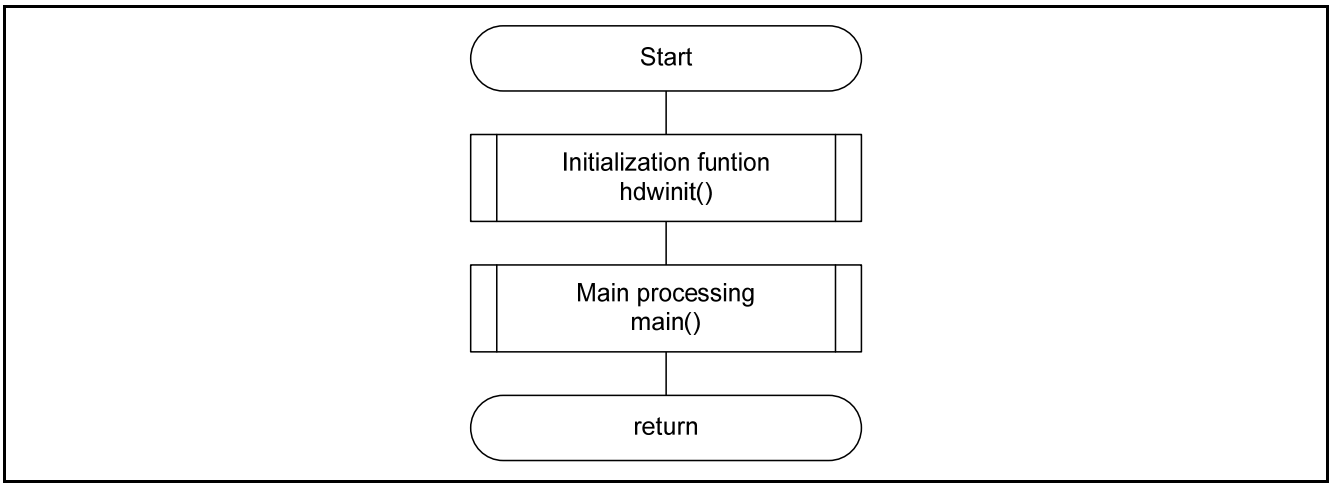

Figure 5.1 Overall Flow

5.7.1 Initialization Function

Figure 5.2 shows the flowchart for the initialization function.

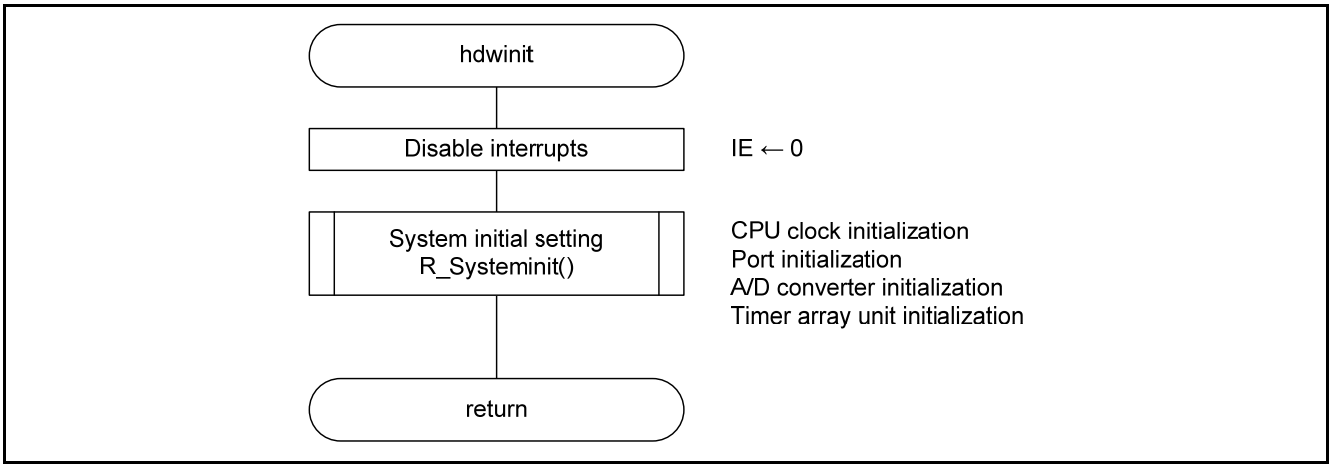

Figure 5.2 Initialization Function

5.7.2 System Initial Setting

Figure 5.3 shows the flowchart for the system initial setting.

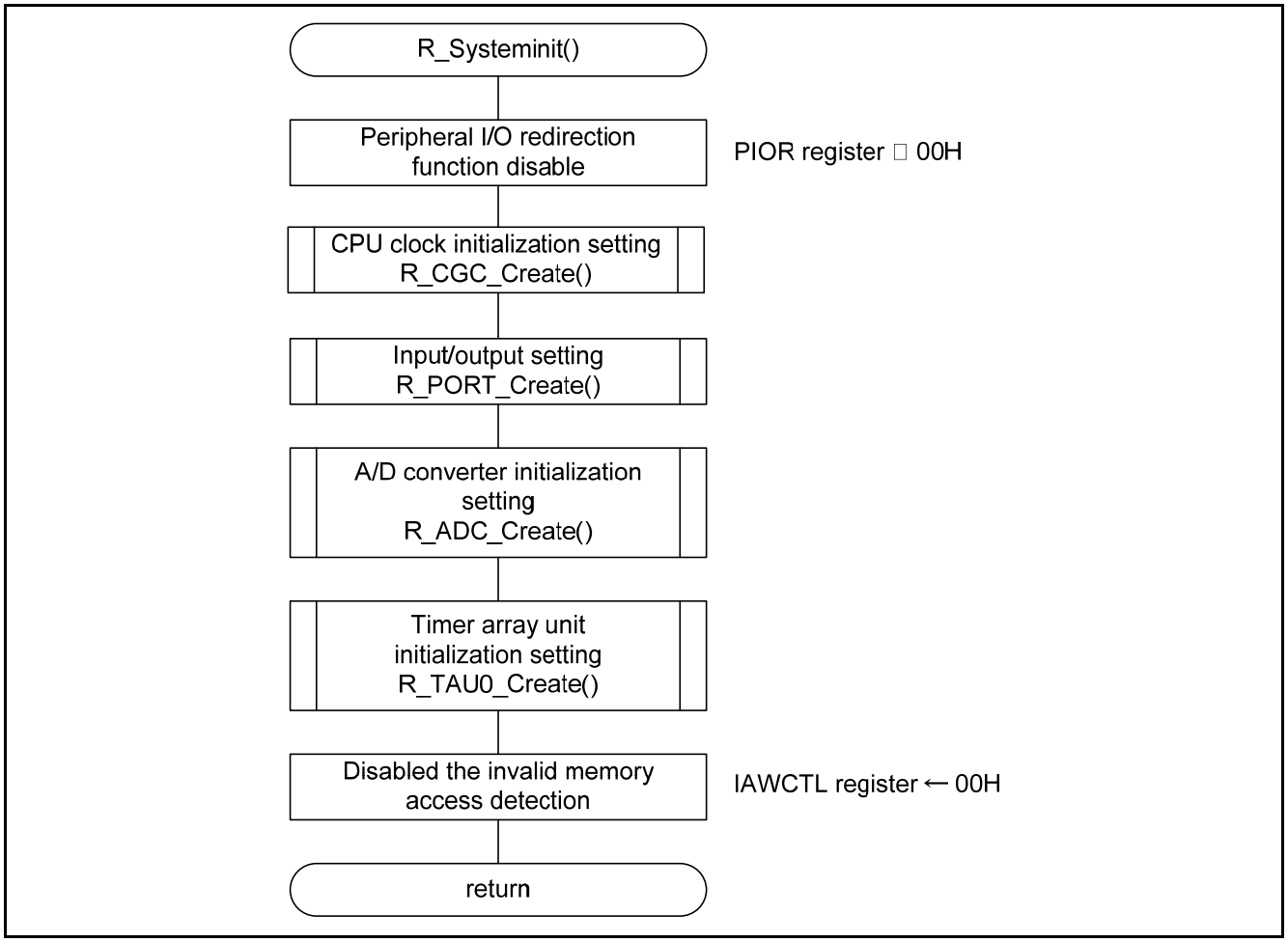

Figure 5.3 System Initial Setting

5.7.3 Ports Initial Setting

Figure 5.4 shows the flowchart for the ports initial setting.

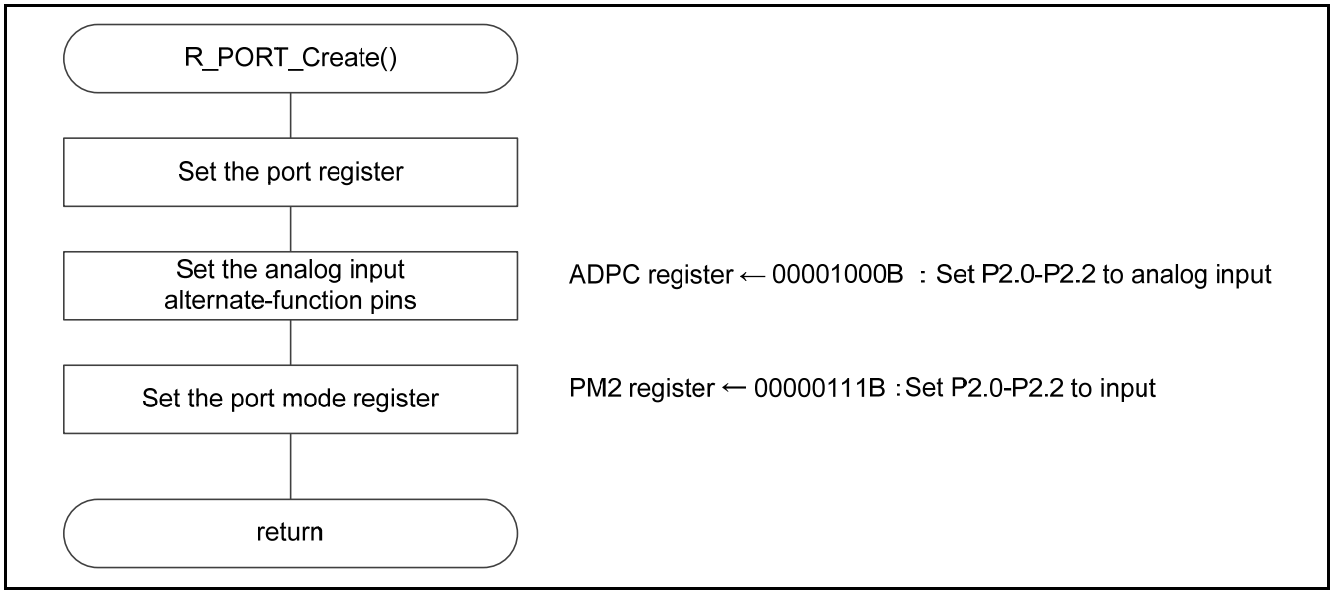

Figure 5.4 Port Initial Setting

Note: Refer to the initialization flowchart in the RL78/G13 Initialization CC-RL (R01AN2575E) Application Note for details on how to set unused ports.

Caution: When designing circuits, always make sure unused ports are properly processed and all electrical characteristics are met. Also make sure each unused input-only port is connected to VDD or VSS through a resister.

5.7.4 CPU Initial Setting

Figure 5.5 shows the flowchart for the CPU initial setting.

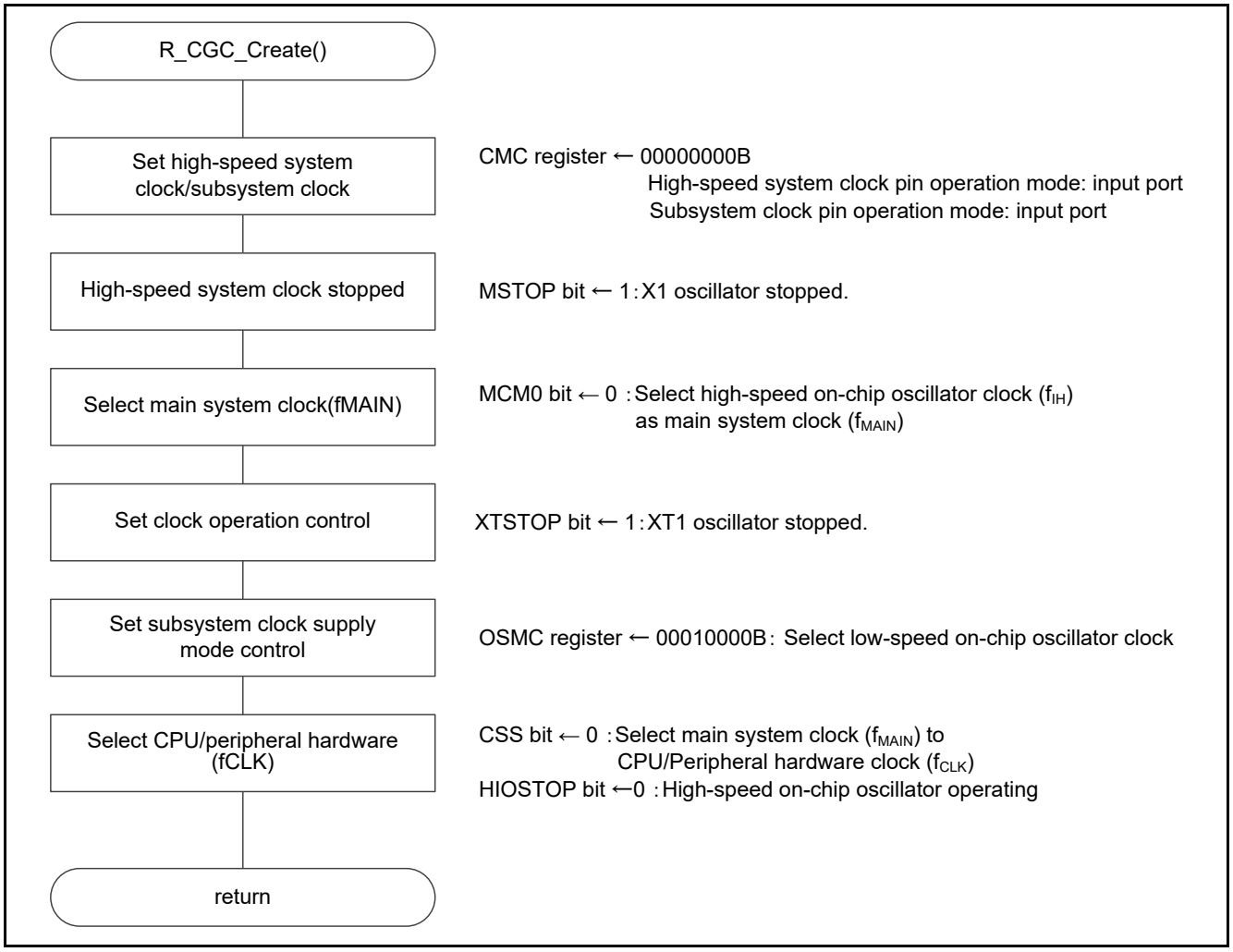

Figure 5.5 CPU Initial Setting

Clock operation mode setting

- Clock operation mode control register (CMC)
  High-speed system clock pin operation mode: input port mode
  Subsystem clock pin operation mode: input port mode

Symbol: CMC

7	6	5	4	3	2	1	0
EXCLK	OSCSEL	EXCLKS	OSCSELS	0	AMPHS1	AMPHS0	AMPH
0	**0**	**0**	**0**	0	**0**	**0**	**0**

Bits 7-6

EXCLK	OSCSEL	High-seed oscillation clock pin operation mode	X1/P121 Port	X2/EXCLK/P122 Port
0	**0**	**Input port mode**	**Input port**	
0	1	X1 oscillation mode	Crystal/ceramic resonator connection	
1	0	Input port mode	Input port	
1	1	External clock input mode	Input port	External clock input

Bits 5-4

EXCLKS	OSCSELS	Subsystem clock pin operation mode	XT1/P123 Pin	XT2/EXCLKS/P124 Pin
0	**0**	**Input port mode**	**Input port**	
0	1	XT1 oscillation mode	Crystal resonator connection	
1	0	Input port mode	Input port	
1	1	External clock input mode	Input port	External clock input

Bits 2-1

AMPHS1	AMPHS0	XT1 oscillator oscillation mode selection
0	**0**	**Low-power consumption oscillation (default)**
0	1	Normal oscillation
1	0	Ultra-low power consumption oscillation
1	1	Setting prohibited

Bit 0

AMPH	Control of X1 clock oscillation frequency
0	**1MHz ≤ f_X ≤ 10MHz**
1	10MHz < f_X ≤ 20MHz

Note: Refer to the RL78/G13 User's Manual (Hardware version) for details on how to set registers.

Operation control of clocks

- Clock operation status control register (CSC)

High-speed system clock operation control: X1 oscillator stopped
Subsystem clock operation control: XT1 oscillator stopped
High-speed on-chip oscillator clock operation control: High-speed on-chip oscillator

Symbol: CSC

7	6	5	4	3	2	1	0
MSTOP	XTSTOP	0	0	0	0	0	HIOSTOP
1	**1**	0	0	0	0	0	**0**

Bit 7

MSTOP	High-speed system clock operation control		
	X1 oscillation mode	External clock input mode	Input port mode
0	X1 oscillator operating	External clock from EXCLK pin is valid	**Input port**
1	**X1 oscillator stopped**	External clock from EXCLK pin is invalid	

Bit 6

XTSTOP	Subsystem clock operation control		
	XT1 oscillation mode	External clock input mode	Input port mode
0	XT1 oscillator operating	External clock from EXCLKS pin is valid	**Input port**
1	**XT1 oscillator stopped**	External clock from EXCLKS pin is invalid	

Bit 0

HIOSTOP	High-speed on-chip oscillator clock operation control
0	**High-speed on-chip oscillator operating**
1	High-speed on-chip oscillator stopped

Note: Refer to the RL78/G13 User's Manual (Hardware version) for details on how to set registers.

System clock control setting

- System clock control register (CKC)

Select the high-speed on-chip oscillator clock as a CPU/peripheral hardware clock.

Symbol: CKC

7	6	5	4	3	2	1	0
CLS	CSS	MCS	MCM0	0	0	0	0
0	**0**	**0**	**0**	0	0	0	0

Bit 6

CSS	Selection of CPU/peripheral hardware clock (f_{CLK})
0	**Main system clock (f_{MAIN})**
1	Subsystem clock (f_{SUB})

Bit 4

MCM0	Main system clock (f_{MAIN}) operation control
0	**Selects the high-speed on-chip oscillator clock (f_{IH}) as the main system clock (f_{MAIN})**
1	Selects the high-speed system clock (f_{MX}) as the main system clock (f_{MAIN})

Note: Refer to the RL78/G13 User's Manual (Hardware version) for details on how to set registers.

5.7.5 A/D Converter Initial Setting

Figure 5.6 shows the flowchart for the A/D converter initial setting.

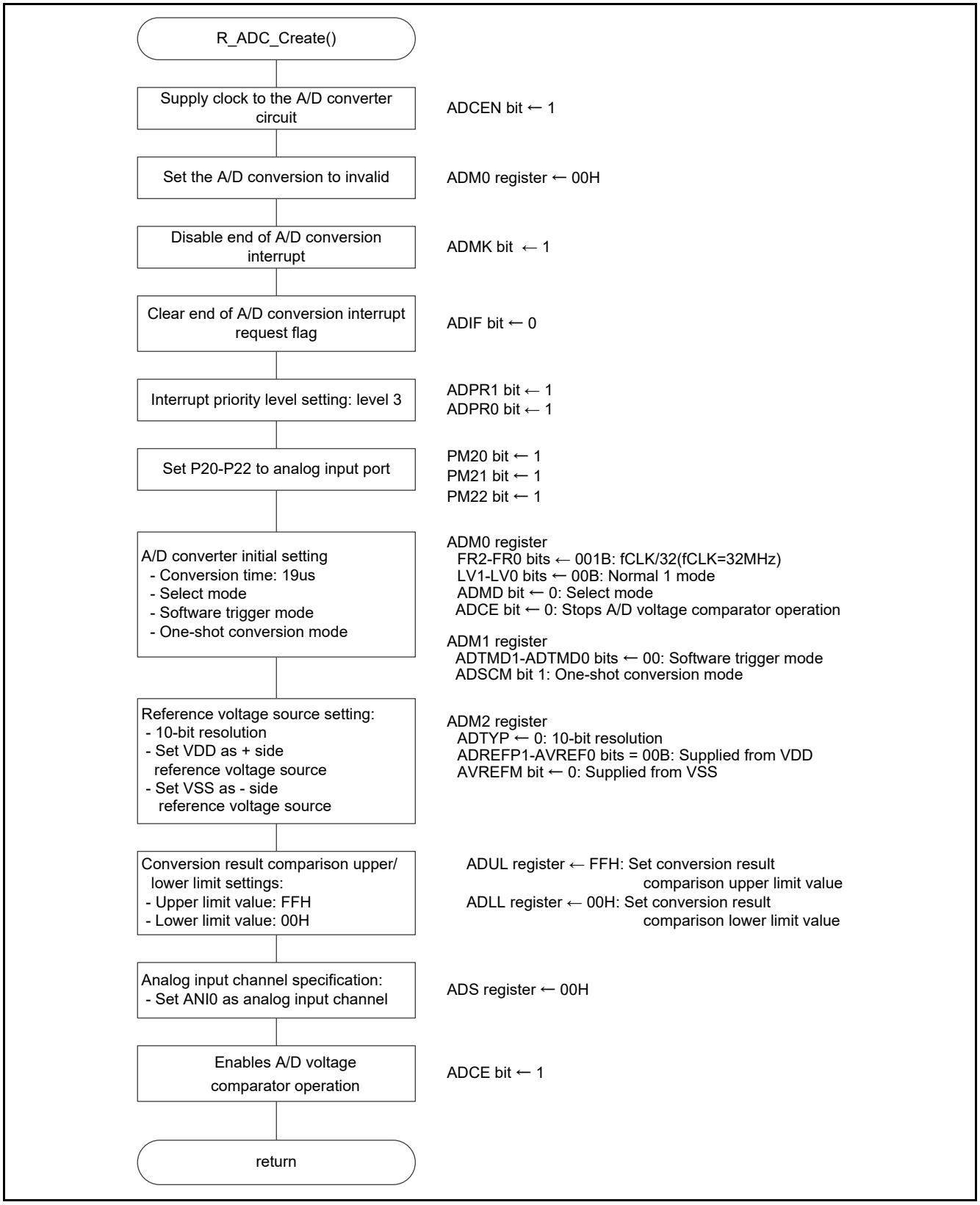

Figure 5.6 A/D Converter Initial Setting

Starting the supply of clock to the A/D

- Peripheral enable register 0 (PER0)

Starts the supply of the clock to the A/D converter.

Symbol: PER0

7	6	5	4	3	2	1	0
RTCEN	IICA1EN	ADCEN	IICA0EN	SAU1EN	SAU0EN	TAU1EN	TAU0EN
x	x	**1**	x	x	x	x	x

Bit 5

ADCEN	A/D converter input clock control
0	Stops supply of input clock.
1	**Starts supply of input clock.**

Note: Refer to the RL78/G13 User's Manual (Hardware version) for details on how to set registers.

Setting up the A/D conversion time and operation mode

- A/D converter mode register 0 (ADM0)

Controls the A/D conversion operation.

Specifies the A/D conversion channel selection mode.

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
x	**0**	**0**	**0**	**1**	**0**	**0**	x

Bit 6

ADMD	A/D channel selection mode select
0	**Select mode**
1	Scan mode

Bits 5-1

ADM0					Mode	Conversion Time Selection					Conversion Clock(f_{AD})
FR2	FR1	FR0	LV1	LV0		f_{CLK}= 1MHz	f_{CLK}= 4MHz	f_{CLK}= 8MHz	f_{CLK}= 16MHz	**f_{CLK}= 32MHz**	
0	0	0	**0**	**0**	**Standard 1**	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	38µs	f_{CLK}/64
0	**0**	**1**							38µs	**19µs**	**f_{CLK}/32**
0	1	0						38µs	19µs	9.5µs	f_{CLK}/16
0	1	1					38µs	19µs	9.5µs	4.75µs	f_{CLK}/8
1	0	0					28.5µs	14.25µs	7.125µs	3.5625µs	f_{CLK}/6
1	0	1					23.75µs	11.875µs	5.938µs	2.9688µs	f_{CLK}/5
1	1	0					19µs	9.5µs	4.75µs	2.375µs	f_{CLK}/4
1	1	1				38µs	9.5µs	4.75µs	2.375µs	Setting prohibited	f_{CLK}/2
0	0	0	0	1	Standard2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	34µs	f_{CLK}/64
0	0	1							34µs	17µs	f_{CLK}/32
0	1	0						34µs	17µs	8.5µs	f_{CLK}/16
0	1	1					34µs	17µs	8.5µs	4.25µs	f_{CLK}/8
1	0	0					25.5µs	12.75µs	6.375µs	3.1875µs	f_{CLK}/6
1	0	1					21.25µs	10.625µs	5.3125µs	2.6536µs	f_{CLK}/5
1	1	0					17µs	8.5µs	4.25µs	2.125µs	f_{CLK}/4
1	1	1				34µs	8.5µs	4.25µs	2.125µs	Setting prohibited	f_{CLK}/2

Note: Refer to the RL78/G13 User's Manual (Hardware version) for details on how to set registers.

Setting up the A/D conversion trigger mode

- A/D converter mode register 1 (ADM1)

Selects the A/D conversion trigger mode.
Selects the A/D conversion mode.

Symbol: ADM1

7	6	5	4	3	2	1	0
ADTMD1	ADTMD0	ADSCM	0	0	0	ADTRS1	ADTRS0
0	**0**	**1**	0	0	0	**0**	**0**

Bits 7-6

ADTMD1	ADTMD0	Selection of the A/D conversion trigger mode
0	**—**	**Software trigger mode**
1	0	Hardware trigger no-wait mode
1	1	Hardware trigger wait mode

Bit 5

ADSCM	Specification of the A/D conversion mode
0	Sequential conversion mode
1	**One-shot conversion mode**

Bits 1-0

ADTRS1	ADTRS0	Selection of the hardware trigger signal
0	**0**	**End of timer channel 01 count or capture interrupt signal (INTTM01)**
0	1	Setting prohibited
1	0	Real-time clock interrupt signal (INTRTC)
1	1	12-bit interval timer interrupt signal (INTIT)

Note: Refer to the RL78/G13 User's Manual (Hardware version) for details on how to set registers.

Setting up the reference voltage

- A/D converter mode register 2 (ADM2)

Sets up the reference voltage source.

Symbol: ADM2

7	6	5	4	3	2	1	0
ADREFP1	ADREFP0	ADREFM	0	ADCRK	AWC	0	ADTYP
0	**0**	**0**	0	**0**	**0**	0	**0**

Bits 7-6

ADREFP1	ADREFP0	Selection of the + side reference voltage source of the A/D converter
0	**0**	**Supplied from VDD.**
0	1	Supplied from P20/AVREFP/ANI0.
1	0	Supplied from internal reference voltage (1.45 V).
1	1	Setting prohibited

Bit 5

ADREFM	Selection of the – side reference voltage source of the A/D converter
0	**Supplied from VSS.**
1	Supplied from P21/AVREFM/ANI1.

Bit 3

ADCRK	Checking the upper limit and lower limit conversion result values
0	**The interrupt signal (INTAD) is output when the ADLL register ≤ the ADCR register ≤ the ADUL register.**
1	Interrupt signal (INTAD) is output when ADCR register < ADLL register and ADUL register < ADCR register.

Bit 2

AWC	Specification of the wakeup function (SNOOZE mode)
0	**Do not use the SNOOZE mode function.**
1	Use the SNOOZE mode function.

Bit 0

ADTYP	Selection of the A/D conversion resolution
0	**10-bit resolution**
1	8-bit resolution

Note: Refer to the RL78/G13 User's Manual (Hardware version) for details on how to set registers.

Setting up the conversion result comparison upper limit/lower limit

- Conversion result comparison upper limit setting register (ADUL)
- Conversion result comparison lower limit setting register (ADLL)

Sets up the conversion result comparison upper- and lower-limit values.

Symbol: ADUL

7	6	5	4	3	2	1	0
ADUL7	ADUL6	ADUL5	ADUL4	ADUL3	ADUL2	ADUL1	ADUL0
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Symbol: ADLL

7	6	5	4	3	2	1	0
ADLL7	ADLL6	ADLL5	ADLL4	ADLL3	ADLL2	ADLL1	ADLL0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Specifying the input channel

- Analog input channel specification register (ADS)

Specifies the input channel for the analog voltage to be subjected to A/D conversion.

Symbol: ADS

7	6	5	4	3	2	1	0
ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0
0	0	0	**0**	**0**	**0**	**0**	**0**

Bits 7, 4-0

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog Input Channel	Input Source
0	**0**	**0**	**0**	**0**	**0**	**ANI0**	**P20/ANI0/AV_{REFP} pin**
0	0	0	0	0	1	ANI1	P21/ANI1 /AV_{REFM} pin
0	0	0	0	1	0	ANI2	P22/ANI2 pin
0	0	0	0	1	1	ANI3	P23/ANI3 pin
0	0	0	1	0	0	ANI4	P24/ANI4 pin
0	0	0	1	0	1	ANI5	P25/ANI5 pin
0	0	0	1	1	0	ANI6	P26/ANI6 pin
0	0	0	1	1	1	ANI7	P27/ANI7 pin
0	1	0	0	0	0	ANI16	P03/ANI16 pin
0	1	0	0	0	1	ANI17	P02/ANI17 pin
0	1	0	0	1	0	ANI18	P147/ANI18 pin
0	1	0	0	1	1	ANI19	P120/ANI19 pin
1	0	0	0	0	0	—	Temperature sensor output voltage
1	0	0	0	0	1	—	Internal reference voltage(1.45V)
Other than above						Setting prohibited	

Note: Refer to the RL78/G13 User's Manual (Hardware version) for details on how to set registers.

5.7.6 Timer Array Unit Initial Setting

Figure 5.7 and Figure 5.8 shows the flowchart for the timer array unit initial setting.

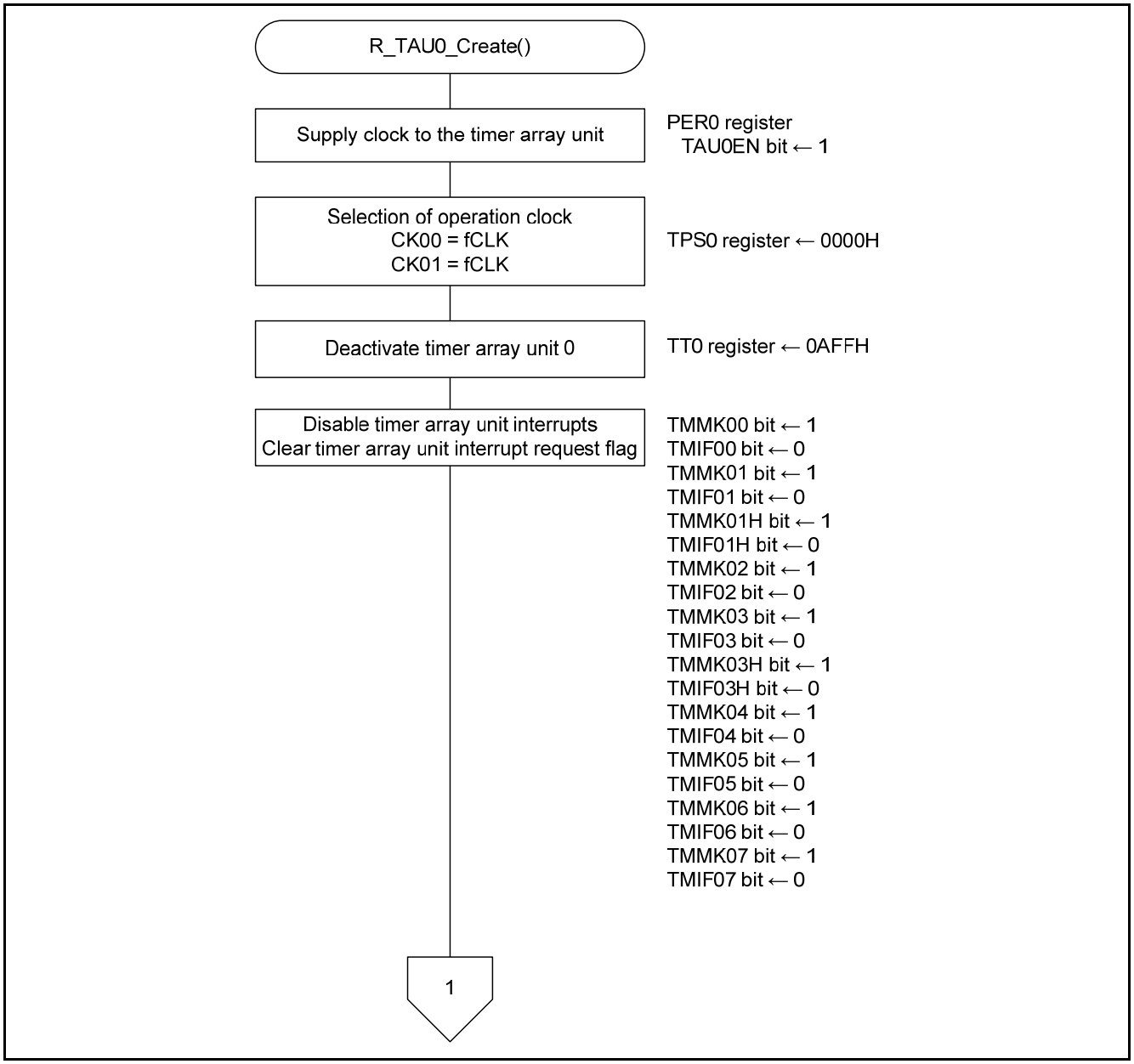

Figure 5.7 Timer Array Unit Initial Setting (1/2)

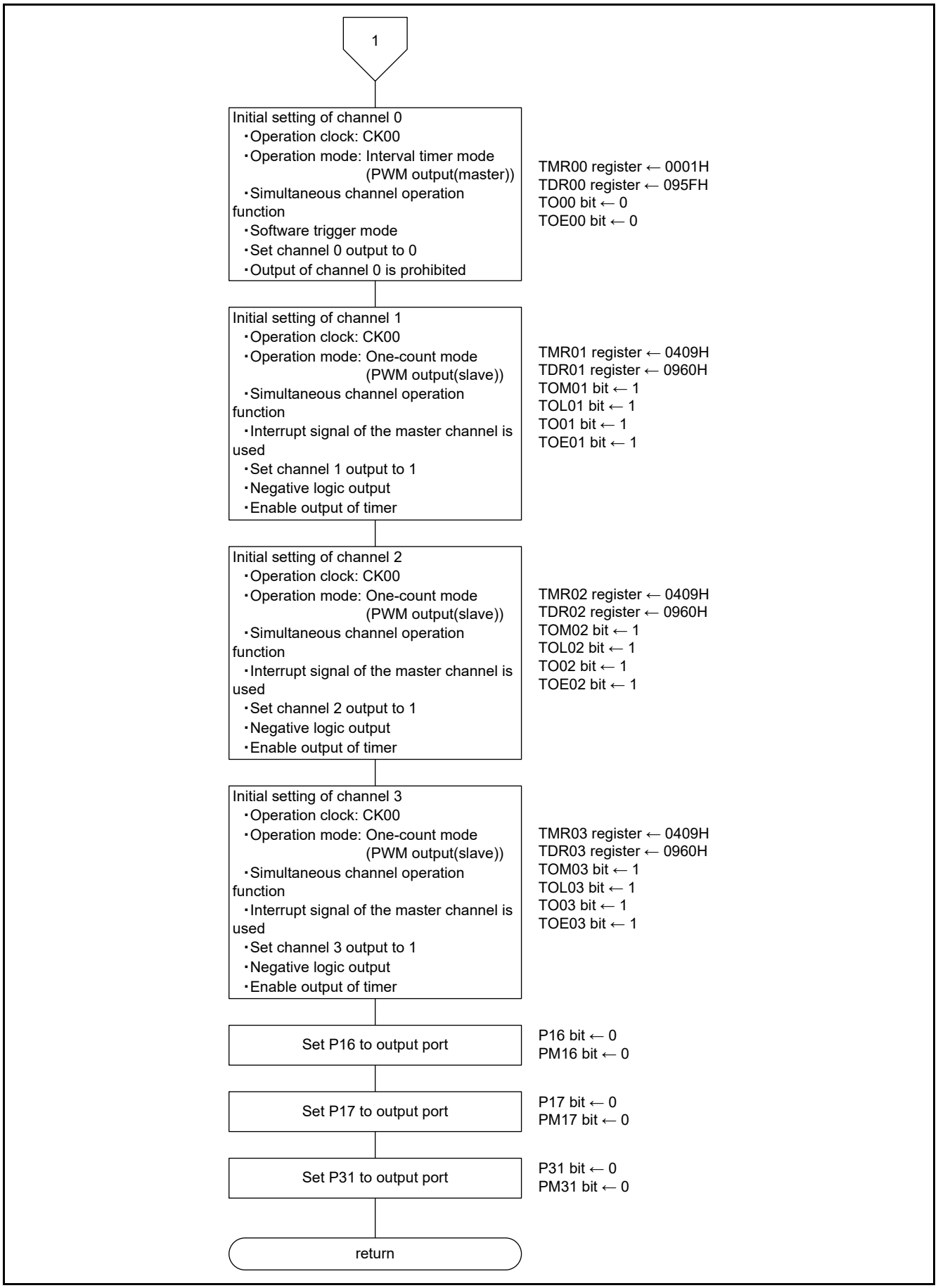

Figure 5.8 Timer Array Unit Initial Setting (2/2)

Clock supply to timer array unit started

- Peripheral enable register 0 (PER0)

Clock supply to timer array unit

Symbol: PER0

7	6	5	4	3	2	1	0
RTCEN	IICA1EN	ADCEN	IICA0EN	SAU1EN	SAU0EN	TAU1EN	TAU0EN
x	x	x	x	x	x	x	**1**

Bit 0

TAU0EN	Control of timer array 0 unit input clock
0	Stops supply of input clock.
1	**Supplies input clock.**

Operation clock setting

- Timer clock select register 0 (TPS0)

Selection of operation clock (CK00)

Symbol: TPS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	PRS 031	PRS 030	0	0	PRS 021	PRS 020	PRS 013	PRS 012	PRS 011	PRS 010	PRS 003	PRS 002	PRS 001	PRS 000
0	0	**0**	**0**	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**

PRS 003	PRS 002	PRS 001	PRS 000		Operation Clock (CK00) Selection				
					f_{CLK} = 2MHz	f_{CLK} = 5MHz	f_{CLK} = 10MHz	f_{CLK} = 20MHz	f_{CLK} = 32MHz
0	**0**	**0**	**0**	**f_{CLK}**	2MHz	5MHz	10MHz	20MHz	32MHz
0	0	0	1	$f_{CLK}/2$	1MHz	2.5MHz	5MHz	10MHz	12MHz
0	0	1	0	$f_{CLK}/2^2$	500kHz	1.25MHz	2.5MHz	5MHz	6MHz
0	0	1	1	$f_{CLK}/2^3$	250kHz	625kHz	1.25MHz	2.5MHz	3MHz
0	1	0	0	$f_{CLK}/2^4$	125kHz	312.5kHz	625kHz	1.25MHz	1.5MHz
0	1	0	1	$f_{CLK}/2^5$	62.5kHz	156.2kHz	312.5KHz	625KHz	750kHz
0	1	1	0	$f_{CLK}/2^6$	31.25kHz	78.1kHz	156.2kHz	312.5kHz	375kHz
0	1	1	1	$f_{CLK}/2^7$	15.62kHz	39.1kHz	78.1kHz	156.2kHz	187.5kHz
1	0	0	0	$f_{CLK}/2^8$	7.81kHz	19.5kHz	39.1kHz	78.1kHz	93.8kHz
1	0	0	1	$f_{CLK}/2^9$	3.91kHz	9.76kHz	19.5kHz	39.1kHz	46.9kHz
1	**0**	**1**	**0**	**$f_{CLK}/2^{10}$**	**1.95kHz**	**4.88kHz**	**9.76kHz**	**19.5kHz**	**23.4kHz**
1	0	1	1	$f_{CLK}/2^{11}$	976Hz	2.44kHz	4.88kHz	9.76kHz	11.7kHz
1	1	0	0	$f_{CLK}/2^{12}$	488Hz	1.22kHz	2.44kHz	4.88kHz	5.86kHz
1	1	0	1	$f_{CLK}/2^{13}$	244Hz	610Hz	1.22kHz	2.44kHz	2.93kHz
1	1	1	0	$f_{CLK}/2^{14}$	122Hz	305Hz	610Hz	1.22kHz	1.46kHz
1	1	1	1	$f_{CLK}/2^{15}$	61Hz	153Hz	305Hz	610Hz	732Hz

Note: Refer to the RL78/G13 User's Manual (Hardware version) for details on how to set registers.

Channel stop control

- Timer channel stop register 0 (TT0)

Stop the counting operation of each channel

Symbol: TT0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TT H03	0	TT H01	0	TT 07	TT 06	TT 05	TT 04	TT 03	TT 02	TT 01	TT 00
0	0	0	0	1	0	1	0	1	1	1	1	**1**	**1**	**1**	**1**

Bit 3

TT03	Operation stop trigger of channel 3
0	TE03 bit is cleared to 0 and the count operation is stopped.
1	**Operation is stopped (stop trigger is generated).**

Bit 2

TT02	Operation stop trigger of channel 2
0	TE02 bit is cleared to 0 and the count operation is stopped.
1	**Operation is stopped (stop trigger is generated).**

Bit 1

TT01	Operation stop trigger of channel 1
0	TE01 bit is cleared to 0 and the count operation is stopped.
1	**Operation is stopped (stop trigger is generated).**

Bit 0

TT00	Operation stop trigger of channel 0
0	TE00 bit is cleared to 0 and the count operation is stopped.
1	**Operation is stopped (stop trigger is generated).**

Note: Refer to the RL78/G13 User's Manual (Hardware version) for details on how to set registers.

Timer array unit 0 channel 0 initialization

- Timer mode register 00 (TMR00)
  Selection of operation mode, Selection start trigger,
  Selection of operation clock

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 001	CKS 000	0	CCS 00	0	STS 002	STS 001	STS 000	CIS 001	CIS 000	0	0	MD 003	MD 002	MD 001	MD 000
0	**0**	0	**0**	0	**0**	**0**	**0**	**0**	**0**	0	0	**0**	**0**	**0**	**1**

Bits 15-14

CKS001	CKS000	Selection of operation clock (f_{MCK}) for channel 0
0	**0**	**Operation clock CKm0 set in timer clock selection register m (TPSm)**
0	1	Operation clock CKm2 set in timer clock selection register m (TPSm)
1	0	Operation clock CKm1 set in timer clock selection register m (TPSm)
1	1	Operation clock CKm3 set in timer clock selection register m (TPSm)

Bit 12

CCS00	Selection of channel 0 operation clock (f_{TCLK})
0	**Operation clock (f_{MCK}) set in bits CKS000 and CKS001**
1	Valid edge of input signal from TI00 pin

Bits 10-8

STS 002	STS 001	STS 000	Setting start or capture trigger of channel 0
0	**0**	**0**	**Only software trigger start is valid (other trigger sources are unselected)**
0	0	1	Valid edge of TI00 pin input is used as both the start trigger and capture trigger
0	1	0	Both edges of TI00 pin input are used as the start trigger and capture trigger
1	0	0	Interrupt signal of master channel is used (when using slave channel with simultaneous channel operation function)
Other than above			Setting prohibited

Note: Refer to the RL78/G13 User's Manual (Hardware version) for details on how to set registers.

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 001	CKS 000	0	CCS 00	0	STS 002	STS 001	STS 000	CIS 001	CIS 000	0	0	MD 003	MD 002	MD 001	MD 000
0	**0**	0	**0**	0	**0**	**0**	**0**	**0**	**0**	0	0	**0**	**0**	**0**	**1**

Bits 7-6

CIS 001	CIS 000	Selection of TI00 pin input valid edge
0	**0**	**Falling edge**
0	1	Rising edge
1	0	Both edges (when low-level width is measured)
1	1	Both edges (when high-level width is measured)

Bits 3-0

MD 003	MD 002	MD 001	MD 000	Operation mode of channel 0
0	**0**	**0**	0	Interval timer mode (Timer interrupt is not generated when counting is started).
			1	**Interval timer mode** **(Timer interrupt is generated when counting is started）.**
0	1	0	0	**Capture mode** **(Timer interrupt is not generated when counting is started).**
			1	Capture mode (Timer interrupt is generated when counting is started).
0	1	1	0	Event counter mode (Timer interrupt is not generated when counting is started).
1	0	0	0	One-count mode (Start trigger is invalid during counting operation).
			1	One-count mode (Start trigger is valid during counting operation).
1	1	0	0	Capture & one-count mode (Timer interrupt is not generated when counting is started Start trigger is invalid during counting operation).
Other than above				Setting prohibited

Note: Refer to the RL78/G13 User's Manual (Hardware version) for details on how to set registers.

Timer array unit 0 channel 1 initialization

- Timer mode register 01 (TMR01)

Selection of operation mode, Selection start trigger,
Selection of operation clock

Symbol: TMR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 011	CKS 010	0	CCS 01	SPLIT 01	STS 012	STS 011	STS 010	CIS 011	CIS 010	0	0	MD 013	MD 012	MD 011	MD 010
0	**0**	0	**0**	**0**	**1**	**0**	**0**	**0**	**0**	0	0	**1**	**0**	**0**	**1**

Bits 15-14

CKS011	CKS010	Selection of operation clock (f_{MCK}) for channel 1
0	**0**	**Operation clock CKm0 set in timer clock selection register m (TPSm)**
0	1	Operation clock CKm2 set in timer clock selection register m (TPSm)
1	0	Operation clock CKm1 set in timer clock selection register m (TPSm)
1	1	Operation clock CKm3 set in timer clock selection register m (TPSm)

Bit 12

CCS01	Selection of channel 1 operation clock (f_{TCLK})
0	**Operation clock (f_{MCK}) set in bits CKS010 and CKS011**
1	Valid edge of input signal from TI01 pin

Bit 11

SPLIT01	Selection of 8 or 16-bit timer operation for channel 1
0	**Operates as 16-bit timer.**
1	Operates as 8-bit timer.

Bits 10-8

STS 012	STS 011	STS 010	Setting start or capture trigger of channel 1
0	0	0	Only software trigger start is valid (other trigger sources are unselected)
0	0	1	Valid edge of TI01 pin input is used as both the start trigger and capture trigger
0	1	0	Both edges of TI01 pin input are used as the start trigger and capture trigger
1	**0**	**0**	**Interrupt signal of master channel is used (when using slave channel with simultaneous channel operation function)**
Other than above			Setting prohibited

Note: Refer to the RL78/G13 User's Manual (Hardware version) for details on how to set registers.

Symbol: TMR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 011	CKS 010	0	CCS 01	SPLIT 01	STS 012	STS 011	STS 010	CIS 011	CIS 010	0	0	MD 013	MD 012	MD 011	MD 010
0	**0**	0	**0**	**0**	**1**	**0**	**0**	**0**	**0**	0	0	**1**	**0**	**0**	**1**

Bit 7-6

CIS 011	CIS 010	Selection of TI01 pin input valid edge
0	**0**	**Falling edge**
0	1	Rising edge
1	0	Both edges (when low-level width is measured)
1	1	Both edges (when high-level width is measured)

Bit 3-0

MD 013	MD 012	MD 011	MD 010	Operation mode of channel 1
0	**0**	**0**	0	Interval timer mode (Timer interrupt is not generated when counting is started).
			1	Interval timer mode (Timer interrupt is generated when counting is started）.
0	1	0	0	**Capture mode** **(Timer interrupt is not generated when counting is started).**
			1	Capture mode (Timer interrupt is generated when counting is started).
0	1	1	0	Event counter mode (Timer interrupt is not generated when counting is started).
1	**0**	**0**	0	One-count mode (Start trigger is invalid during counting operation).
			1	**One-count mode** **(Start trigger is valid during counting operation).**
1	1	0	0	Capture & one-count mode (Timer interrupt is not generated when counting is started Start trigger is invalid during counting operation).
Other than above				Setting prohibited

Note: Refer to the RL78/G13 User's Manual (Hardware version) for details on how to set registers.

Timer array unit 0 channel 2 initialization

- Timer mode register 02 (TMR02)

Selection of operation mode, Selection start trigger,
Selection of operation clock

Symbol: TMR02

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 021	CKS 020	0	CCS 02	MAST ER02	STS 022	STS 021	STS 020	CIS 021	CIS 020	0	0	MD 023	MD 022	MD 021	MD 020
0	**0**	0	**0**	**0**	**1**	**0**	**0**	**0**	**0**	0	0	**1**	**0**	**0**	**1**

Bits 15-14

CKS021	CKS020	Selection of operation clock (f_{MCK}) for channel 2
0	**0**	**Operation clock CKm0 set in timer clock selection register m (TPSm)**
0	1	Operation clock CKm2 set in timer clock selection register m (TPSm)
1	0	Operation clock CKm1 set in timer clock selection register m (TPSm)
1	1	Operation clock CKm3 set in timer clock selection register m (TPSm)

Bit 12

CCS02	Selection of channel 2 operation clock (f_{TCLK})
0	**Operation clock (f_{MCK}) set in bits CKS020 and CKS021**
1	Valid edge of input signal from TI02 pin

Bit 11

MASTER02	Selection between using channel 2 independently or simultaneously with another channel
0	**Operates in independent channel operation function or as slave channel in simultaneous channel operation function.**
1	Operates as master channel in simultaneous channel operation function.

Bits 10-8

STS 022	STS 021	STS 020	Setting start or capture trigger of channel 2
0	0	0	Only software trigger start is valid (other trigger sources are unselected)
0	0	1	Valid edge of TI02 pin input is used as both the start trigger and capture trigger
0	1	0	Both edges of TI02 pin input are used as the start trigger and capture trigger
1	**0**	**0**	**Interrupt signal of master channel is used (when using slave channel with simultaneous channel operation function)**
Other than above			Setting prohibited

Note: Refer to the RL78/G13 User's Manual (Hardware version) for details on how to set registers.

Symbol: TMR02

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 021	CKS 020	0	CCS 02	MAST ER02	STS 022	STS 021	STS 020	CIS 021	CIS 020	0	0	MD 023	MD 022	MD 021	MD 020
0	**0**	0	**0**	**0**	**1**	**0**	**0**	**0**	**0**	0	0	**1**	**0**	**0**	**1**

Bits 7-6

CIS 021	CIS 020	Selection of TI02 pin input valid edge
0	**0**	**Falling edge**
0	1	Rising edge
1	0	Both edges (when low-level width is measured)
1	1	Both edges (when high-level width is measured)

Bits 3-0

MD 023	MD 022	MD 021	MD 020	Operation mode of channel 2
0	0	0	0	Interval timer mode (Timer interrupt is not generated when counting is started).
			1	Interval timer mode (Timer interrupt is generated when counting is started）.
0	1	0	0	**Capture mode** **(Timer interrupt is not generated when counting is started).**
			1	Capture mode (Timer interrupt is generated when counting is started).
0	1	1	0	Event counter mode (Timer interrupt is not generated when counting is started).
1	**0**	**0**	0	One-count mode (Start trigger is invalid during counting operation).
			1	**One-count mode** **(Start trigger is valid during counting operation).**
1	1	0	0	Capture & one-count mode (Timer interrupt is not generated when counting is started Start trigger is invalid during counting operation).
Other than above				Setting prohibited

Note: Refer to the RL78/G13 User's Manual (Hardware version) for details on how to set registers.

Timer array unit 0 channel 3 initialization

- Timer mode register 03 (TMR03)

Selection of operation mode, Selection start trigger,
Selection of operation clock

Symbol: TMR03

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 031	CKS 030	0	CCS 03	SPLIT 03	STS 032	STS 031	STS 030	CIS 031	CIS 030	0	0	MD 033	MD 032	MD 031	MD 030
0	**0**	0	**0**	**0**	**1**	**0**	**0**	**0**	**0**	0	0	**1**	**0**	**0**	**1**

Bits 15-14

CKS031	CKS030	Selection of operation clock (f_{MCK}) for channel 3
0	**0**	**Operation clock CKm0 set in timer clock selection register m (TPSm)**
0	1	Operation clock CKm2 set in timer clock selection register m (TPSm)
1	0	Operation clock CKm1 set in timer clock selection register m (TPSm)
1	1	Operation clock CKm3 set in timer clock selection register m (TPSm)

Bit 12

CCS03	Selection of channel 3 operation clock (f_{TCLK})
0	**Operation clock (f_{MCK}) set in bits CKS030 and CKS031**
1	Valid edge of input signal from TI03 pin

Bit 11

SPLIT03	Selection of 8 or 16-bit timer operation for channel 3
0	**Operates as 16-bit timer.**
1	Operates as 8-bit timer.

Bits 10-8

STS 032	STS 031	STS 030	Setting start or capture trigger of channel 3
0	0	0	Only software trigger start is valid (other trigger sources are unselected)
0	0	1	Valid edge of TI03 pin input is used as both the start trigger and capture trigger
0	1	0	Both edges of TI03 pin input are used as the start trigger and capture trigger
1	**0**	**0**	**Interrupt signal of master channel is used (when using slave channel with simultaneous channel operation function)**
Other than above			Setting prohibited

Note: Refer to the RL78/G13 User's Manual (Hardware version) for details on how to set registers.

Symbol: TMR03

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 031	CKS 030	0	CCS 03	SPLIT 03	STS 032	STS 031	STS 030	CIS 031	CIS 030	0	0	MD 033	MD 032	MD 031	MD 030
0	**0**	0	**0**	**0**	**1**	**0**	**0**	**0**	**0**	0	0	**1**	**0**	**0**	**1**

Bits 7-6

CIS 031	CIS 030	Selection of TI03 pin input valid edge
0	**0**	**Falling edge**
0	1	Rising edge
1	0	Both edges (when low-level width is measured)
1	1	Both edges (when high-level width is measured)

Bits 3-0

MD 033	MD 032	MD 031	MD 030	Operation mode of channel 3
0	0	0	0	Interval timer mode (Timer interrupt is not generated when counting is started).
			1	Interval timer mode (Timer interrupt is generated when counting is started）.
0	1	0	0	Capture mode (Timer interrupt is not generated when counting is started).
			1	Capture mode (Timer interrupt is generated when counting is started).
0	1	1	0	Event counter mode (Timer interrupt is not generated when counting is started).
1	**0**	**0**	0	One-count mode (Start trigger is invalid during counting operation).
			1	**One-count mode** **(Start trigger is valid during counting operation).**
1	1	0	0	Capture & one-count mode (Timer interrupt is not generated when counting is started Start trigger is invalid during counting operation).
Other than above				Setting prohibited

Note: Refer to the RL78/G13 User's Manual (Hardware version) for details on how to set registers.

Setting up the timer output mode

- Timer output mode register 0 (TOM0)

Set up the timer output mode for each channel

Symbol: TOM0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	TOM07	TOM06	TOM05	TOM04	TOM03	TOM02	TOM01	0
0	0	0	0	0	0	0	0	x	x	x	x	**1**	**1**	**1**	0

Bits 3-1

TOM0n	Channel n timer output mode control
0	Master channel output mode. (Output is toggled with the timer interrupt request signal (INTTM0n))
1	**Slave channel output mode. (Output is set with the master channel's timer interrupt request signal (INTTM0n) and reset with the slave channel's timer interrupt request signal (INTTM0p).)**

Configuring the output level for the timer output pin

- Timer output level register 0 (TOL0)

Configure the output pin for each channel.

Symbol: TOL0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	TOL07	TOL06	TOL05	TOL04	TOL03	TOL02	TOL01	0
0	0	0	0	0	0	0	0	x	x	x	x	**1**	**1**	**1**	0

Bits 3-1

TOL0n	Channel n timer output level control
0	Positive logic output (active-high)
1	**Negative logic output (active-low)**

Note: Refer to the RL78/G13 User's Manual (Hardware version) for details on how to set registers.

Configuring the output value for the timer output pin

- Timer output register 0 (TO0)

Configure the output value for the timer output pin for each channel.

Symbol: TO0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	TO07	TO06	TO05	TO04	TO03	TO02	TO01	TO00
0	0	0	0	0	0	0	0	x	x	x	x	**1**	**1**	**1**	x

Bits 3-1

TO0n	Channel n timer output
0	Timer output value is 0
1	**Timer output value is 1**

Enabling the timer output

- Timer output enable register 0 (TOE0)

Enable/disable the timer output for each channel.

Symbol: TOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	TOE 07	TOE 06	TOE 05	TOE 04	TOE 03	TOE 02	TOE 01	TOE 00
0	0	0	0	0	0	0	0	x	x	x	x	**1**	**1**	**1**	x

Bits 3-1

TOE0n	Timer output enable/disable of channel n
0	The TO0n operation stopped by count operation (timer channel output bit). Writing to the TO0n bit is enabled. The TO0n pin functions as data output, and it outputs the level set to the TO0n bit. The output level of the TO0n pin can be manipulated be software.
1	**The TO0n operation enabled by count operation (timer channel output bit).** **Writing to the TO0n bit is disabled (writing is ignored).** **The TO0n pin functions as timer output, and the TOE0n bit is set or reset depending on the timer operation.** **The TO0n pin outputs the square-wave or PWM depending on the timer operation.**

Note: Refer to the RL78/G13 User's Manual (Hardware version) for details on how to set registers.

5.7.7 Main Processing

Figure 5.9 shows the flowchart of the main processing.

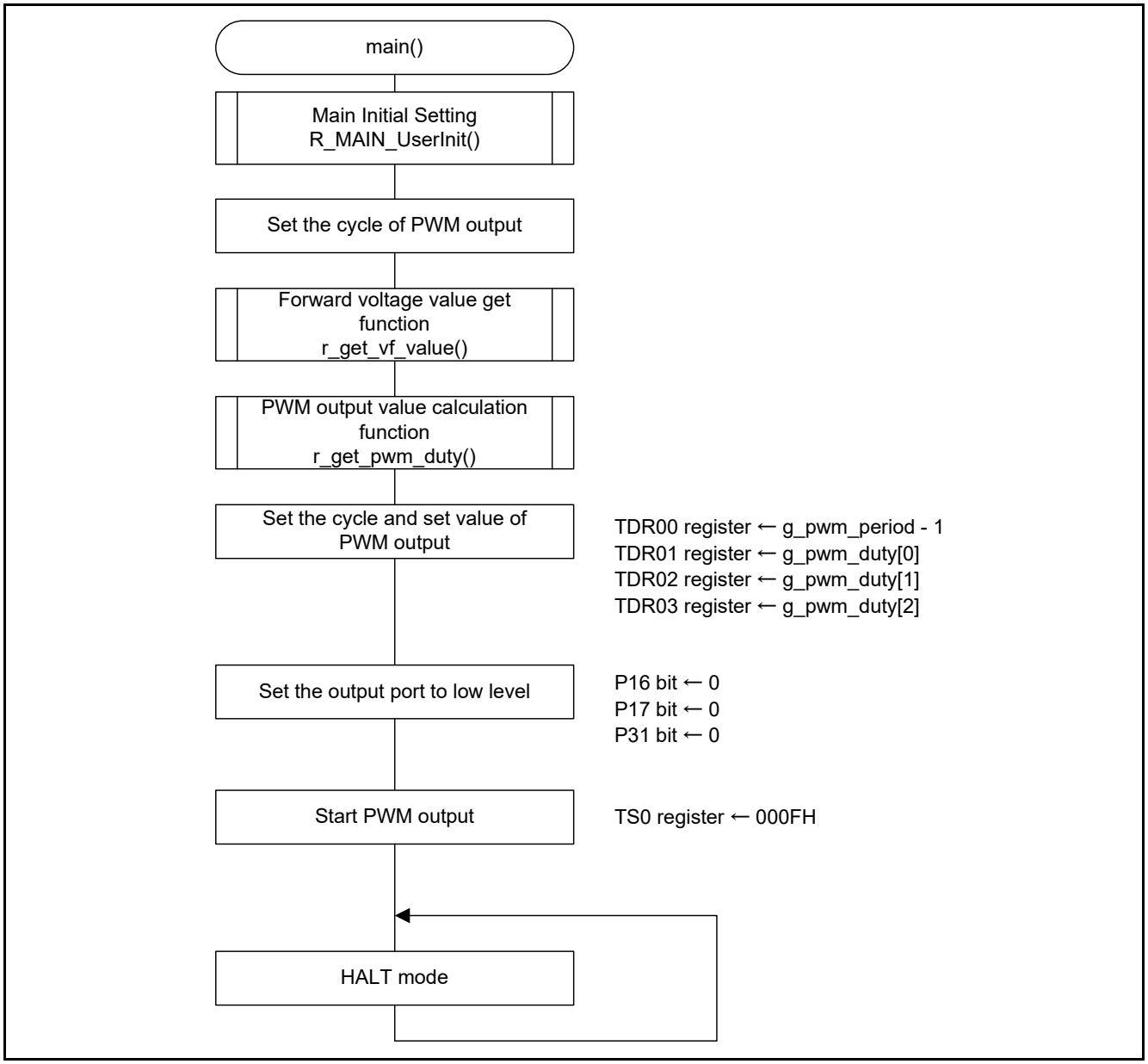

Figure 5.9 Main Processing

5.7.8 Main Initial Setting

Figure 5.10 shows the flowchart of the main initial setting.

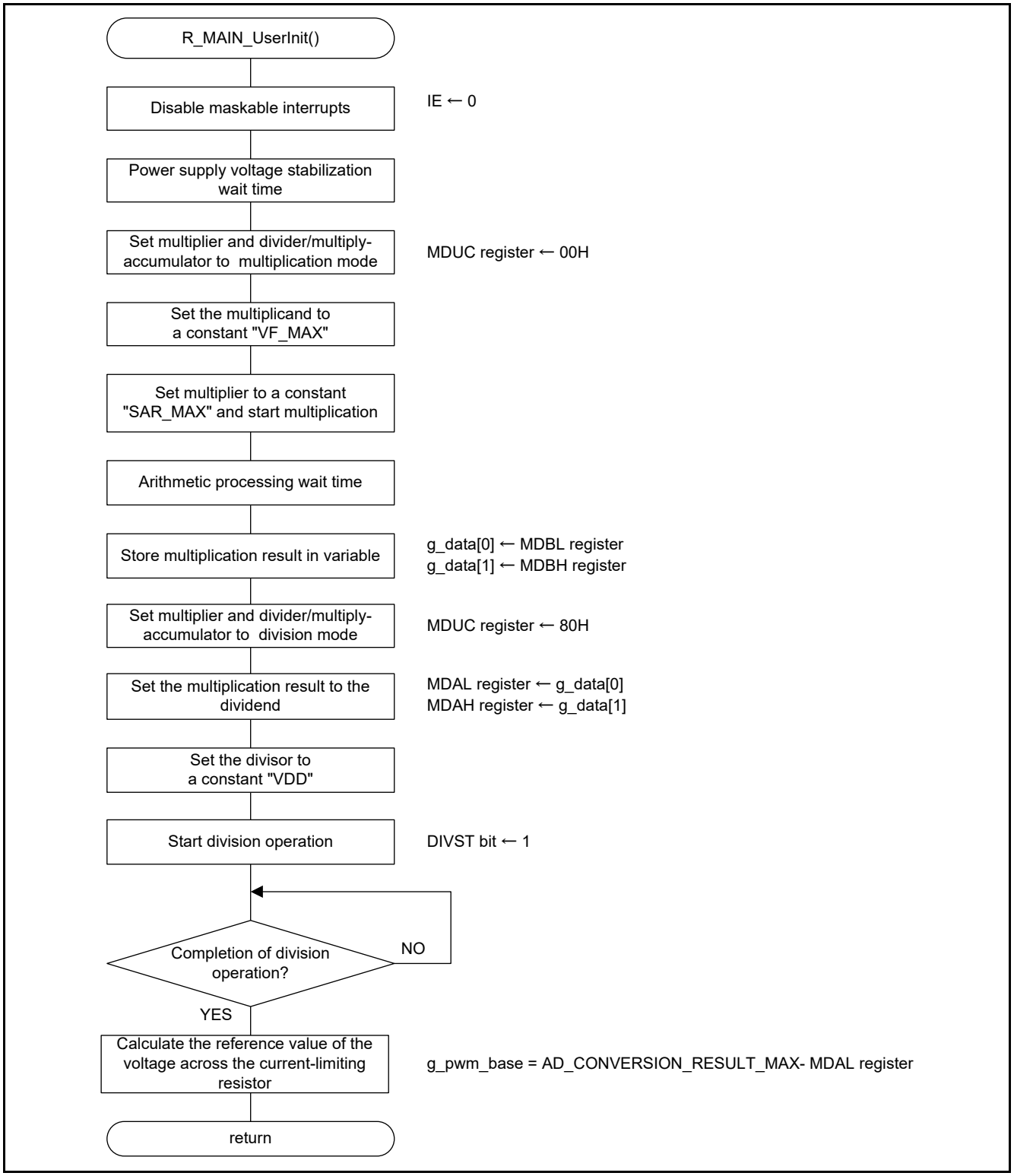

Figure 5.10 Main Initial Setting

5.7.9 Forward Voltage Value Get Function

Figure 5.11 shows the flowchart of the forward voltage value get function.

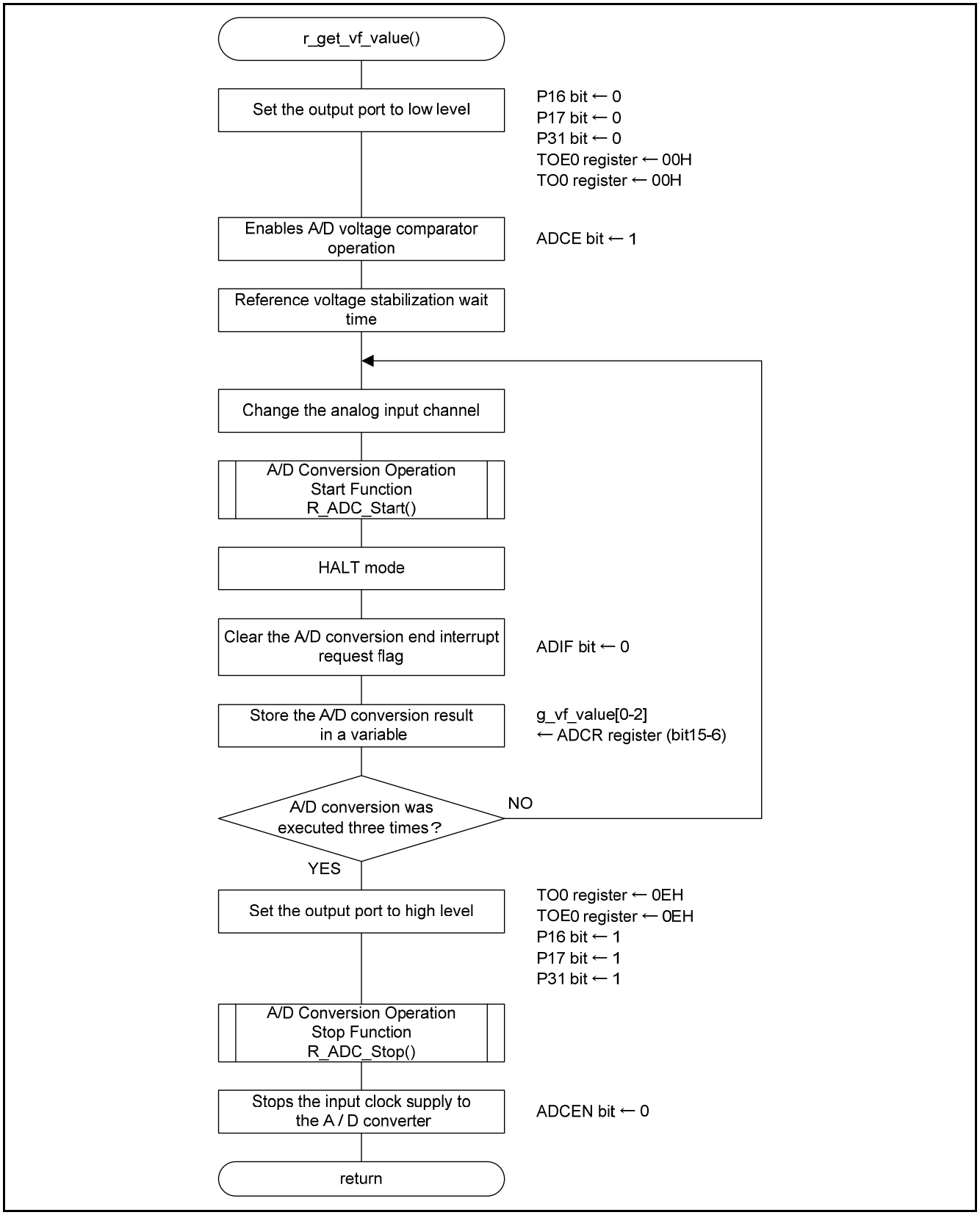

Figure 5.11 Forward Voltage Value Get Function

5.7.10 A/D Conversion Operation Start Function

Figure 5.12 shows the flowchart of the A/D conversion operation start function.

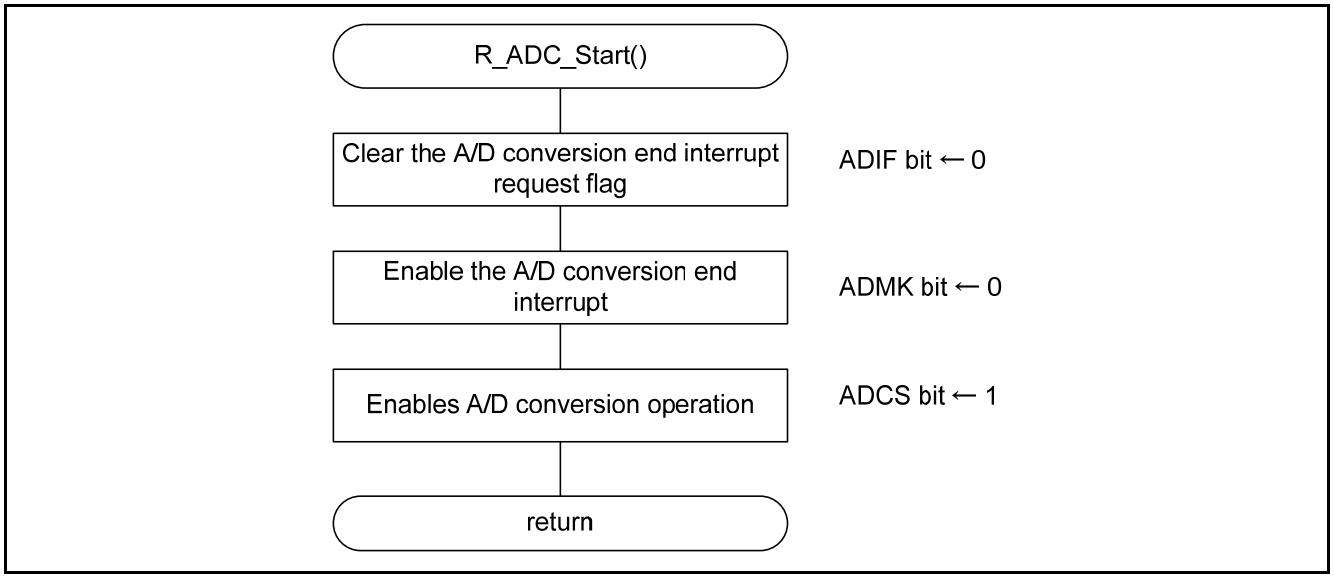

Figure 5.12 A/D Conversion Operation Start Function

5.7.11 A/D Conversion Operation Stop Function

Figure 5.13 shows the flowchart of the A/D conversion operation stop function.

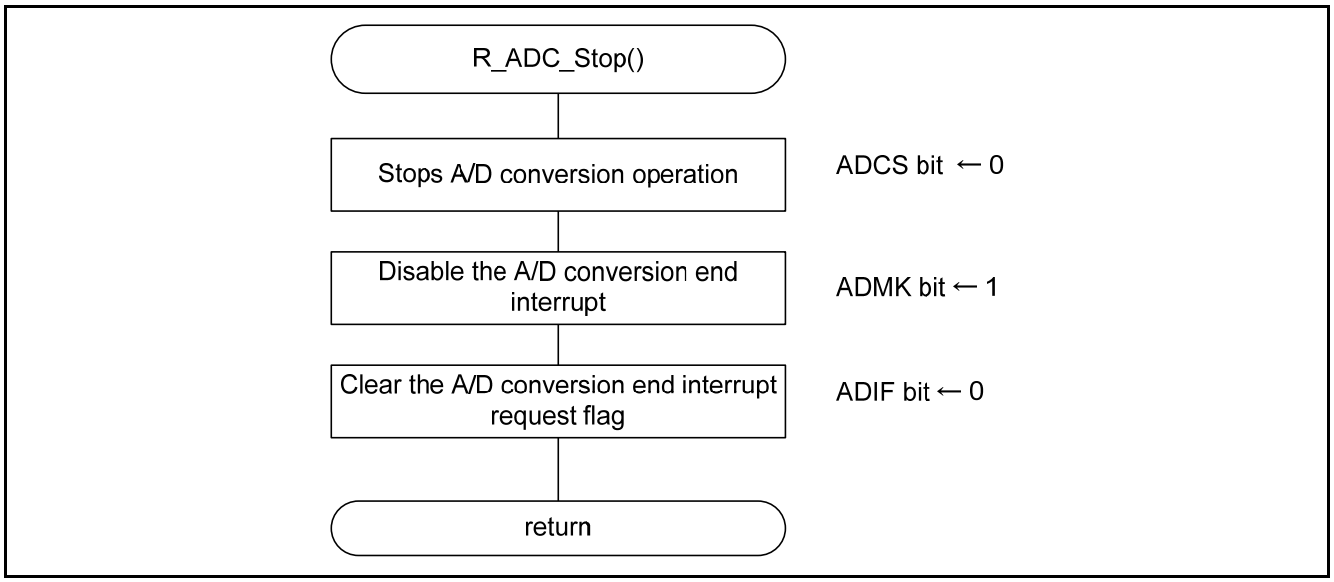

Figure 5.13 A/D Conversion Operation Stop Function

5.7.12 PWM Output Value Calculation Function

Figure 5.14 shows the flowchart of the PWM output value calculation function.

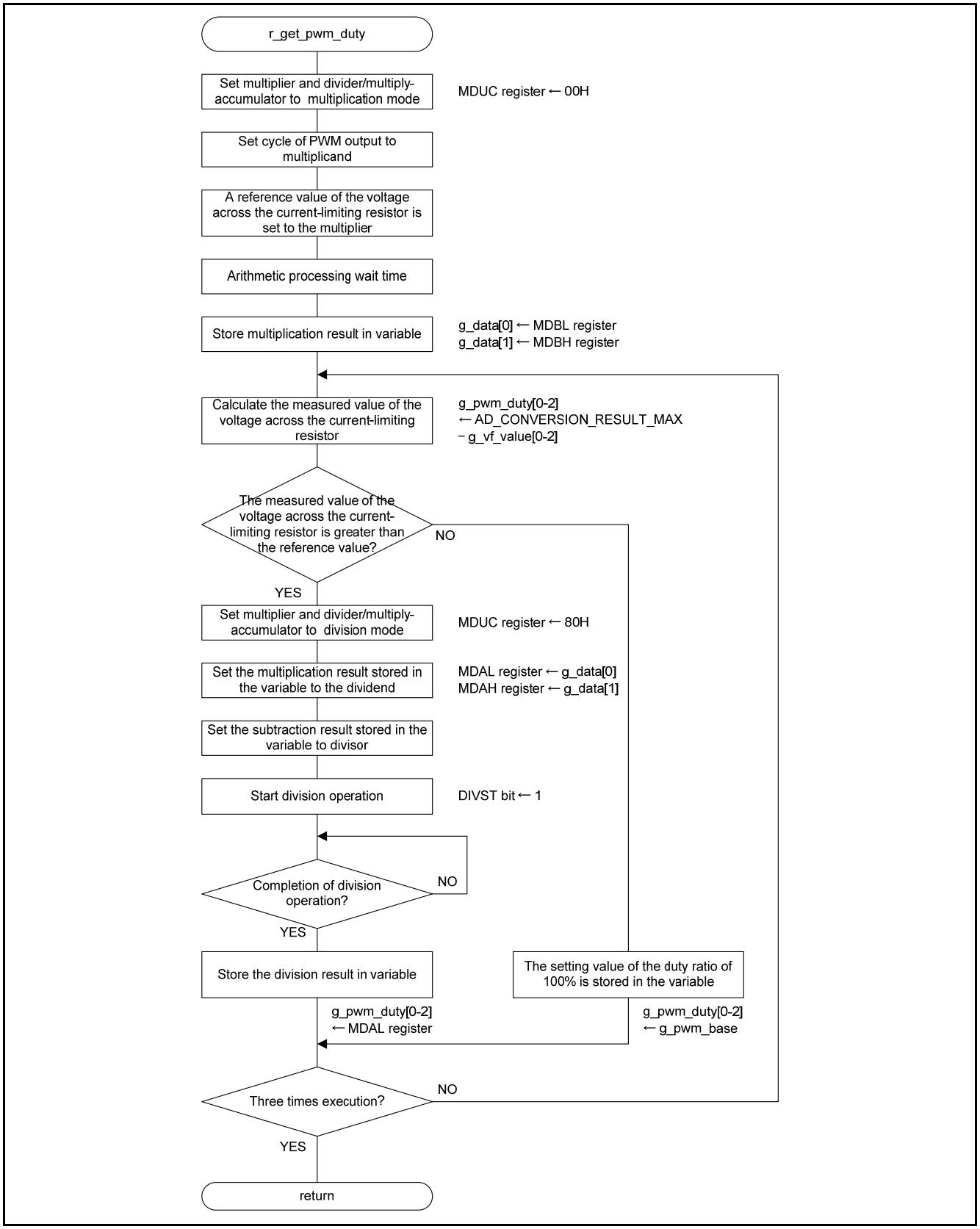

Figure 5.14 PWM Output Value Calculation Function

6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents

RL78/G13 User's Manual: Hardware (R01UH0146E)
RL78 Family User's Manual: Software (R01US0015E)
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can downloaded from the Renesas Electronics website.

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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Jun. 22, 2018	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   ¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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