Renesas Synergy™ S7G2

BACnet® Demo Kit (SK-S7G2) User Guide

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Introduction

This User Guide describes about the Renesas BACnet® Demo Kit. In this Renesas BACnet® solution, Renesas Synergy™ S7 Microcontroller Group is the highlighted Components. Using this BACnet® Demo Kit, developers can easily start to evaluate on Renesas Building Automation solution, using SK-S7G2 starter kit for advance control the edge building devices like thermostat via this unique communication.

Target Device

R7FS7G27H3CFC

Contents

1. Overview

The BACnet® uses the Synergy™ S7G2 MCU has inherent features to support a Graphical User Interface (GUI). In particular, it has a very large 4 MB on-chip flash memory in combination with 640 KB of on-chip SRAM, where the internal SRAM can host graphic frame buffers for the QVGA display panel. It has two LEDs indicators, two toggle switches for input, two potentiometers for analog input, and two temperature sensors. The demo can support both BACnet® IP option and MS/TP option. To evaluate the BACnet® MS/TP option, it is needed one Ethernet to RS-485 convertor to bridge between PC Ethernet and BACnet® MS/TP port.

For setting up the BACnet® system and testing demo, refer to the "BACnet® Demo Kit (SK-S7G2) Quick Start Guide" application note document (R01QS0012EU0100).

https://www.renesas.com/en-us/docs/solutions/lighting/r01qs0012eu0100-synergy-sk-s7g2.pdf

Figure 1 shows top view of the BACnet® Suitcase.

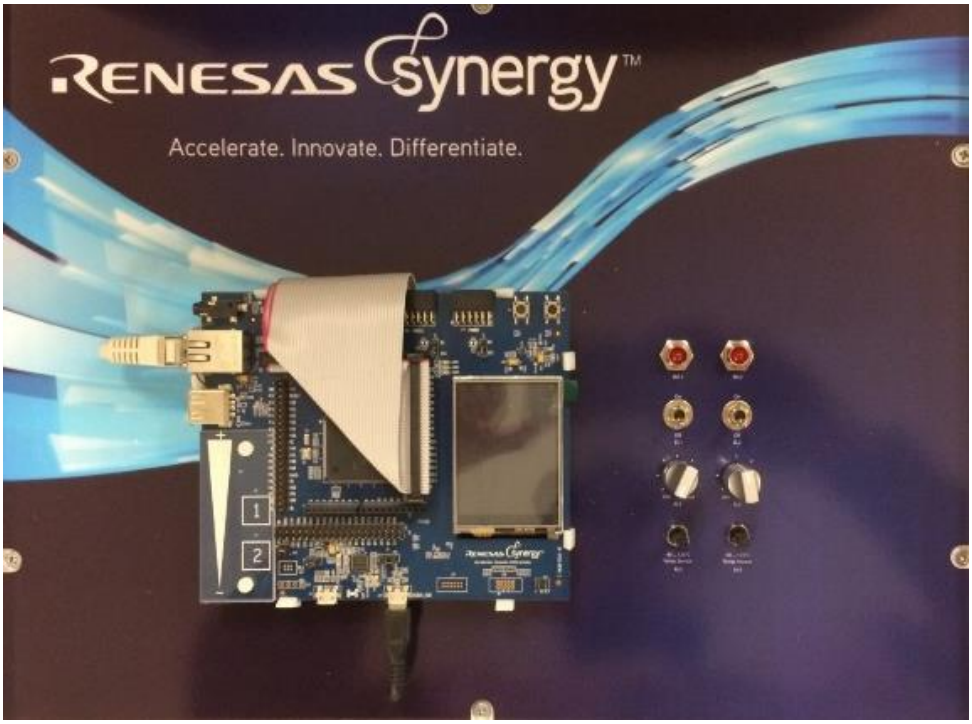


Figure 1 BACnet® Demo Board

2. BACnet® Demo System

BACnet® is an acronym that stands for "Building Automation and Control networking protocol" so it is data communication protocol and a set of rules for Building Automation. Renesas and its third-party CS Lab develop a BACnet® software solution to easily evaluate the system level using Synergy™ SK-S7G2 starter kit hardware. For embedded firmware development, you can develop with Renesas Synergy™ SSP and BACnet® object libraries. Basically, two projects are included in e2 studio project workspace and they are Data layer of IP for interfacing via Ethernet and Data Layer of MS/TP for RS-485 interface. Thus, each application has read and write access through BACnet® Synergy™ Wrapper layer to Synergy™ SSP Stack like HAL/Common layer and Network Thread. Figure 2 shows the BACnet® Demo System Block diagram including BACnet® libraries.

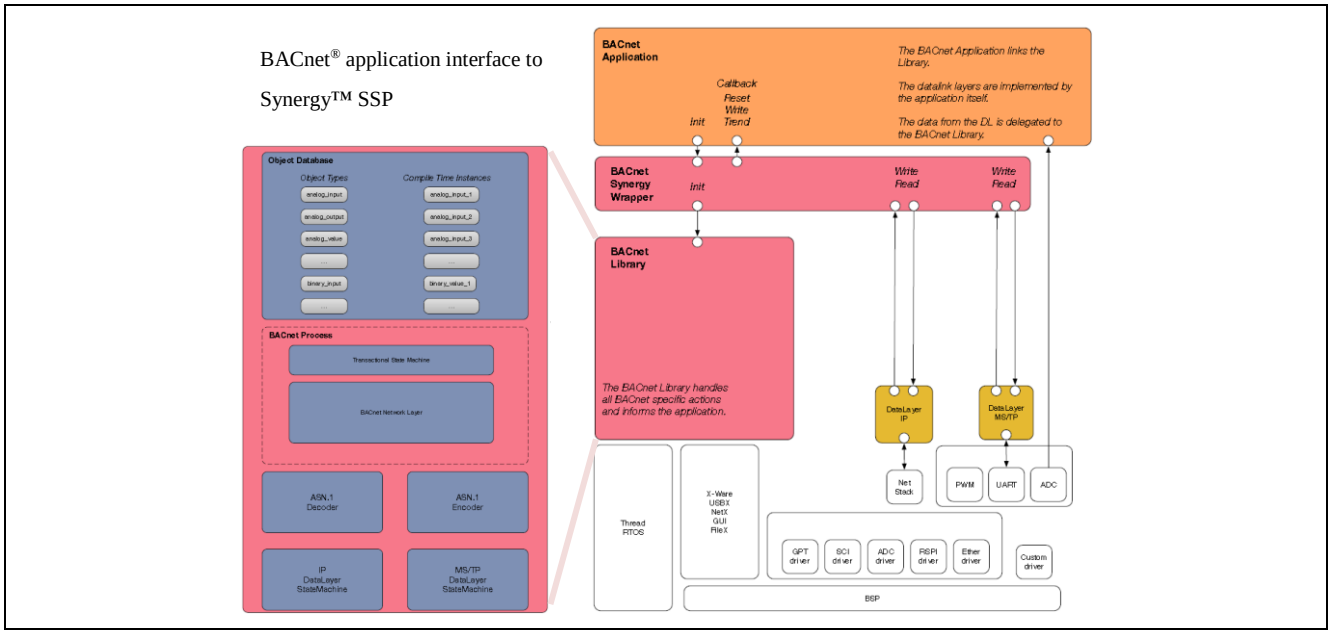


Figure 2 BACnet® System Block diagram

2.1 BACnet® Demo Software Architecture

This BACnet® Demo application creates a BACnet® device with objects such as device object, binary input object, binary output object, analog input object, analog output object, scheduler object with entries, trend log object that connected to potentiometer, calendar object for scheduler, notification class object for alarm. Using the macro definition "BACNET_DATA_LINK_MSTP", you can switch between Data layer of IP and Data Layer of MS/TP application. The demo will start running through from "BacnetDemoMain" which includes "BACnet common", "data link layer", and "User's Application" for initialization and start.

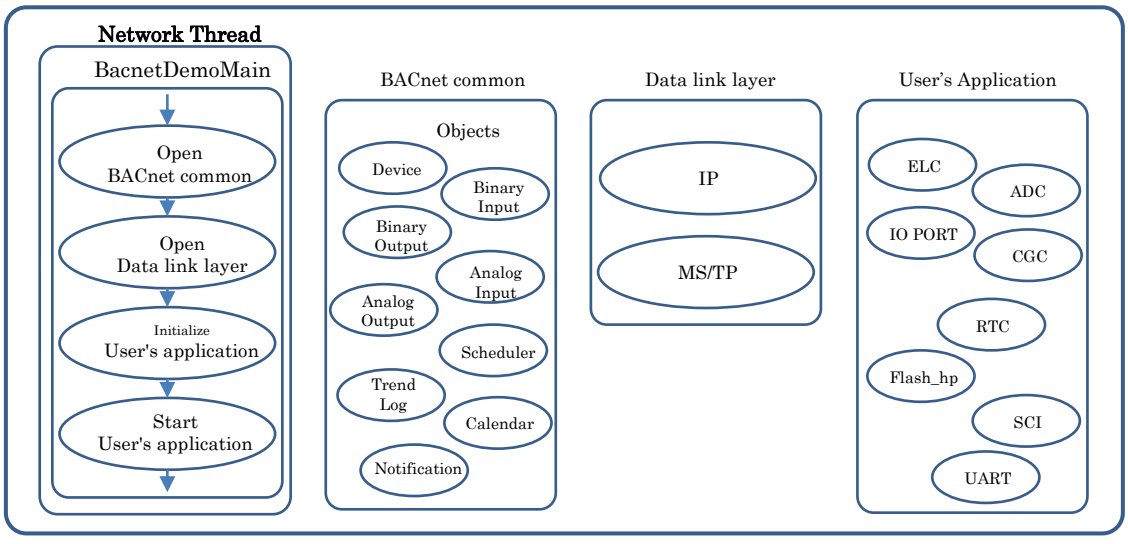


Figure 3 BACnet® Demo Software Architecture Block diagram

2.2 Programming and Debugging

This BACnet® Demo uses a SEGGER J-Link On-Board debugger for S7G2 device through J19 USB connector. For ease of usage, this SK-S7G2 Starter Kit J19 USB connector is extended to suitcase with USB Female type B connector.

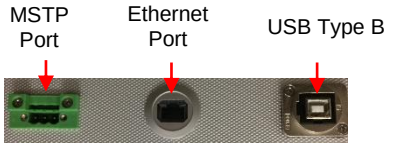


Figure 4 BACnet® Demo Suitcase Connection

Debug Requirement

- Integrated Development Environment : e2 studio Version 5.0.0.043
- Compiler : GCC arm® Embedded 4.9 2015q3
- Software Package : Renesas Synergy™ Software Package (SSP) 1.1.0
- Workspace : BACnet® demo of Renesas Synergy™ Gallery

I/O assignment in the BACnet® Demo project

- Net Address : 192.168.0.111 (Port 47808)
- UART : Channel 3
  - Baud rate : 9600
  - Bit : 8
  - Parity : none
  - Stop Bit : 1
- ADC : Channel 0, 1, 3, 4
  - Channel 0 : Potentiometer 1
  - Channel 1 : Potentiometer 2
  - Channel 3 : Temperature Sensor 1
  - Channel 4 : Temperature Sensor 2
- Input :
  - Port 0 pin5 : Switch 1
  - Port 0 pin6 : Switch 2
- Output :
  - Port 6 pin 0 : LED 1
  - Port 6 pin 1 : LED 2

BACnet® Object Memory Usage

BACnet® Object	RAM (byte)	ROM (byte)
Device (DEV)	113	1413
Binary Input (BI)	53	942
Binary Output (BO)	11	484
Analog Input (AI)	70	1008
Analog Output (AO)	83	1040
Calendar (CA)	3	226
Notification (NC)	18	290
Scheduler (SC)	59	482
Trend Log (TR)	149	1170

3. Building Sample Project

3.1 Renesas Synergy™ S7G2 Firmware

Renesas standard starter kit with Synergy™ microcontroller S7 device is used to evaluate the BACnet® network. Thus, the board can be used as development platform as well. When using this SK-S7G2 starter kit, it was modified to suite the BACnet® MSTP interface and added two LED indicators, two trimer ports, two switches, and two temperature sensors for BACnet objects. For debugging to the BACnet® firmware, you can use onboard build-in JTAG debugger via USB (J19) connector or use extended USB connector form the suitcase. For using S7 programmer/debugger tool and detail project development, refer Renesas website.
(Note: SEGGER J-Link download link: https://www.segger.com/downloads/jlink)

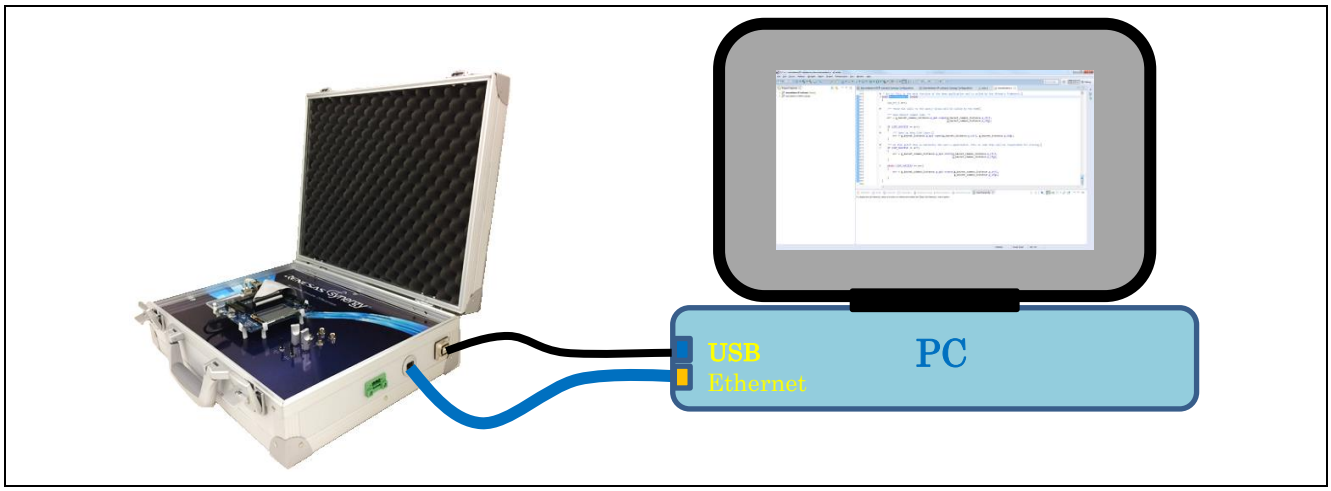


Figure 5 Synergy™ S7G2 Hardware Programming/Debugging setting

In order to build and debug the BACnet® demo firmware, you need e2 Studio version 5.3 or later and Synergy™ SSP package version 1.1.0. To begin debugging, import the project from the following folder.

\..\ BACnet_Demo\ Synergy_project.

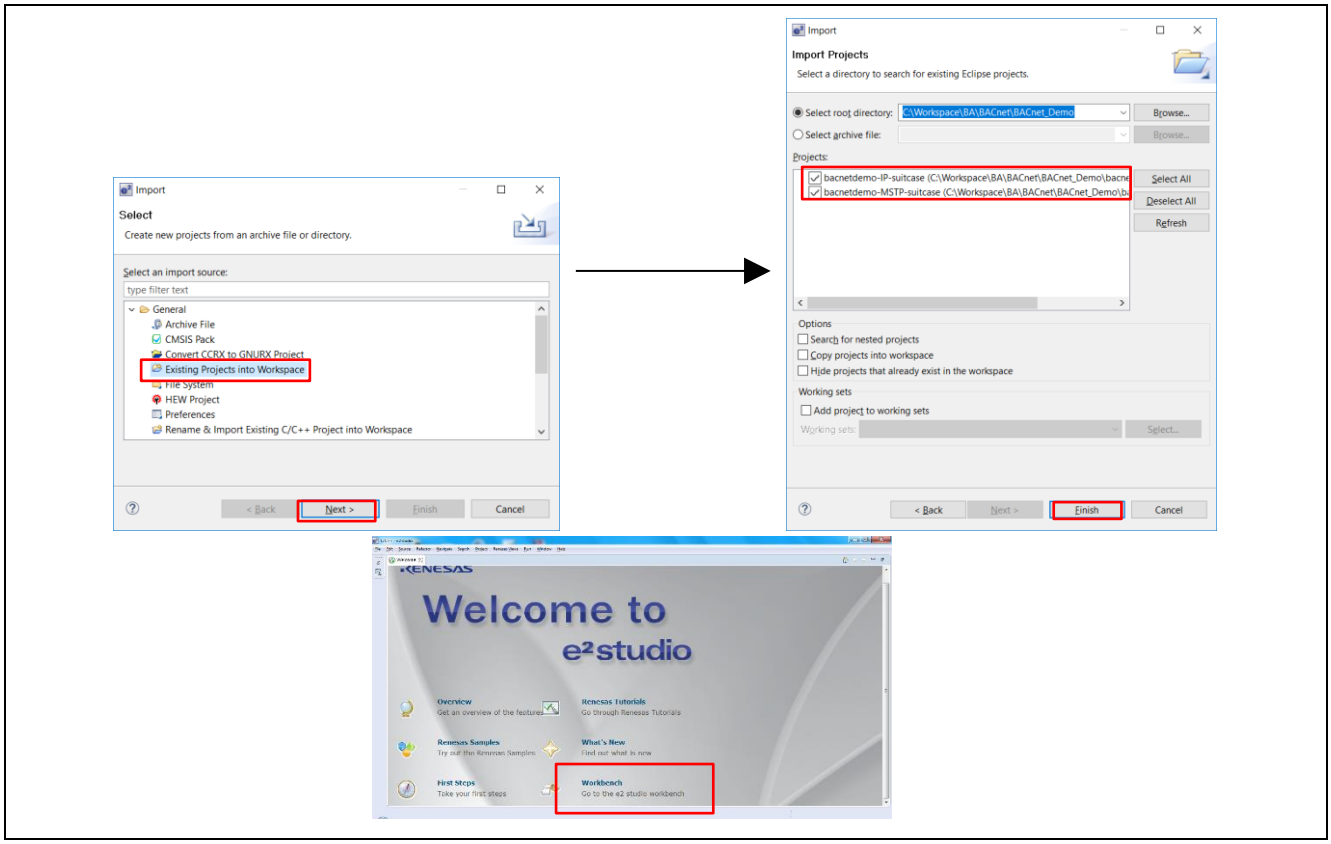


Figure 6 e2 studio Workspace Environment Import Projects

3.2 Importing the Synergy™ Project in e2 Studio Workspace

To import the project into e2 studio workspace, following the below step 1 to 6.

1. First, launch the e² studio workspace.
2. Select **Import** from the File pulldown menu.
3. Select **Existing Projects into Workspace** from General, and click **Next**.
4. Browse the projects folder (root directory), select the projects, and click **Finish**.
5. Clicking **Workbench** in the Welcome screen opens the Workspace (see Figure 7)
6. selects **Build All** (to build all the projects in the Workspace) from Project pulldown menu.

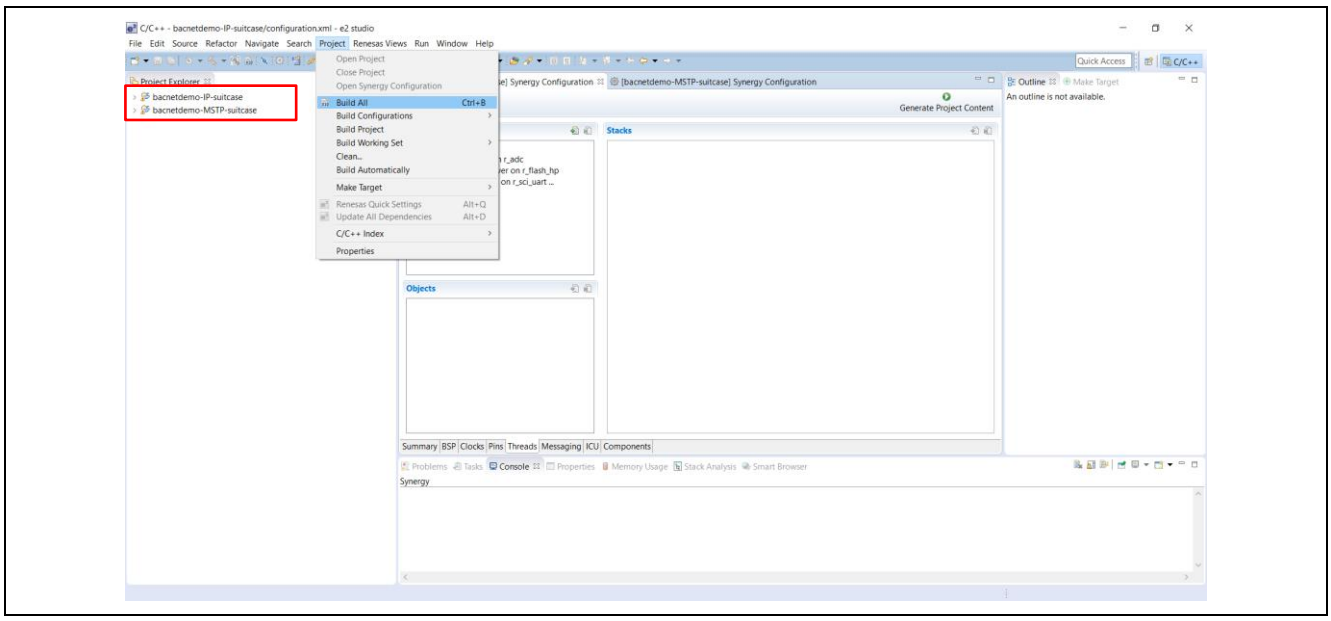


Figure 7 e2 studio Workspace Environment

3.3 Debugging the Synergy™ Project in e2 Studio Workspace

To enable JTAG debug function on the SK-S7G2 board, do the following steps (see Figure 8).

1. Attach the micro USB cable to Demo suitcase USB connector and PC USB port.

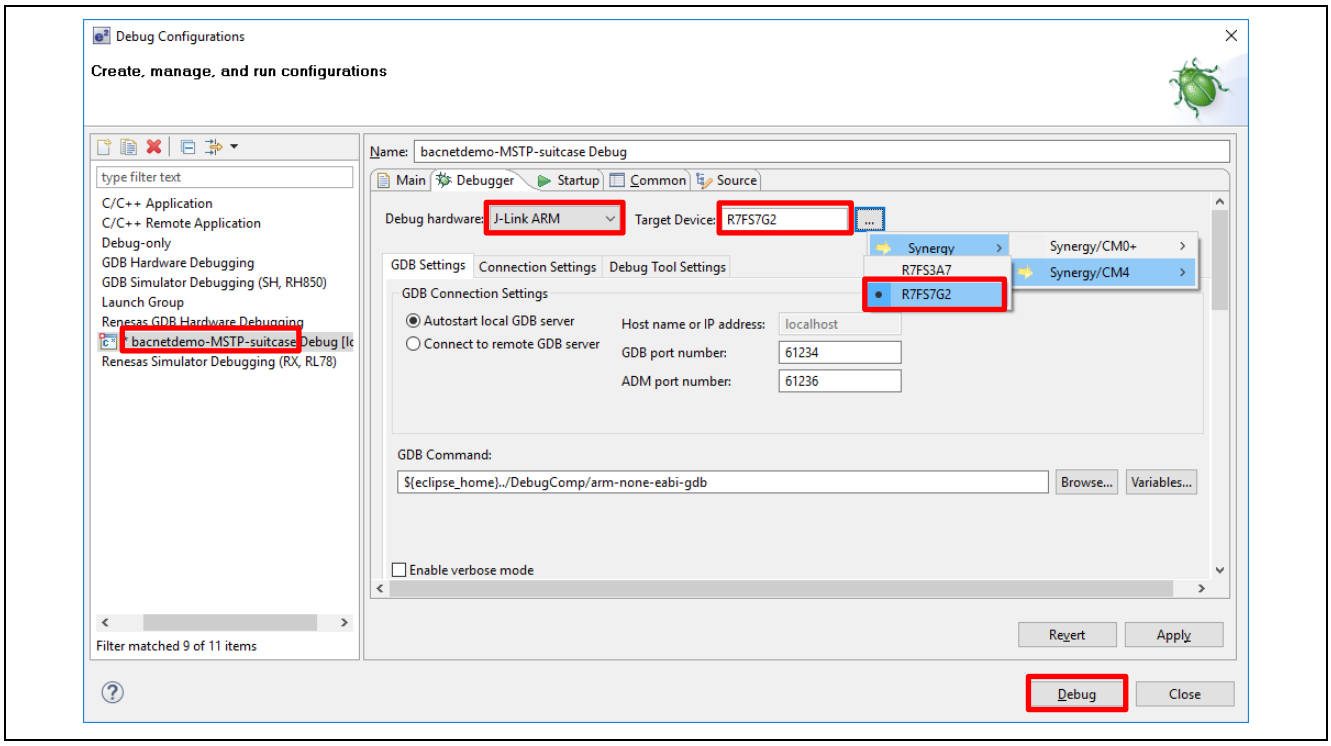


Figure 8 e2 studio Workspace Debugging Setup

2. Set the Debug configuration by selecting a project to debug if not in debug mode.
3. Figure 8 shows the Debug Configuration window.
4. Select Debug Configuration from the Run pulldown menu.
5. Right-click Renesas GDB hardware Debugging.
6. Select New from the options menu to create a new debug launch.
7. Select the **Debugger** tab.
8. Select **J-Link arm®** for debug hardware and **R7FS7G2** for Target Device.
9. Click **Debug** to start debugging.
   Figure 9 shows the Debug window. Click **Resume** (F8) to run the program in Debug mode.

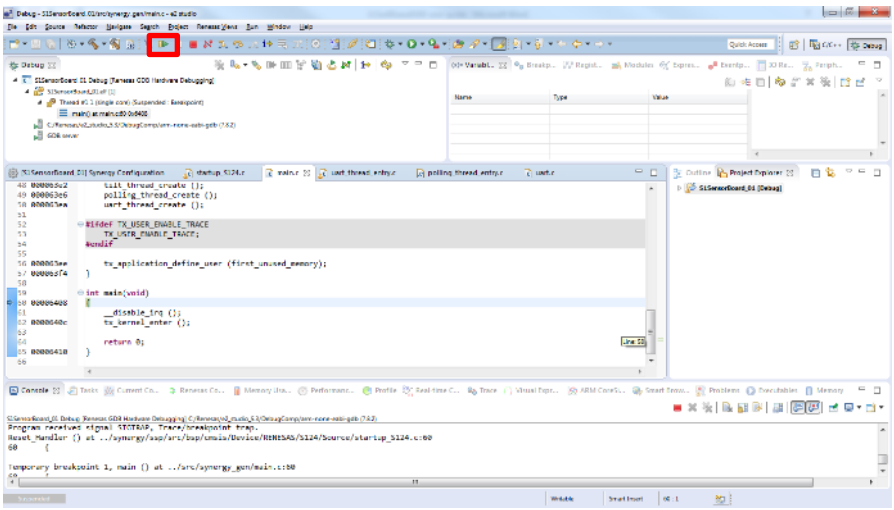
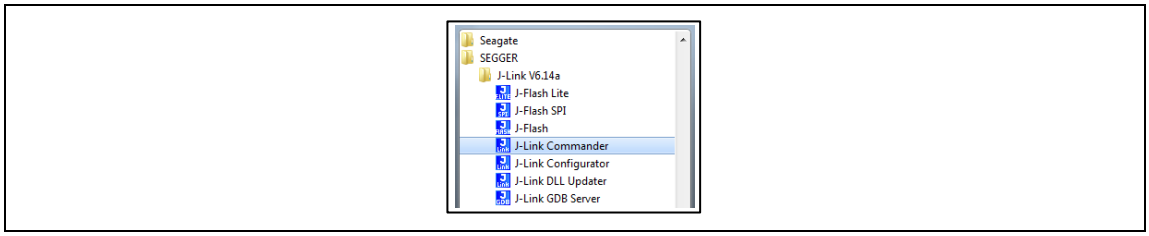


Figure 9 e2 studio workspace in debugging mode for Synergy™ S7G2

4. Programming to SK-S7G2 Starter Kit

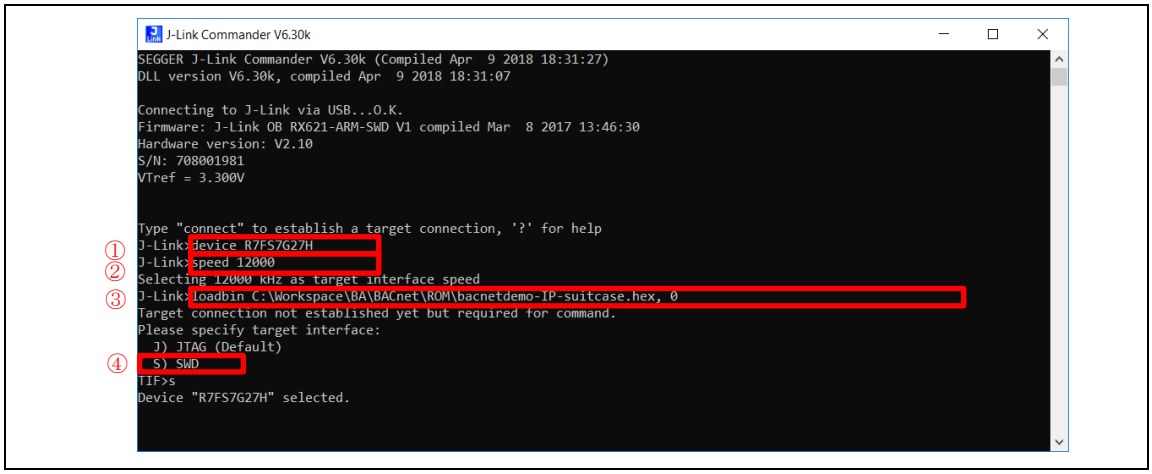
Step 1. Attach the USB cable between the Demo suitcase unit and PC via micro USB cable.

Step 2. Open J-Link Commander from Start menu in All Programs, SEGGER folder.



Step 3. Enter the below commands to program target device.

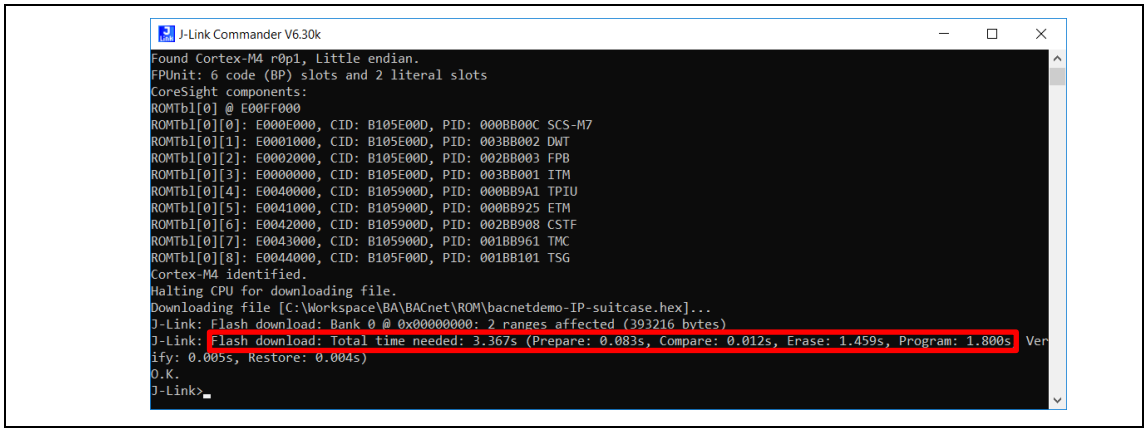
1. Device R7FS7G27H
2. Speed 12000
3. loadbin C:\...\ROM_File\file_name.hex, 0
4. S



Step 4. Note: This Demo Kit includes following Hex files for respective demonstration

a. BACnet® IP demo : bacnetdemo-IP-suitcase.hex

b. BACnet® MSTP demo : bacnetdemo-MSTP-suitcase.hex

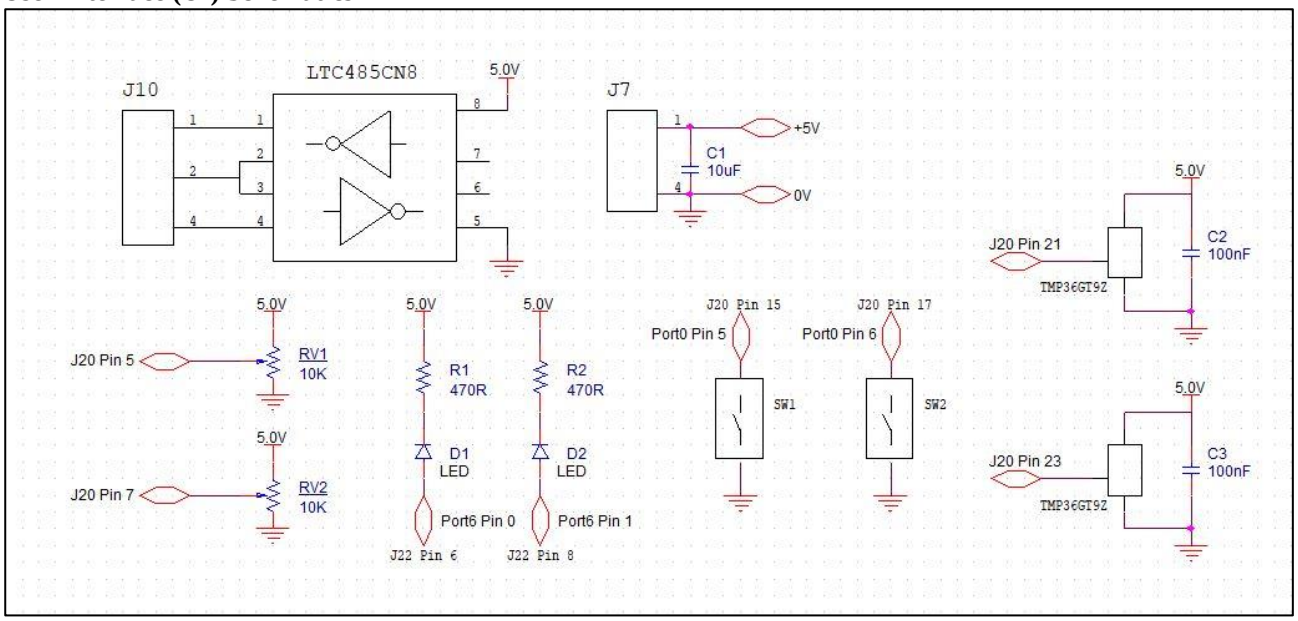


Step 5. After programming, disconnect the board from the PC to evaluate.

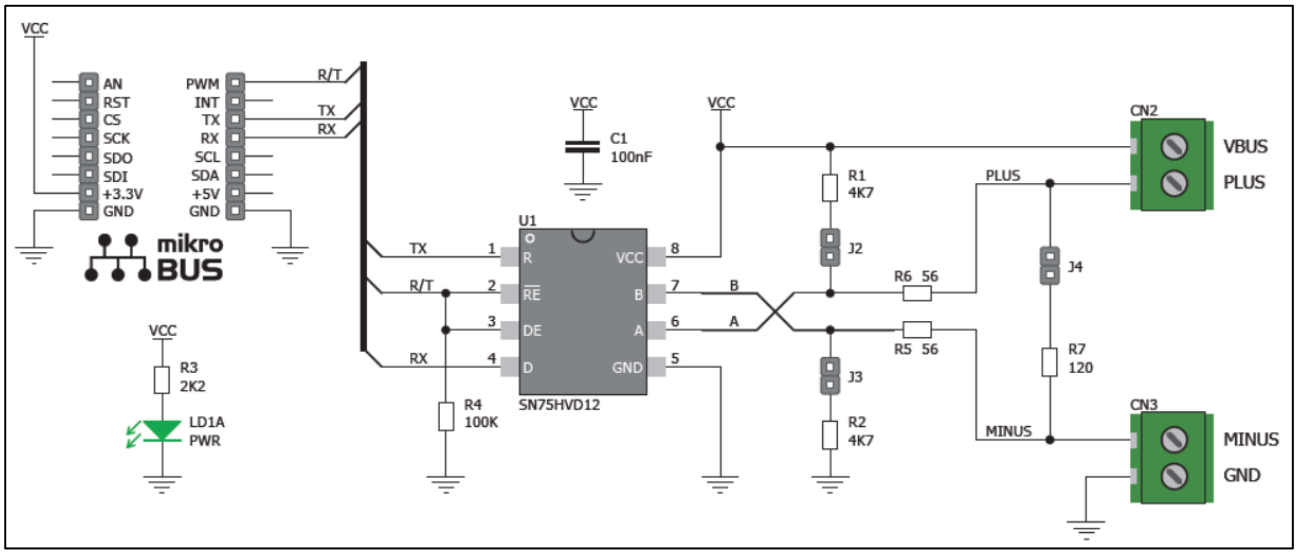
5. Circuit Diagram

This section shows the BACnet® Demo kit wiring diagram.

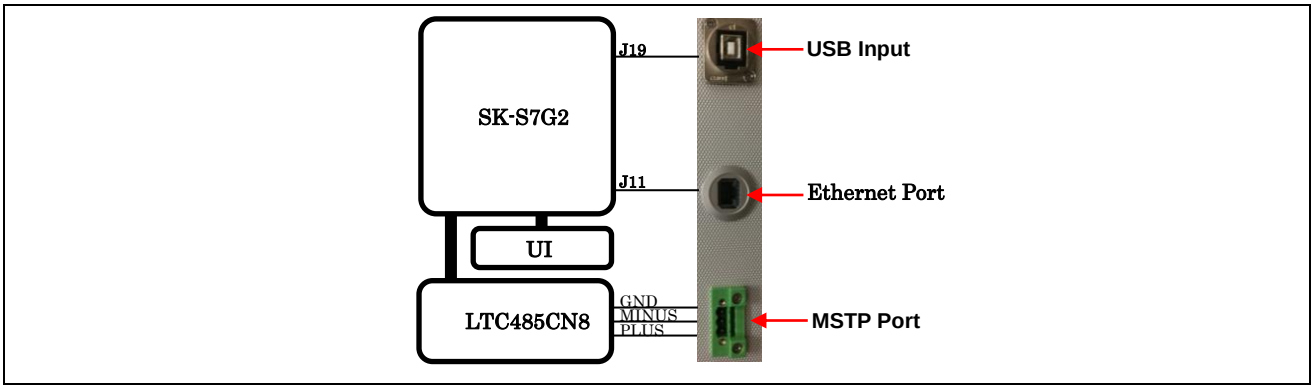
User Interface (UI) Schematics



LTC485CN8 Schematics



BACnet Suitcase wiring diagram



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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Jun 15, 2018	–	Initial Release

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1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

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(Rev.4.0-1 November 2017)

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