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April 1st, 2010
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R8C/35C Group

A/D Converter in Single Sweep Mode

1. Abstract

This document describes the setting method and an application example for inputting an analog voltage by A/D converter (single sweep mode) on R8C/35C Group.

2. Introduction

The application example described in this document applies to the following MCU and parameters.

- MCU : R8C/35C Group
- VCC/AVCC, VREF : 5 V

The sample program in this application note can be used with other R8C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using this application note.

3. Application Example

3.1 Program Outline

Perform A/D conversion on the analog voltage which is input from the analog input pins (two pins).

Main settings

- Select P0_6/AN1 pin and P0_7/AN0 pin for analog input
- Select single sweep mode as the A/D operating mode
- Select f1 as the clock source of fAD
- Select fAD divided-by-2 as the ϕAD operation clock
- Select 10 bits resolution
- Select a software trigger as the A/D conversion start condition
- Disable the A/D open-circuit detection assist function

Figure 3.1 shows the block diagram, and Figure 3.2 shows the operation in single sweep mode. Table 3.1 lists the pins used and their functions.

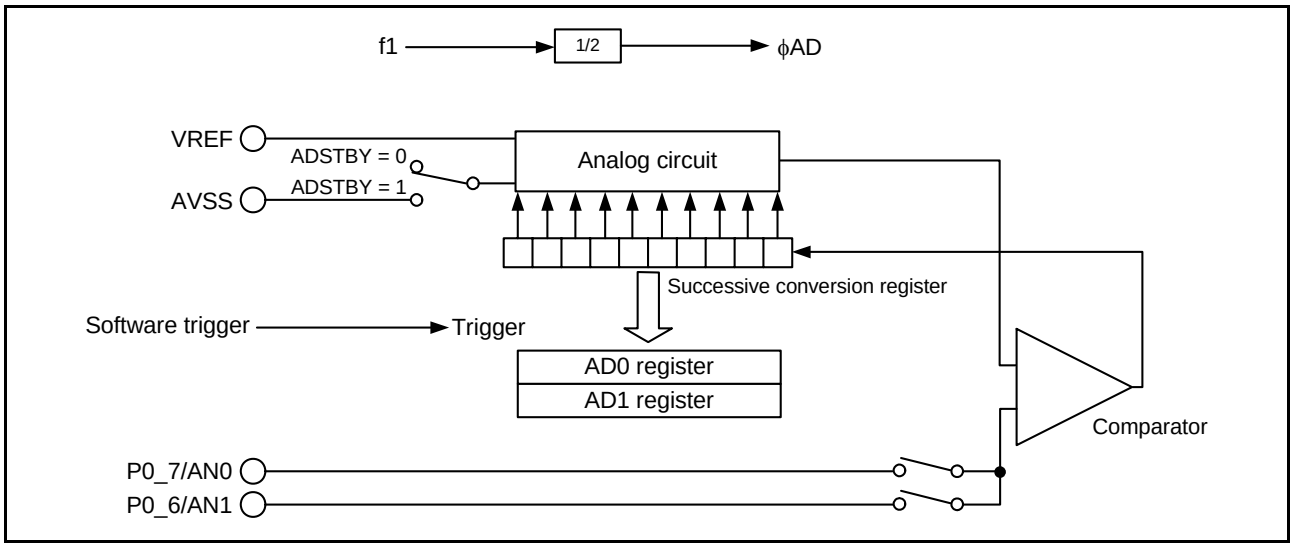


Figure 3.1 Block Diagram

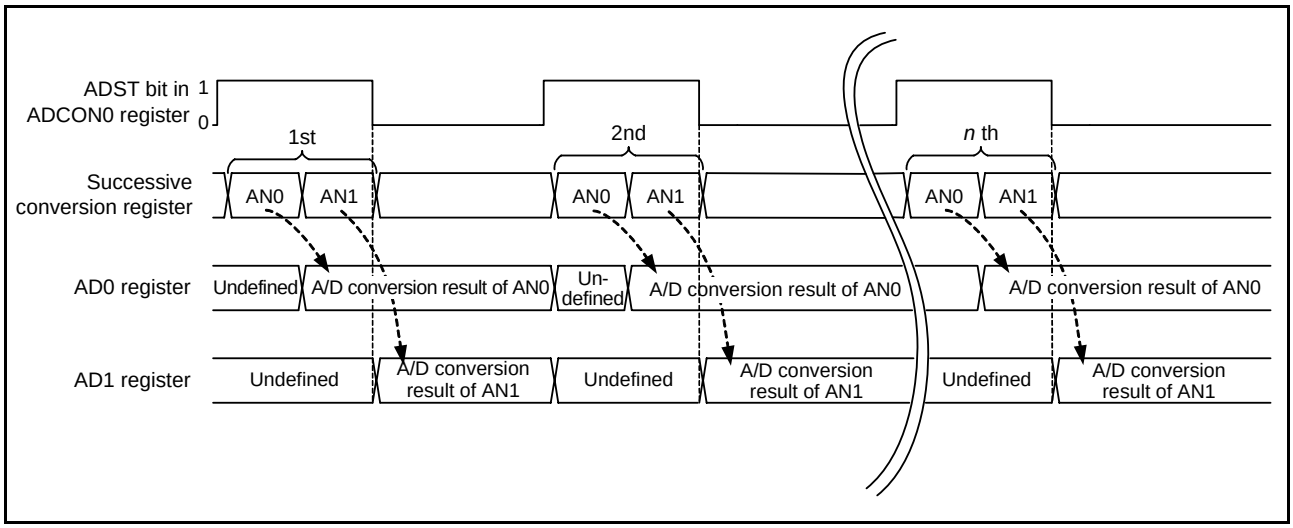


Figure 3.2 Operation in Single Sweep Mode

Table 3.1 Pins and Functions

Pin Name	I/O	Function
P0_6/AN1	Input	A/D input 1
P0_7/AN0	Input	A/D input 0

3.2 Memory

Table 3.2 Memory

Memory	Size	Remarks
ROM	197 bytes	In the rej05b1332_src.c module
RAM	4 bytes	In the rej05b1332_src.c module
Maximum user stack	12 bytes	
Maximum interrupt stack	0 bytes	

Memory size varies depending on the C compiler version and compile options. The above applies to the following conditions:

C compiler: M16C/60, 30, 20, 10, and Tiny and R8C/Tiny Series Compiler V.5.45 Release 00
Compile option: -c -finfo -dir “$(CONFIGDIR)” -R8C

4. Software

This section shows the initial setting procedures and values to set the example described in section **3. Application Example**. Refer to the latest **R8C/35C Group Hardware Manual** for details on individual registers.

The × in the register's Setting Value represents bits not used in this application, blank spaces represent bits that do not change, and the dash represents reserved bits or bits that have nothing assigned.

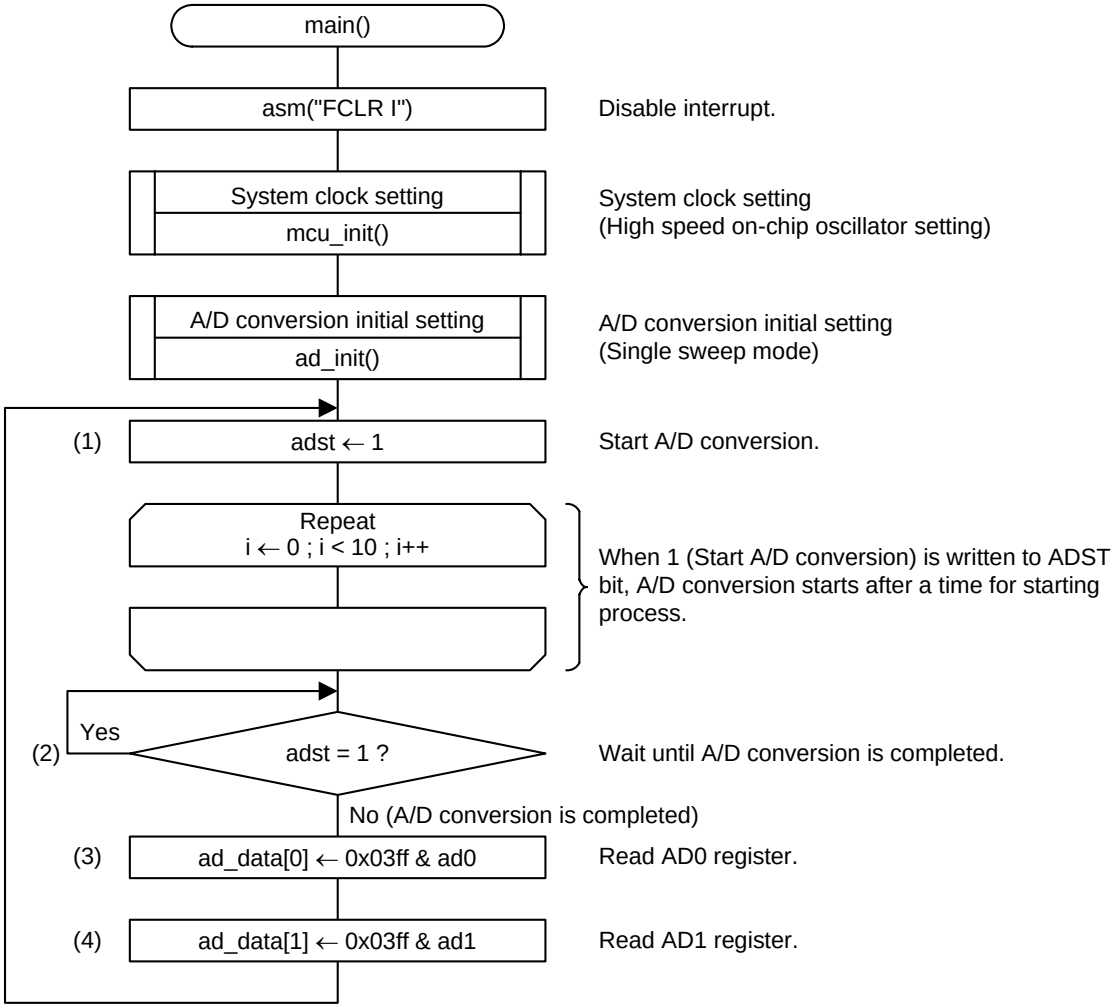
4.1 Function Tables

Declaration	void mcu_init(void)		
Outline	System clock setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	The system clock (high-speed on-chip oscillator) is set.		

Declaration	void ad_init(void)		
Outline	A/D conversion initial setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Set the SFR registers to use A/D conversion in single sweep mode.		

4.2 Main Function

• Flowchart



• Register Setting

(1) Start A/D conversion.

A/D Control Register 0 (ADCON0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	—	—	—	1

Bit	Symbol	Bit Name	Function	R/W
b0	ADST	A/D conversion start flag	1: Start A/D conversion	R/W

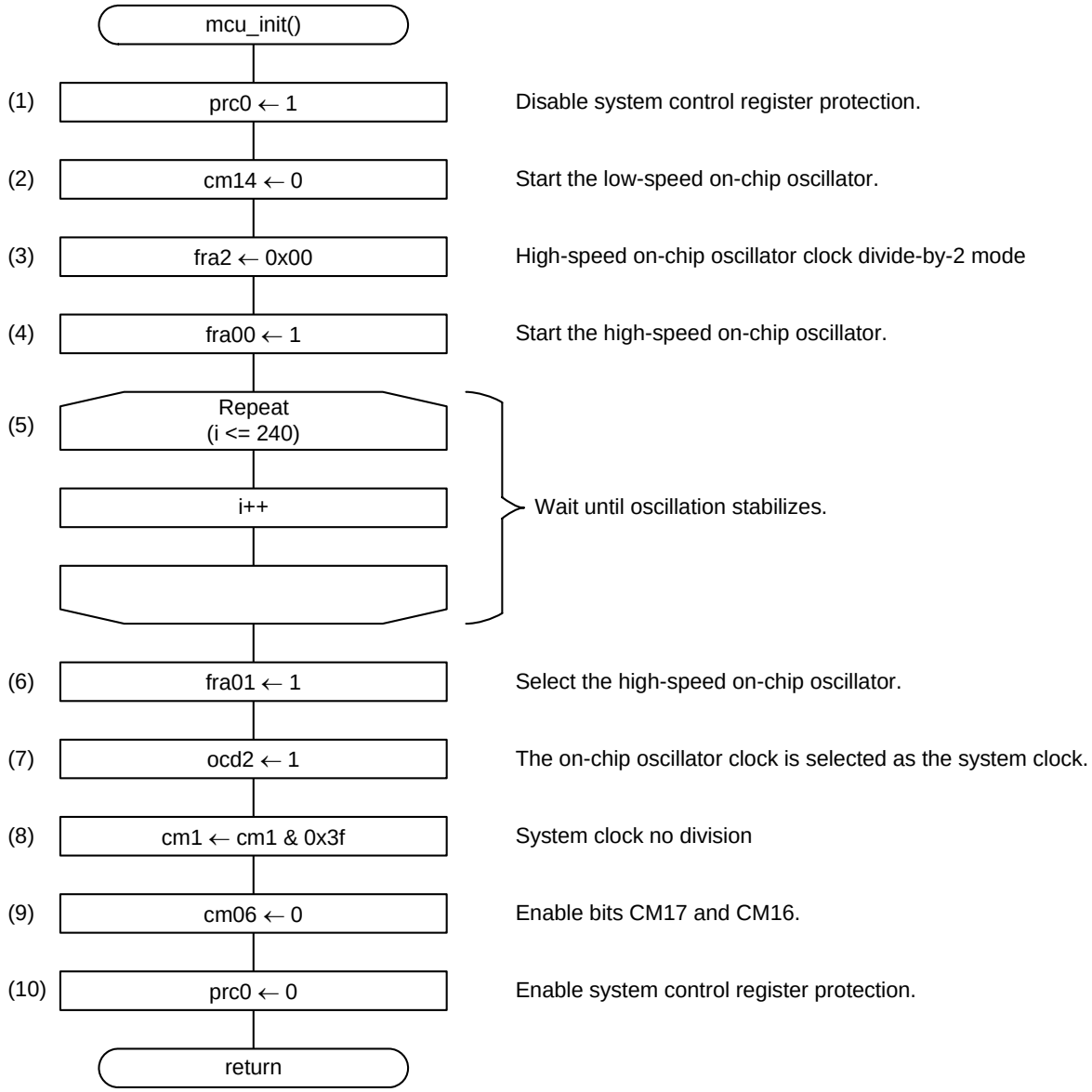
(2) Wait until A/D conversion is completed.

(3) Read the A/D conversion result in AN0.

(4) Read the A/D conversion result in AN1.

4.3 System Clock Setting

- Flowchart



• Register Setting

(1) Enable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 1: Write enabled	R/W

(2) Start the low-speed on-chip oscillator.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			—	0	x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b4	CM14	Low-speed on-chip oscillator stop bit	0: Low-speed on-chip oscillator on	R/W

(3) Set the divide ratio of the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 2 (FRA2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	—	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FRA20	High-speed on-chip oscillator frequency switching bit	Division selection These bits select the division ratio for the high-speed on-chip oscillator clock. b2 b1 b0 0 0 0: Divide-by-2 mode	R/W
b1	FRA21			R/W
b2	FRA22			R/W

(4) Start the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	—		1

Bit	Symbol	Bit Name	Function	R/W
b0	FRA00	High-speed on-chip oscillator enable bit	1: High-speed on-chip oscillator on	R/W

(5) Wait until oscillation stabilizes.

(6) Select the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	—	1	

Bit	Symbol	Bit Name	Function	R/W
b1	FRA01	High-speed on-chip oscillator select bit	1: High-speed on-chip oscillator selected	R/W

(7) Select the on-chip oscillator clock as a system clock.

Oscillation Stop Detection Register (OCD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	1	x	x

Bit	Symbol	Bit Name	Function	R/W
b2	OCD2	System clock select bit	1: On-chip oscillator clock selected	R/W

(8) Set CPU clock division select bit 1.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	—		x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b6	CM16	CPU clock division select bit 1	b7 b6 0 0: No division mode	R/W
b7	CM17			R/W

(9) Set CPU clock division select bit 0.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	0	x	x	x	x	—	—

Bit	Symbol	Bit Name	Function	R/W
b6	CM06	CPU clock division select bit 0	0: Bits CM16 and CM17 in CM1 register enabled	R/W

(10) Disable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

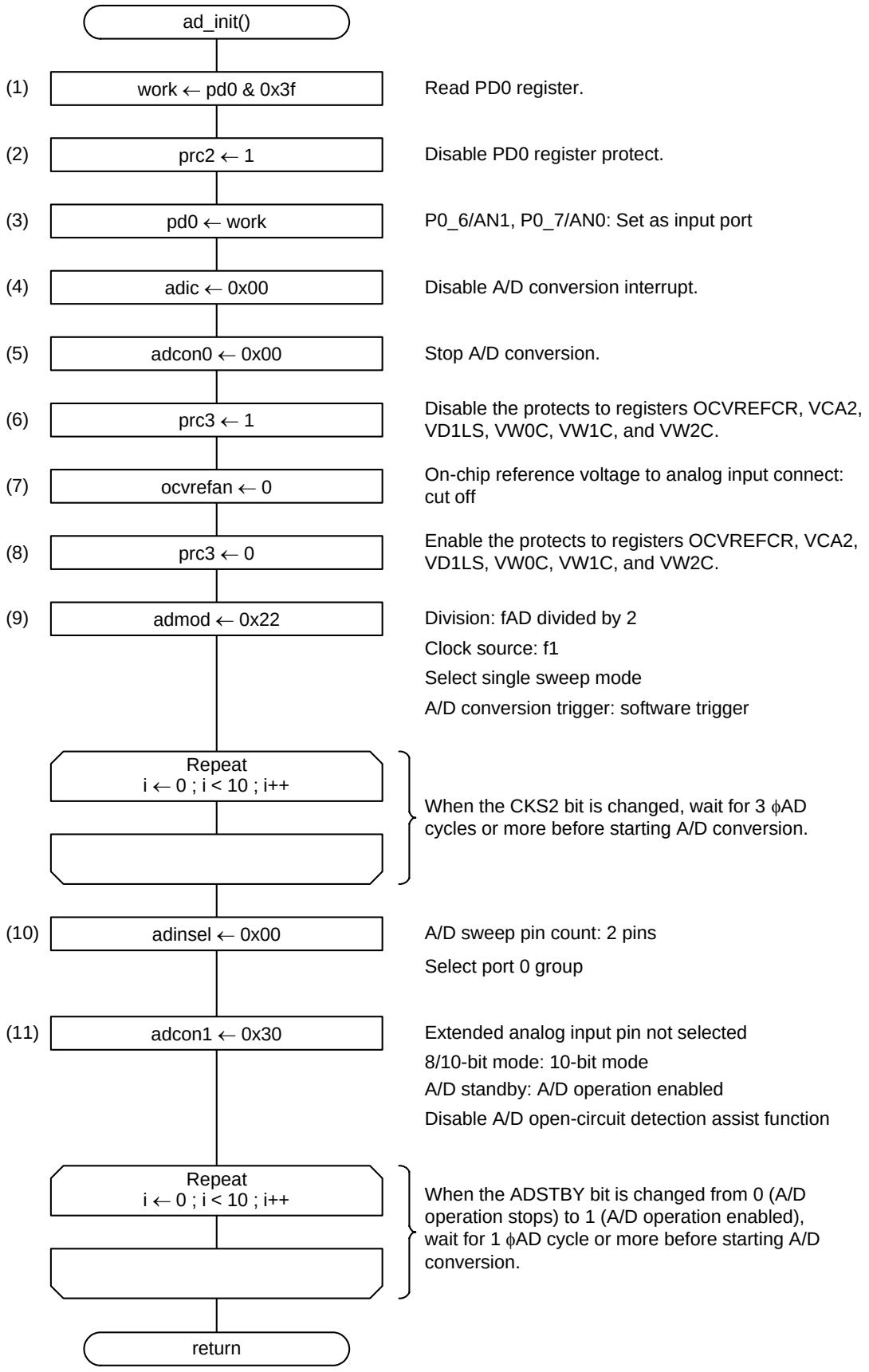
Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 0: Write disabled	R/W

4.4 A/D Conversion Initial Setting

- Flowchart



• Register Setting

(1) Read the PD0 register.

(2) Enable writing to the PD0 register.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—		1	x	x

Bit	Symbol	Bit Name	Function	R/W
b2	PRC2	Protect bit 2	Enables writing to the PD0 register. 1: Write enabled	R/W

(3) Set P0_6 and P0_7 direction bits as input ports.

Port P0 Direction Register (PD0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	x	x	x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b6	PD0_6	Port P0_6 direction bit	0: Input mode (functions as an input port)	R/W
b7	PD0_7	Port P0_7 direction bit		R/W

(4) Disable A/D conversion interrupt.

Interrupt Control Register (ADIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

(5) Stop A/D conversion.

A/D Control Register 0 (ADCON0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	—	—	—	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADST	A/D conversion start flag	0: Stop A/D conversion	R/W

(6) Enable writing to the registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	1		x	x

Bit	Symbol	Bit Name	Function	R/W
b3	PRC3	Protect bit 3	Enables writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C. 1: Write enabled	R/W

(7) Cut off on-chip reference voltage from the analog input.

On-Chip Reference Voltage Control Register (OCVREFCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	—	—	—	0

Bit	Symbol	Bit Name	Function	R/W
b0	OCVREFAN	On-chip reference voltage to analog input connect bit	0: On-chip reference voltage and analog input are cut off	R/W

(8) Disable writing to the registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0		x	x

Bit	Symbol	Bit Name	Function	R/W
b3	PRC3	Protect bit 3	Enables writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C. 0: Write disabled	R/W

(9) Set the A/D mode register.

A/D Mode Register (ADMOD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	1	0	0	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	CKS0	Division select bit	b1 b0 1 0: fAD divided by 2	R/W
b1	CKS1			R/W
b2	CKS2	Clock source select bit	0: Select f1	R/W
b3	MD0	A/D operating mode select bit	b5 b4 b3 1 0 0: Single sweep mode	R/W
b4	MD1			R/W
b5	MD2			R/W
b6	ADCAP0	A/D conversion trigger select bit	b7 b6 0 0: A/D conversion start by software trigger (ADST bit in the ADCON0 register)	R/W
b7	ADCAP1			R/W

(10) Select the A/D sweep pin count as 2 pins and A/D input group as port P0.

A/D Input Select Register (ADINSEL)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	—	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b4	SCAN0	A/D sweep pin count select bits	b5 b4 0 0: 2 pins	R/W
b5	SCAN1			R/W
b6	ADGSEL0	A/D input group select bits	b7 b6 0 0: Port P0 group selected	R/W
b7	ADGSEL1			R/W

(11) Set the A/D control register 1.

A/D Control Register 1 (ADCON1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	0	1	1	—	—	—	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADEX0	Extended analog input pin select bit	0: Extended analog input pin not selected	R/W
b4	BITS	8/10-bit mode select bit	1: 10-bit mode	R/W
b5	ADSTBY	A/D standby bit	1: A/D operation enabled	R/W
b6	ADDDAEN	A/D open-circuit detection assist function enable bit	0: Disabled	R/W

5. Sample Program

A sample program can be downloaded from the Renesas Technology website.
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6. Reference Documents

Hardware Manual
R8C/35C Group Hardware Manual Rev.0.10
The latest version can be downloaded from the Renesas Technology website.

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REVISION HISTORY	R8C/35C Group A/D Converter in Single Sweep Mode

Rev.	Date	Description	
		Page	Summary
1.00	Oct 22, 2009	–	First Edition issued

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