## **Application Note**

# RENESAS

## D2-4P

Layout Guidelines

## Abstract

The D2-4P (<u>D2-45057</u> and <u>D2-45157</u>) IC devices are complete Class-D digital audio amplifiers combining integrated power stages with a PWM controller and DSP audio processing. These devices provide a flexible and efficient single-chip audio amplifier solution.

Performance of audio amplifier systems is typically dependent upon circuit layout. This application note provides guidelines and layout recommendations for successful D2-4P based system designs.

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## **Related Literature**

For a full list of related documents, visit our website:

• <u>D2-45057</u>, <u>D2-45157</u> device pages



## 1. Overview

## 1.1 Design Goals

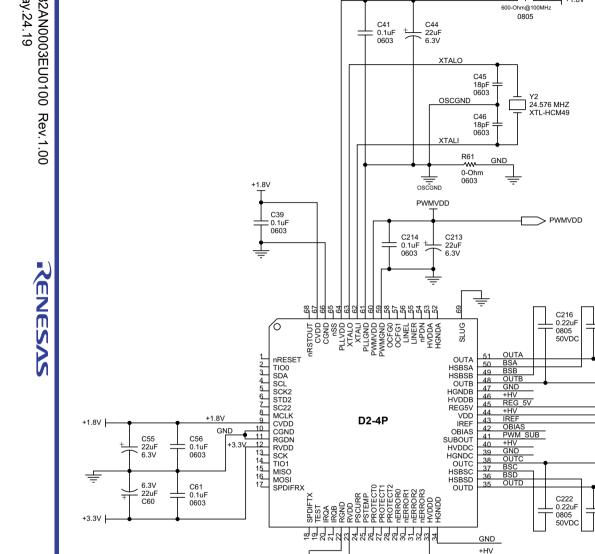
- Optimize amplifier output performance
  - $\circ$  Maximize efficiency by circuit trace routing
  - Minimize noise and interference
- Optimize thermal performance
  - $\circ$  Best use of PC board and layout to dissipate heat
- Optimize EMI performance
  - Effective bypassing to minimize interferences
- Minimize PC board complexity and cost

## 1.2 Figure References

The figures in this document include a simplified schematic (Figure 1 on page 3) showing the significant power bypass capacitors and related connections and components. Figures 2 through 5 starting on page 5, show examples for PCB layout (top view).



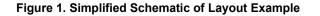




C70

0.1uF 0603 +3.3V

÷



BD1

+1.8V

+3.3V

÷

R62 ₹ 10 0603

C50

6.3V

+<u>H</u>∨

+HV

₩35V

Ŧ

C217 0.22uF

0805

50VDC

C223

- 0.22uF

0805 50VDC

R256

121K 0603

÷

C202

100uF

KMG

C206

0.1uF

0603

50VDC

· 1000uF

KY SERIES

One each bulk/HF cap pair per IPS HVDD pin.

C207

0.1uF

0603

50VDC

+<u>H</u>V

Ŧ

L11

15uH

L12

15uH

L13

15uH

L14

15uH

C226 0.1uF

50VDC 0603

C122

1uF

0805

÷

+HV

+HV

C204

100uF

35V

KMG

C208

. 0.1uF

0603

50VDC

C198

0.33uF

50VDC 1206 ÷

C218 0.33uF

50VDC

+<u>HV</u>

╧

÷

+HV

C205

100uF

- 35V

KMG

C209

0.1uF

0603

C199 0.1uF

50VDC

0603

C211 0.1uF

50VDC 0603

C219 0.1uF

50VDC

0603

C228

0.1uF

0603

50VDC

OUT\_LEFT+

OUT\_LEFT-

OUT\_RIGHT+

OUT\_RIGHT-

50VDC

+<u>HV</u>

÷

OUTA

OUTB

OUTC

OUTD

C225

0.1uF

0603

+HV

C203

100uF

KMG

35V

PLLAVDD

Layout Guidelines

## 2. Layout Recommendations

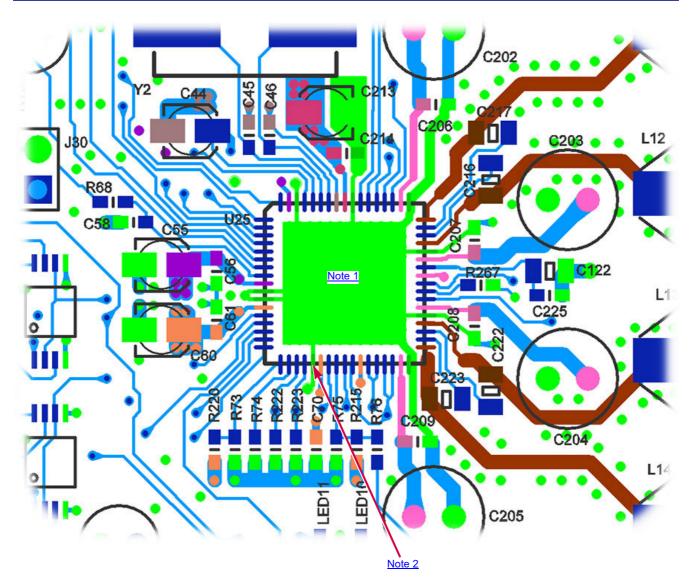
- Tie the I<sub>REF</sub> resistor connected to Pin 43 directly to the thermal pad ground to avoid noise pickup. I<sub>REF</sub> is
  sensitive to noise, so route its connections as short and direct as possible, and do not connect near any HGND
  ground connections.
- Low voltage signals and power should follow standard design practices, avoid routing or component placement close to the HVDD, HGND, or output circuits.
- When routing ground connections on both top and bottom of the PCB, use as many "stitching" vias as possible to minimize connection impedance, and to maximize the connected surface area.
- Heat dissipation is improved by filling PCB space with as much copper as possible. The PCB provides the heat dissipation path, but heavier copper plating and higher copper surface area helps to improve thermal performance. Minimize the amount of circuit traces on the bottom-side PCB layer within the immediate area below the D2-4P, to allow as much contiguous copper area as possible to aid in dissipating heat from that area.
- Wherever it is practical and acceptable within circuit connection limitations, use additional vias to tie the top layer to the bottom copper layers, further aiding heat dissipation. Typically an application supports adding at least 20 to 30 vias to help spread heat from top to bottom of the PCB.
- Avoid using vias crossing from top to bottom of any power traces located between bypass components and D2-4P pins. While via use may help in thermal dissipation, their use in power and ground connection circuits is not as optimum for minimizing conductor path impedances.

## 2.1 Component Placement Priority

Ideally, mount all components as close as possible to the D2-4P device, but physical space requirements can limit placement options. The priority of components to be placed closest to the device is:

- Power supply 0.1µF decoupling capacitors (low voltage and high voltage supplies). This maximizes efficiency
  of power conditioning to the device, reduces noise, and minimizes the exposure that can contribute to EMI.
  These capacitors perform high-frequency bypassing, and to maximize that capability, close placement
  minimizes high-frequency impedance from interconnecting PCB traces.
- 2. Output 0.22µF bootstrap capacitors.
- 3. Power supply filter capacitors.
- 4. Mount other components on either the top or bottom of the PCB as close as possible to the D2-4P.



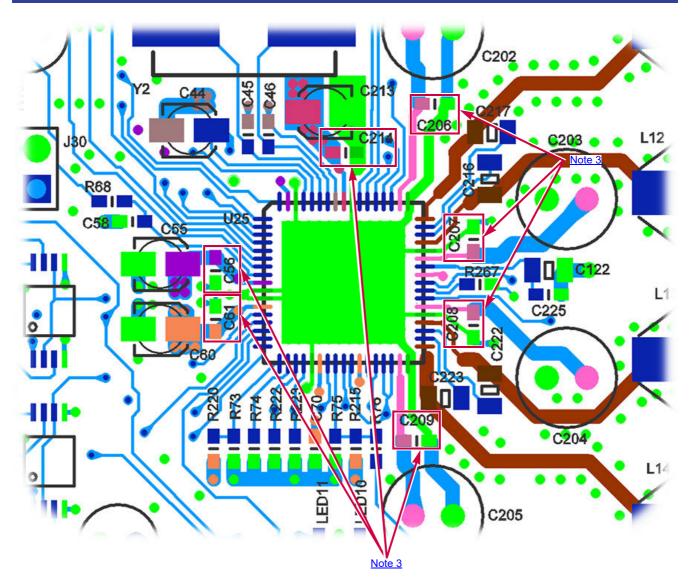


#### Notes:

- 1. The D2-4P package includes a thermal pad on its bottom side that is internally connected within the device to its ground connections. The printed circuit board should provide this thermal pad on the top layer of the PCB, and use it as one of the ground connections to the D2-4P. The PCB copper is used to dissipate heat away from the D2-4P device, but is also a circuit ground.
- 2. Connect all ground pins (nine places) of the D2-4P directly to this thermal ground pad on the PC board.

#### Figure 2. PCB Layout Example - Ground Connections to Thermal Pad



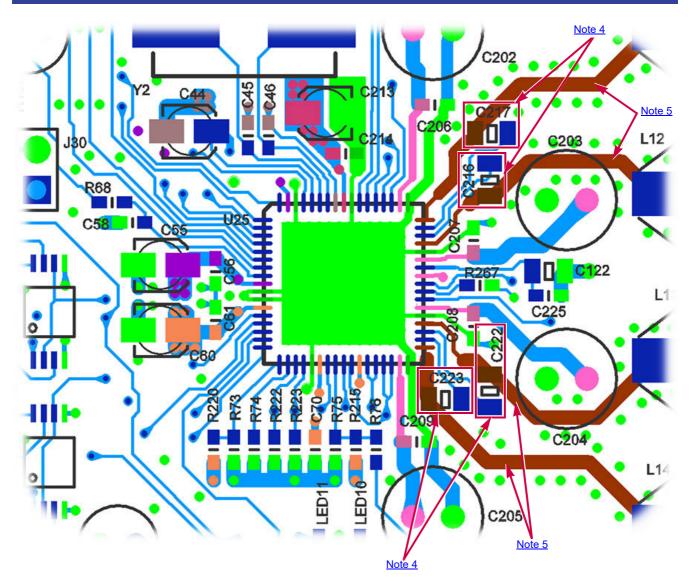


#### Note:

3. Mount all decoupling capacitors on the top side of the PCB. Route all power and ground connections between the D2-4P and the bypass capacitors on the top side.

#### Figure 3. PCB Layout Example - Decoupling Capacitor Placements



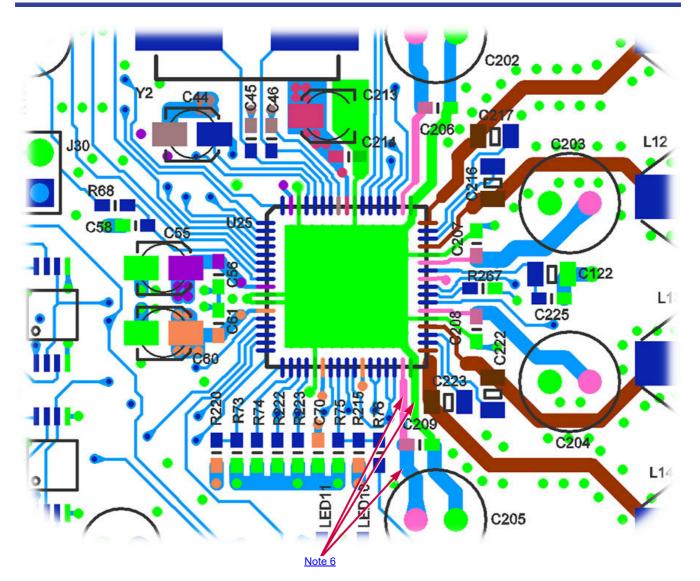


#### Notes:

- 4. Mount the bootstrap capacitors on the top side of the PCB, as close as possible between the device bootstrap pins and the output pins. Route their connections directly on the top side of the PCB and avoid crossing from the top to bottom layers.
- 5. For power stage output traces, use large as possible trace sizes, and route traces as short and direct as possible.

Figure 4. PCB Layout Example - Output Traces, Components





Note:

6. For HVDD supply power and HGND ground connections, use trace sizes as large as possible, and route traces as short and direct as possible.

Figure 5. PCB Layout Example - Power Traces

## 3. Revision History

Rev.	Date	Description
1.00	May.24.19	Initial release





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