R2A20114BFP

Application Note

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Introduction

R2A20114BFP is a boost converter control IC with PFC (Power Factor Correction).

Employing continuous conduction mode (CCM), it has interleaving control which produces 180 degrees phase shift between the output signals (GD1,2) driving the boost converters. Interleaving control of the boost converters enables the system to perform high conversion efficiency and low switching noises and, at the same time, to reduces ripple currents in input and output current and then this allows use of smaller components such as boost inductors, input filters and output capacitors, which is best suitable for high power applications.

Based on the R2A20114AFP, R2A20114BFP features improved usability such as built-in PFC boost voltage control, current detection amplifier with differential inputs, independent and high-functional error output pin, timer reset of OFF latch, and partial switch for PFC.

The two mode over voltage protection, over current protection are built in to enable construct a reliable power supply system with few external parts.

Target Device

R2A20114BFP

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1. Outline

R2A20114BFP is a boost converter control IC with PFC (Power Factor Correction).

Employing continuous conduction mode (CCM), it has interleaving control which produces 180 degrees phase shift between the output signals (GD1,2) driving the boost converters. Interleaving control of the boost converters enables the system to perform high conversion efficiency and low switching noises and, at the same time, to reduces ripple currents in input and output current and then this allows use of smaller components such as boost inductors, input filters and output capacitors, which is best suitable for high power applications.

Also, R2A20114BFP uses resistors to detect current of switching elements, enabling small space and low cost current sense best suitable for air-conditioner application.

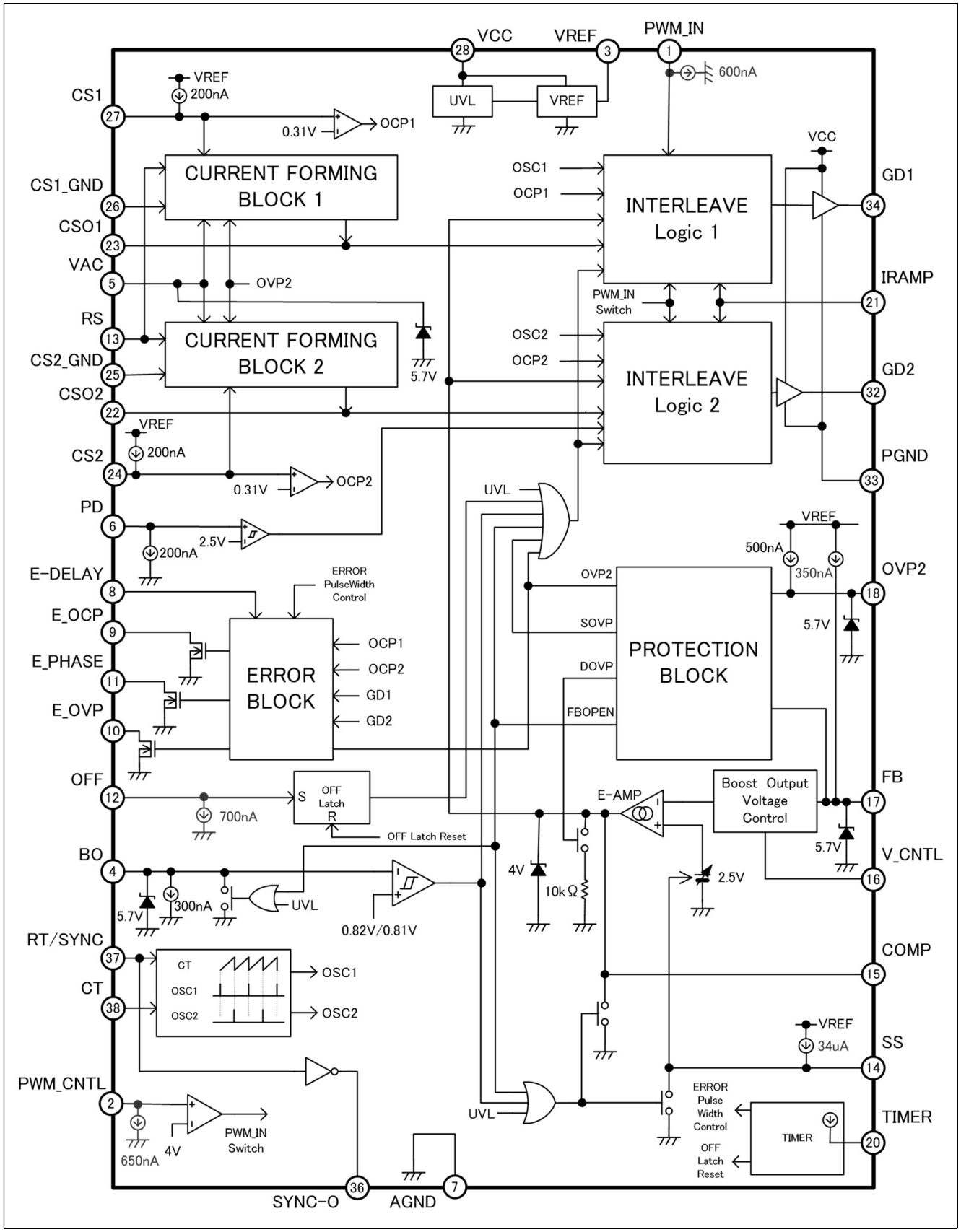
The two mode over voltage protection, over current protection are built in to enable construct a reliable power supply system with few external parts.

Compared to the conventional R2A20114AFP, harmonic current characteristics in smaller input/output voltage difference is improved in R2A20114BFP. And functions for stable operation are improved. Table 1 shows the difference from R2A20114AFP.

Table1 Difference between R2A20114AFP and R2A20114BPF

Function	R2A20114BFP	R2A20114AFP (conventional)
Boost voltage control	Built-in	External circuits required
Current amplifier	Differential amplifier	Single end
Error detecting pins	Independent OCP, OVP, Phase error output pin	Sharing 1 pin
	Error can be distinguished even if error pins are put together, by changing output duration for the error	Errors can't be distinguished
	Low at error	High at error
OFF latch reset	Timer automatically reset	Need to power off to reset
Partial SW	Built-in	Not applicable
Semi bridge-less PFC	Negative voltage of CS pin	Not applicable
4 phases operation	SYNC-O signal is inverter output of RT/SYNC wave	External circuits required.

2. Block Diagram



3. R2A20114BFP Block Descriptions

3.1 Protection

R2A20114BFP provides 4 types of protecting functions, over-voltage protection, over-voltage protection 2, over-current protection and feedback loop open detect.

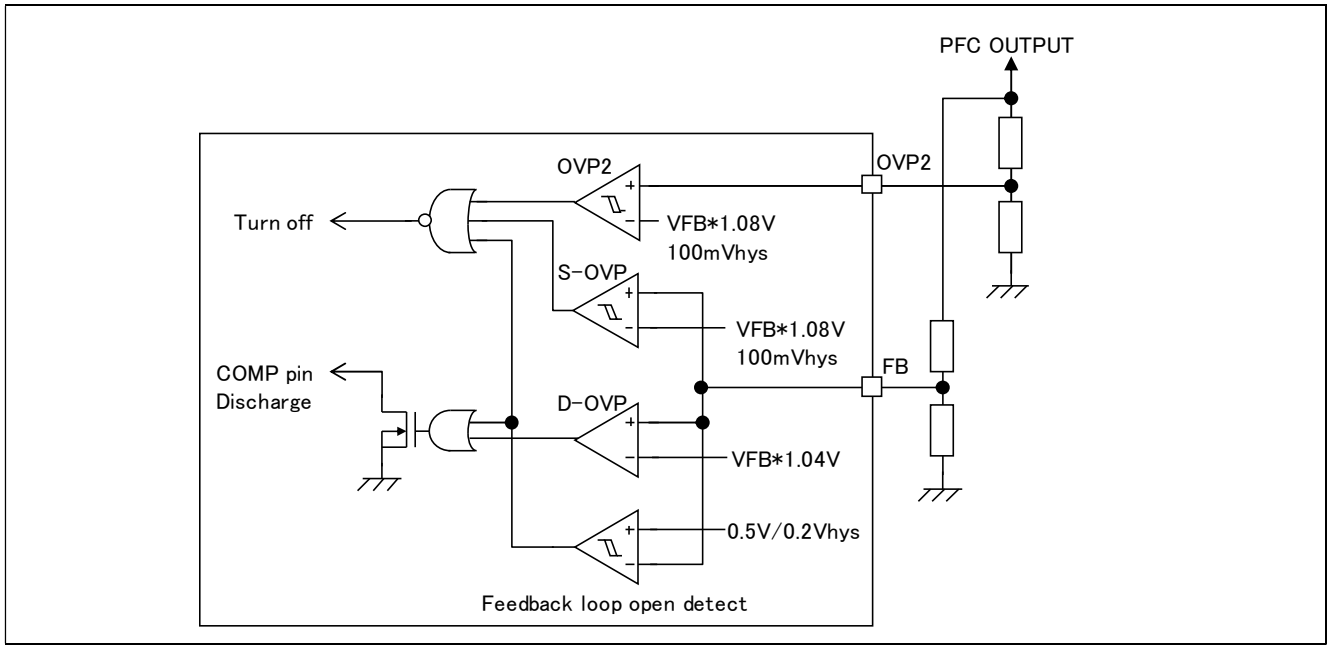


Figure 1 Protection

3.1.1 Over-voltage protection <OVP>

The over voltage protection has two step protections. Dynamic over voltage protection (D-OVP) discharges COMP pin voltage when FB pin voltage reaches 1.04 *VFB (2.5Vtyp). The Power MOSFET on time is limited gradually, therefore the audio noise is avoided because an inductor current does not stop suddenly. Static over voltage protection (S-OVP) stops IC output when FB pin voltage reaches 1.08 *VFB (2.5Vtyp). A Power MOSFET turns off quickly and S-OVP keeps stopping until FB pin voltage reaches 1.08 *VFB (2.5Vtyp) – 100mV.

3.1.2 Over-voltage protection 2 <OVP2>

In over-voltage protection 2 (OVP2), PFC output voltage is monitored by a special pin independent from FB pin which has D-OVP and S-OVP functions. When OVP2 pin becomes 1.08*VFB(2.5Vtyp), it stops switching and keeps re-start when OVP2 pin voltage reaches 1.08 *VFB (2.5Vtyp) – 100mV. If over-voltage protection 2 is detected, E_OVP pin operates. For details, refer to item 3.5.

3.1.3 Feedback loop open detect

The feedback open-loop protection discharges COMP pin voltage to stop IC output during FB pin voltage is under 0.5V There is 0.2V hysteresis in detection voltage.

3.1.4 Over-current protection <OCP>

R2A20114BFP stops output of GD1 or GD2 when CS1 or CS2 pin reaches 0.31V. OCP is reset every cycle by pulse by pulse protection.

When over current is detected, E-DELAY pin charges, and turn into discharge status when over current status is cancelled. If over-current status continues up to E-DELAY pin being 2.45V, open drain element at E-OCP pin turns ON. For details, refer to item 3.5.

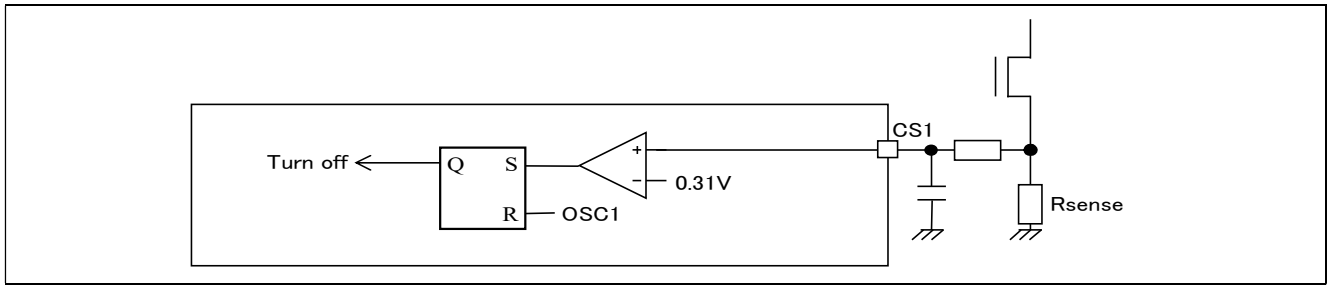


Figure 2 Over-current protection

3.2 Drive Stage

R2A20114BFP contains two totem-pole output for phase 1 and phase 2. The maximum rating of drivability is 0.2A peak. Use the drive circuit to adjust the drivability for switching elements characteristics used. The following shows a drive circuit example. By connecting GND of drive circuit to emitter (or source), it can avoid the influence of long wiring for stable characteristics

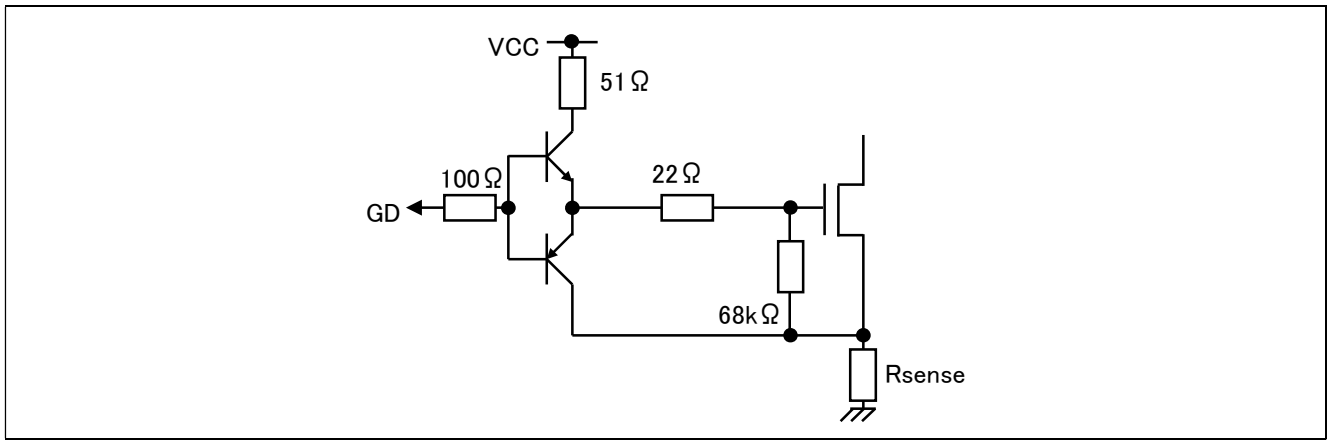


Figure 3 Drive circuit example

3.3 Soft Start

ON time increase gradually by connecting capacitor between SS pin and GND. SS pin charge current is 34uA constant current, and SS time is adjustable by changing external capacitor value. SS pin discharge the capacitor when VCC is under UVLO threshold voltage or FB voltage is under 0.3Vtyp. or BO voltage is under 0.81V.

The error signal E_OVP may be output during the soft start period at startup. When the gate pulse is stopped by using E_OVP, it is recommended to mask the error signal, or count the number of error signal occurrence and stop the system when detecting a certain number of times by microcomputer or the like.

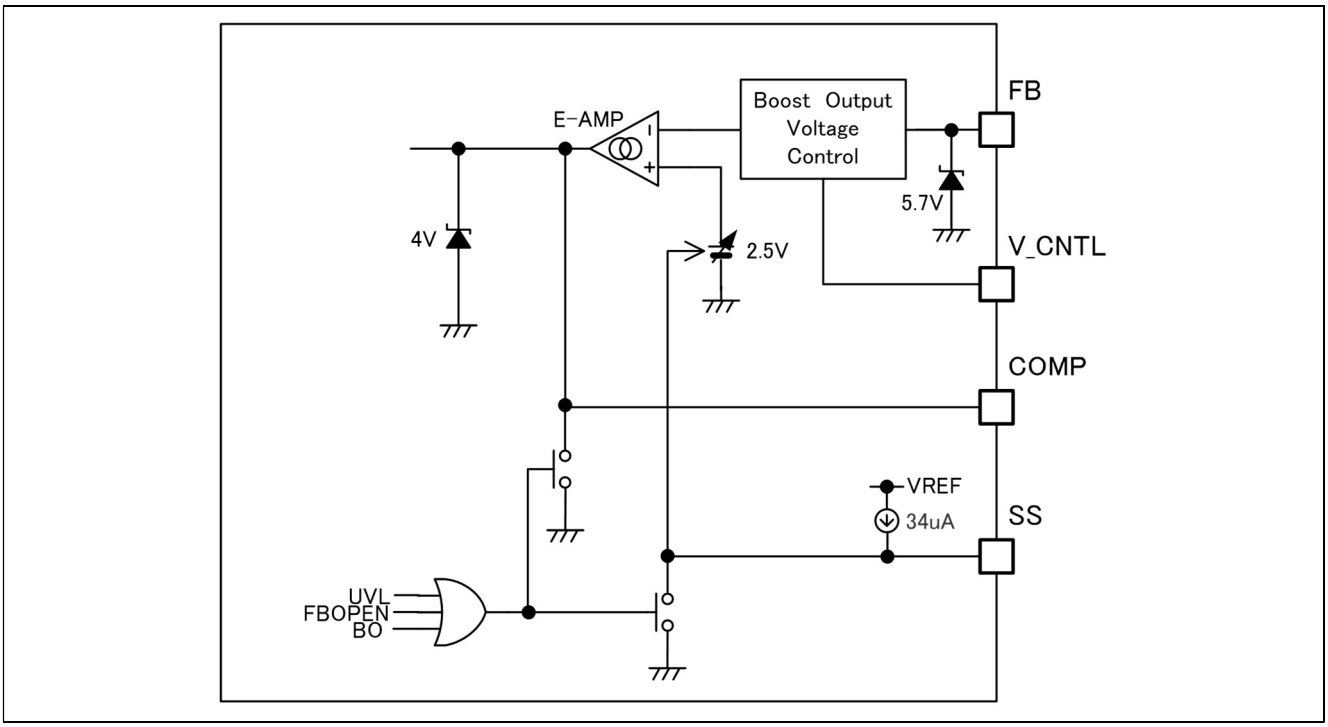


Figure 4 Soft Start

3.4 Phase Drop

When the PD signal becomes 2.5V or more, GD2 stops in order to reduce switching loss at light load

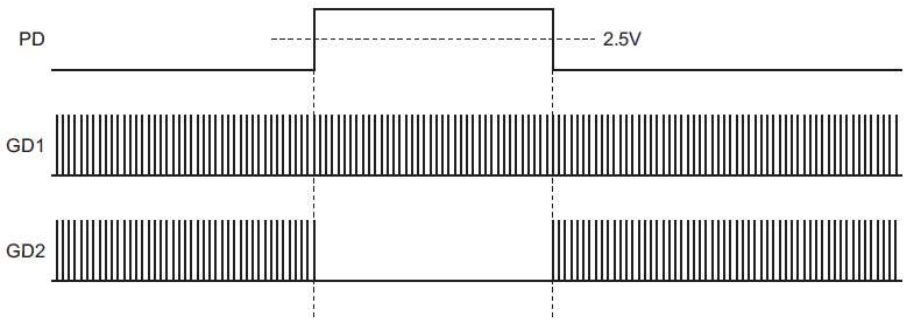


Figure 5 Phase Drop

Phase drop switching is equal to increase to twice/reduce by half momentarily. It prevents output voltage variation at phase drop switching by controlling slope of internal RAMP signal to increase/decrease momentary current supply.

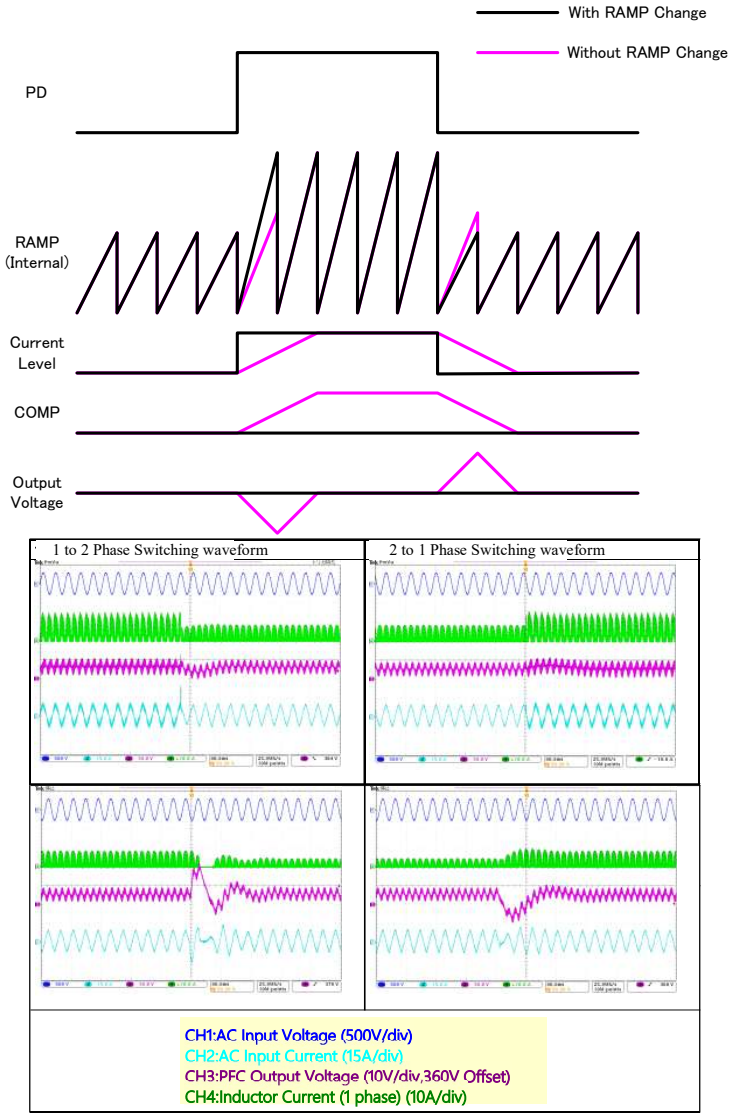


Figure 6 Operation at Phase Drop Switching

3.5 Error Function

When over-voltage protection 2 (OVP2), over-current protection (OCP) or phase error is detected, the corresponding error pin (E_OVP pin, E_OCP pin, E_PHASE pin respectively) operates in R2A20114BFP. Each error pins are open drain output and the open drain element turns ON at error detection. During the error continues, the open drain element keeps ON. If any error is detected, TIMER pin charges. If the TIMER pin does not reach 2Vtyp when the error is cancelled, the open drain element keeps ON until it reaches 2V typ., then turns OFF. If TIMER pin voltage is over 2Vtyp., the open drain element turns OFF immediately. When open drain element becomes OFF, the TIMER pin current switches into rapid discharge mode.

The charge current varies depending on the error. Since the period of error pin being ON is different in case of transient short-time error, MCU can distinguish the error type.

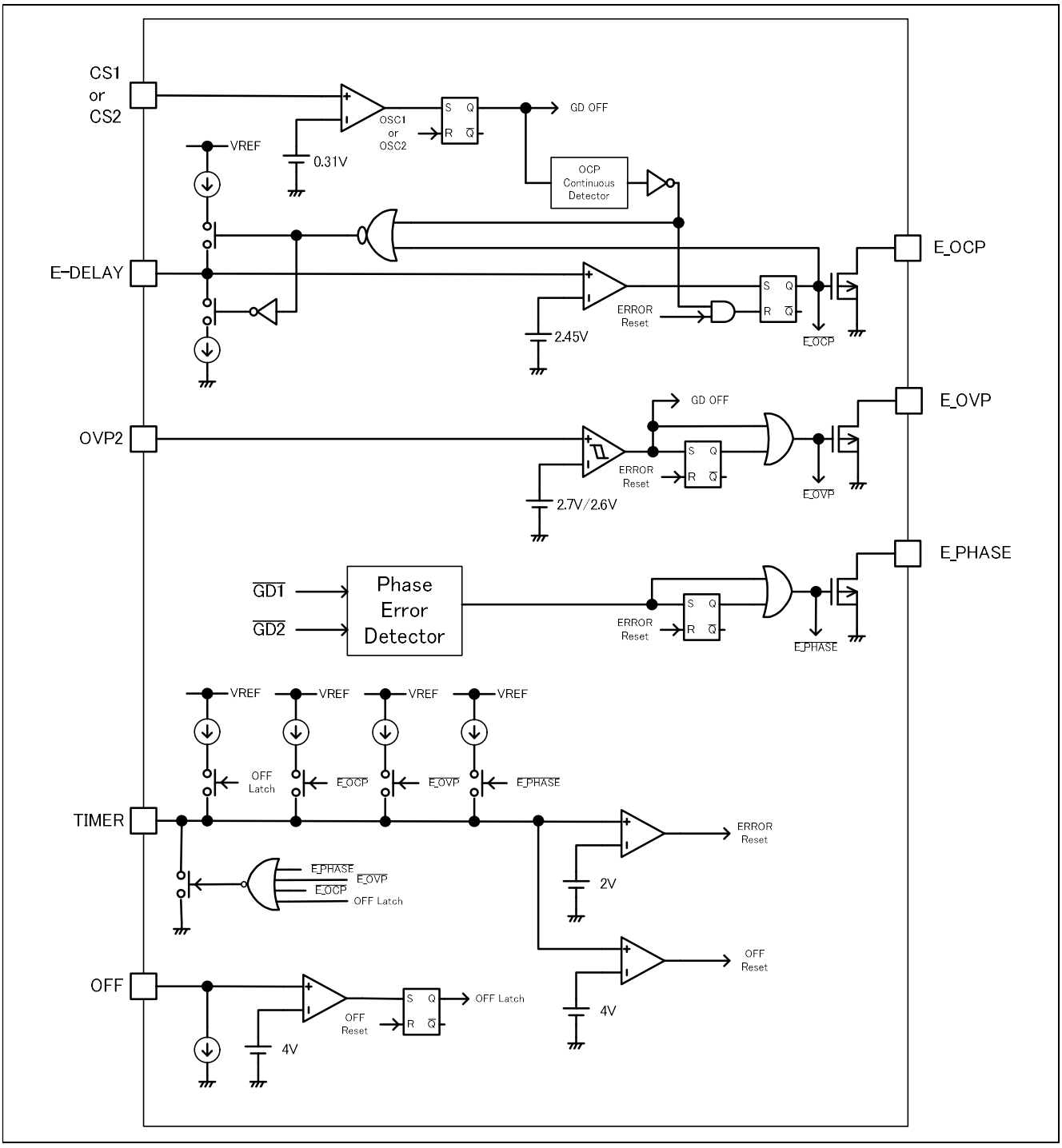


Figure 7 Error Function

3.5.1 E_OVP pin movement by overvoltage protection detection 2 (OVP2)

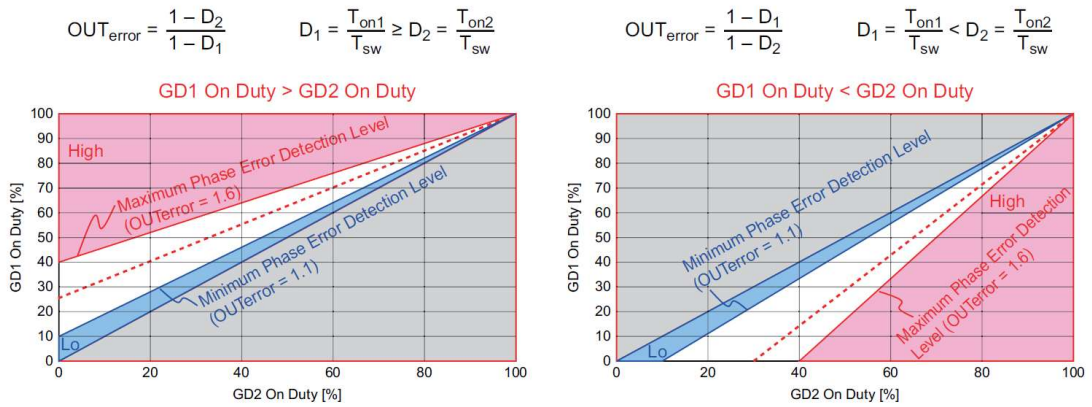
When an OVP2 pin voltage exceeds 1.08*VFB[2.5Vtyp.], it becomes OVP2 error and E_OVP pin operates. When an OVP2 pin voltage becomes less than 1.08*VFB[2.5Vtyp.]-100mV, the over-voltage error is cancelled.

The error signal E_OVP may be output during the soft start period at startup. When the gate pulse is stopped by using E_OVP, it is recommended to mask the error signal, or count the number of error signal occurrence and stop the system when detecting a certain number of times by microcomputer or the like.

Also in case the switching of 2 phase and 4 phase is done by ON/OFF of slave IC in 4 phase application , it is done by pulling up OVP2 pin of slave IC, so that Please be aware that an error signal is output from the E_OVP pin of the slave IC.

3.5.2 E_PHASE pin movement by phase error detection 2

When the duty ratio of GD1, 2 becomes large by abnormal movement such as the open/short destruction of the power element, it's judged to be phase error and E_PHASE pin operates. When the duty ratio of GD1,2 becomes small close to 1, the phase error is cancelled. The followings show the area judged to be phase error with considering variations of devices.



Phase error detection level is the same for light and heavy loads.

Figure 8 Phase Error Area

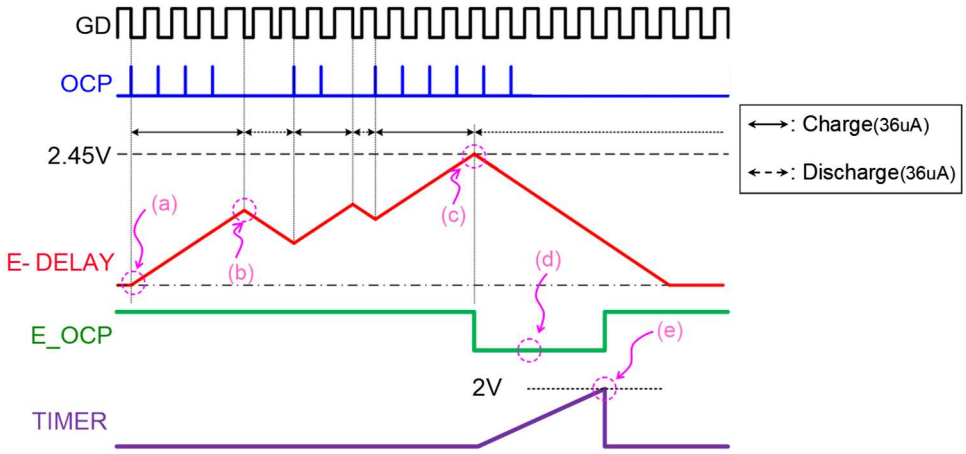
When the duty of GD1 and GD2 is within the deep blue area, E_PHASE pin is OFF. If it's in red area, E_PHASE pin turns ON. The white area is dispersion area of phase error detection circuits, where phase error may be detected.

In normal operation, the duty is balanced by feedback control and the phase error does not occur. However, the duty balance may be temporarily lost in transient duration such as sudden change of load or input voltage at power on, to make E_PHASE pin ON

3.5.3 E_OCP pin movement by overcurrent detection

When the over-current protection operates, E-DELAY pin start charging. If the over-current is cancelled, E-DELAY discharges. When over-current status continue up to E-DELAY pin voltage being the threshold 2.45V, it's in OCP error. If the overcurrent condition continues, the OCP error condition will also continue.

Connecting a capacitor between E-DELAY pin and GND can adjust the time from the OCP detection to error signal output. The followings outlines OCP timer latch operation.



a) E-DELAY starts to charge when OCP is detected.
b) E-DELAY switches from charge to discharge if OCP is not detected by IC output Turn-off
c) When E-DELAY reaches threshold 2.45V, OCP becomes Low and E-DELAY starts to discharge.
d) OCP keeps Low even if OCP is not detected until TIMER reaches to 2V.
e) OCP turns to High when TIMER reaches to 2V.

Figure 9 Over-current Error Operation

3.6 OFF Function

When a pulse signal which amplitude is over than the threshold voltage Voff is added to OFF pin, GD pulse stops and TIMER pin is in charge mode. The OFF function is cancelled when TIMER pin is charged up to 4V(typ.) and the gate pulse is reset and the TIMER pin is discharged rapidly.

■The pulse width Toff_in input to the OFF pin must be shorter than the TIMER pin charging time Tres_lat.

■When stopping with the OFF function by error signal ,since there is a possibility that each error signal is output during transient period such as startup, brownout , rapid load change, it is recommended to mask the error signal during the transient period, or count the number of error signal occurrence and stop the system when detecting a certain number of times by connecting to the OFF pin via a microcomputer or the like. When an error signal is received outside the masking period, follow the regulation of the above pulse for pulses input from the microcomputer to the OFF pin. This latch mode is also cancelled by reducing Vcc pin voltage below UVLO Turn-off Threshold voltage to reset the IC. OFF pin may respond to signals as short as 10ns. To avoid malfunction, it's necessary to construct filters if OFF function is used.

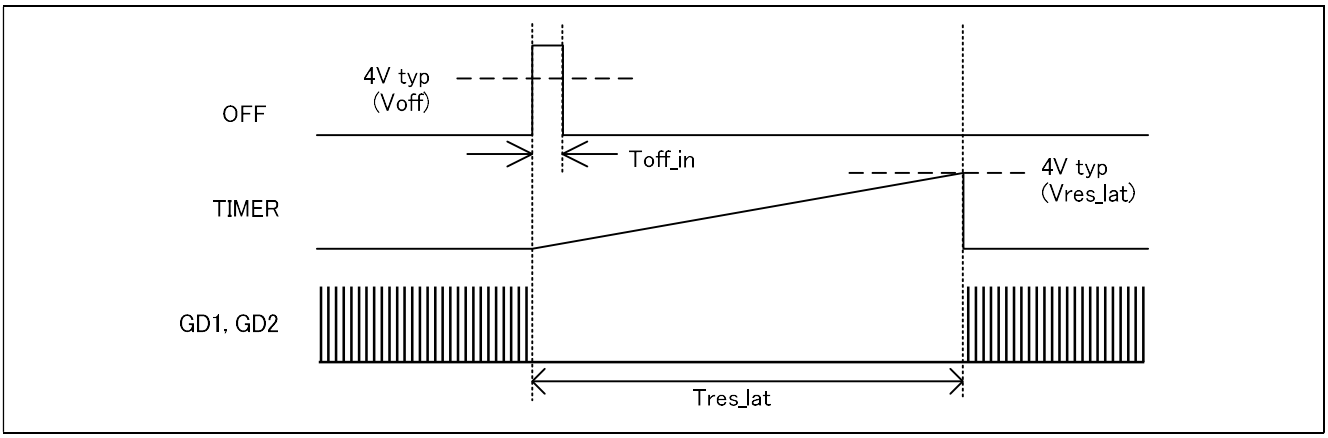


Figure 3.6 OFF Function Operation

3.7 Synchronous Function

R2A20114BFP switched synchronous mode by inputting synchronous signal into RT/SYNC pin. The followings shows the detail of synchronous operation.

The following figure is outline of built-in oscillator.

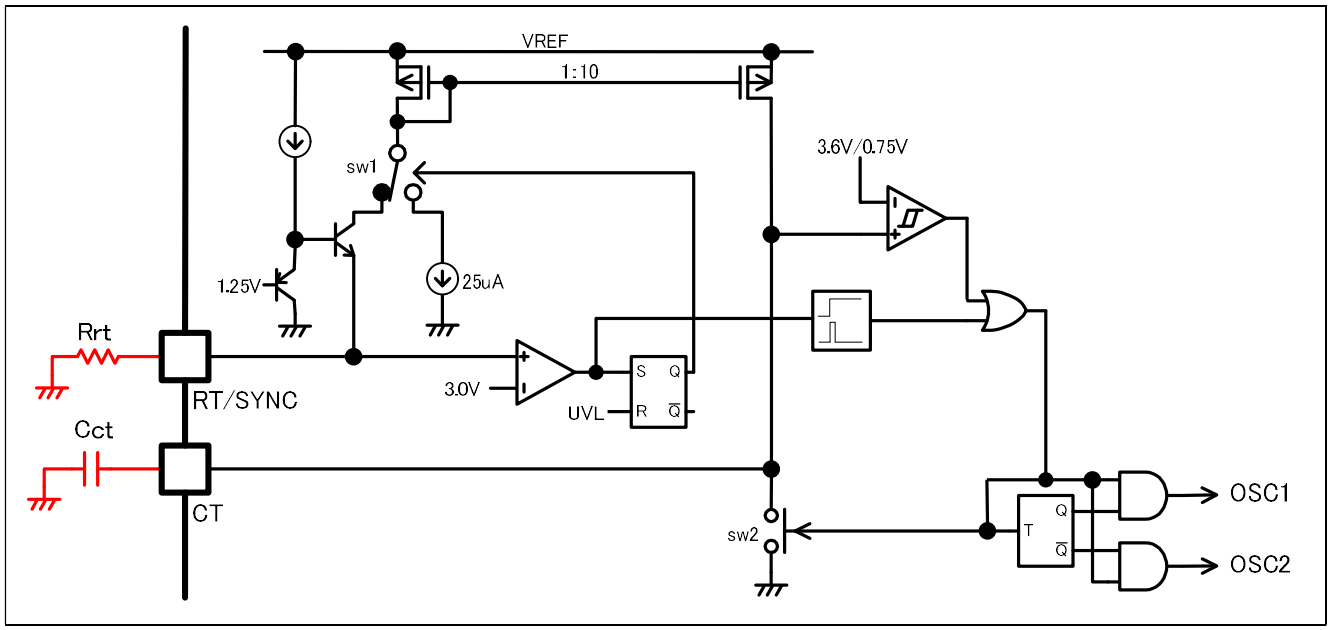


Figure 10 Outline of Synchronous Circuits

Synchronous signal is rise edge (3Vtyp. threshold) trigger operation. As shown in the synchronous timing chart, the fall timing of GD1 and GD2 are alternatively determined by rise edge of synchronous signal.

R2A20114BFP switches into synchronous operation mode once RT/SYNC pin voltage exceeds 3Vtyp. In synchronous operation mode, internal switch sw1 turns and the CT charge current is switched to constant current of 250uAtyp. ± 30%, which is determined in IC internally and does not depend on resistance at RT/SYNC pin. Therefore, the IC operates in this charge current and the frequency by CT pin capacitance unless synchronous input is not provided. Cct should be determined so as to make this frequency slower than the frequency of synchronous signal.

Once 3Vtyp. or more voltage is applied to TR/RYNC pin, sw1 does not turn to RT/SYNC pin side unless supply voltage Vcc is lower than UVL voltage. To release the synchronous operation, IC should be reset by decreasing Vcc.

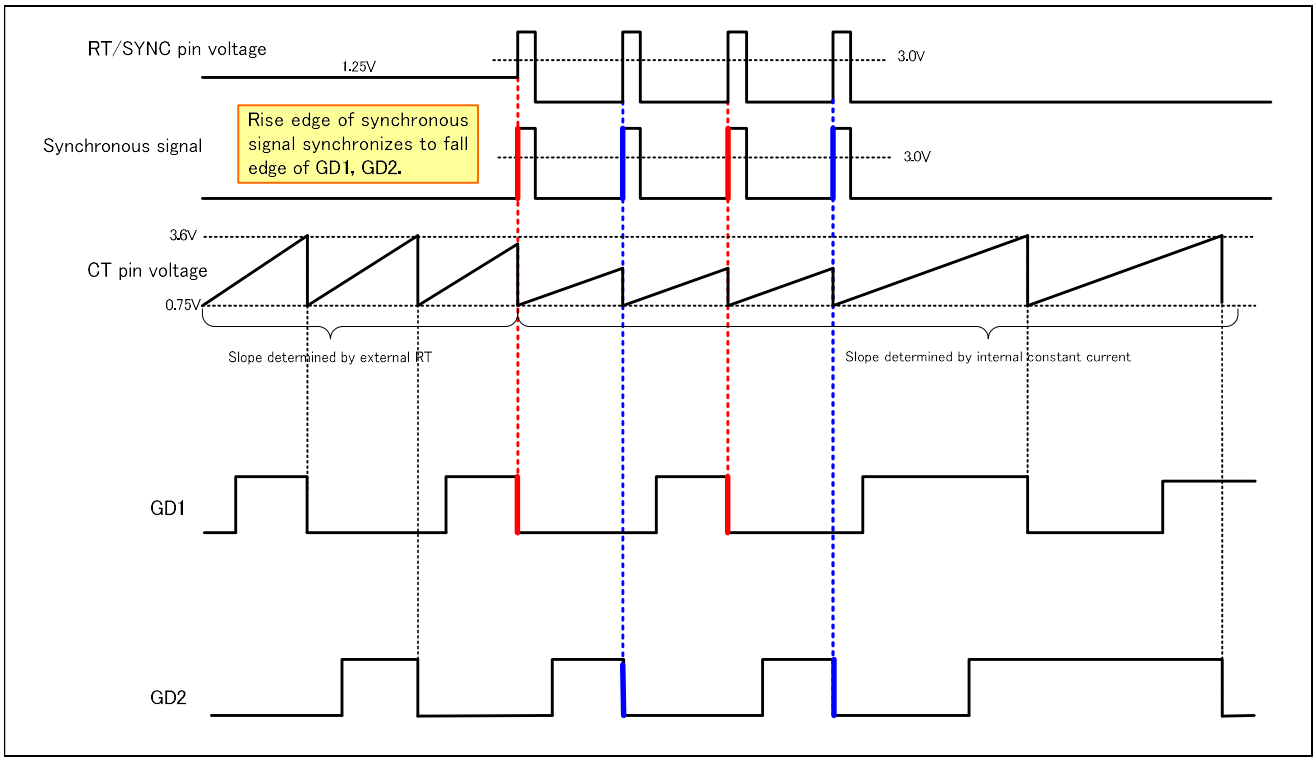


Figure 11 Synchronous Operation

To use synchronous function, please pay attention to the following items.

1) Synchronous signal should not be input when IC stops (Vcc is Low)

2) In case that synchronous circuits are directly connected to RT/SYNC pin, current over the maximum ratings of RT/SYNC pin, 200uA may be applied at startup or switching from normal mode to synchronous mode if the output impedance of synchronous signal circuits is low. (In synchronous mode, the RT/SYNC pin is in high-impedance and, therefore the possibility of current flowing is only at switching into synchronous mode.) In those case, increase of current should be prevented by e.g. inserting a limit resistor or diode as shown below.

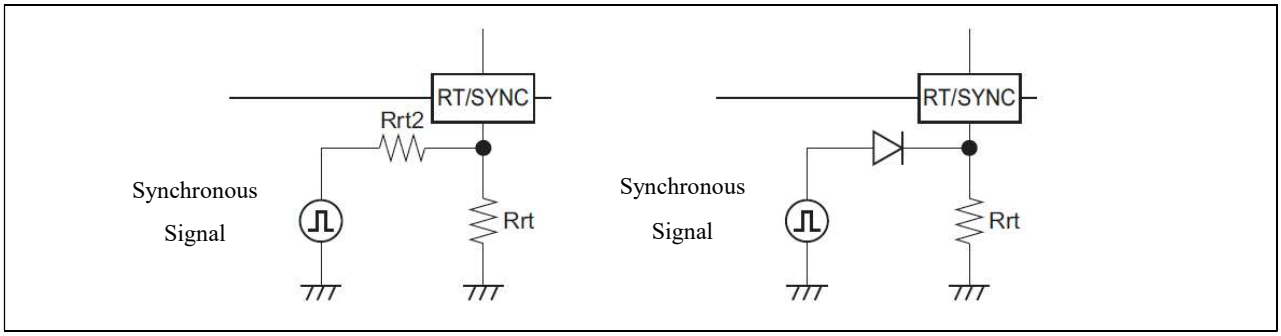


Figure 12 Synchronous Signal Input

3) In synchronous mode, RT/SYNC pin is in high-impedance and may be influenced by noise or negative voltage. For the case, removing noise by RC filter or clamping negative voltage by SBD is required.

4) There is an internal delay between the RT / SYNC pin and the SYNC – O pin, and the phase difference does not become 90 ° if the On Duty of the synchronous signal is 50%. Please adjust the phase difference on the slave side with the On Duty of the synchronization signal.

3.8 Synchronous Output Function

SYNC-O pin provides inverted signal of synchronous signal input to RT/SYNC pin.

3.9 PWM_IN Function

This function is to provide PWM_IN pin at GD1 pin. It enables to use as driver IC with built-in various protection functions for partial switches. This function is available by pulling up PWM_CNTL pin to VREF pin.

Over-current and over-voltage function operate, therefore additional protection circuits are not required.

If the PWM_CNTL and VREF pins are shorted, an error signal continues to be output from the E_OCP pin. If the E_OCP pin is not used, there is no problem with short circuit, but when using it, pull up the PWM_CNTL pin to the VREF pin after 500 µs after VCC is applied.

4. Design Guide

4.1 Boost inductor

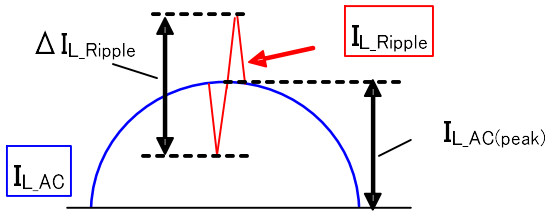
The boost inductor value is determined by an output power and a fixed switching frequency.

A switching frequency must become over 20kHz which is audio frequency to avoid audio noise of an inductor or a input capacitor. Generally it is around 30kHz.

The boost inductor value is obtained by Equation 1 . A conduction loss η input around 0.9.

$$L = \frac{2 \times V_{AC(\min)}^{2} \times (V_{out} - \sqrt{2} \times V_{AC(\min)}) \times \eta \times F_{PFC}}{\gamma \times f_{GD} \times P_{out(\max)} \times V_{out}} \quad (1)$$

$$\gamma = \frac{\Delta I_{L\_Ripple}}{I_{L\_AC(peak)}} \quad (2)$$



Vac(min) : Effective value of minimum input voltage [V(rms)]

Vout : Output voltage[V]

Pout : Maximum output power [W]

η : Efficiency

F_{PFC} : Power Factor

f_{GD} : fixed switching frequency[Hz]

ΔIL_Ripple : Maximum ripple current of Boost inductor.

IL_AC(peak) : Peak current of Boost inductor

4.2 Output capacitor

The necessary capacitor value to guarantee voluntary hold-up time is expressed in the next equation.

$$C_{out}[F] \geq \frac{2 \times P_{out} \times t_{hold}}{V_{out}^{2} - V_{out(min)}^{2}} \quad (3)$$

thold[s] : Hold-up time
Vomin[V] : Minimum output voltage

4.3 Power MOSFET(IGBT), and boost diode

A peak current flowing on a Power MOSFET(IGBT) or a boost diode is expressed in the next equation. A conduction loss η input around 0.9.

$$I_{in} = \frac{P_{OUT}}{V_{AC(\min)} \times \eta \times F_{PFC}} \quad (4)$$

$$I_{L(peak)} = (1 + \gamma/2) \times I_{in} / \sqrt{2} \quad (5)$$

I_{in} : Effective value of Maximum input current.

I_L(peak) : Peak current of Boost inductor

4.4 Operating Frequency

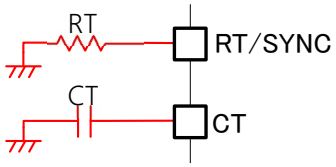
4.4.1 Operating Frequency Setting

The R2A20114BFP operating frequency fGD is determined by adjusting the timing resistor RT (the RT pin) and the timing capacitance CT (the CT pin).

The operating frequency is approximated by the following expression (6). The expression (6) is the formula that was similar so that an error of the whole range of each capacity value and the resistance value of fig.13 is small. Therefore, the calculation result of the expression (6) does not completely accord with the real frequency. Ct and Rt from the expression (6) is used as an initial setting values. More correct value is calculated from the graph in figure 13 or by Excel Calculation Sheet.

$$f_{GD} = \frac{2.5}{R_T \times C_T} \quad (6)$$

f_{GD} : operating frequency [Hz]



It is necessary to select a 7 kΩ or more resistance connected to the RT pin, to limit maximum RT current less than 200uA. Also, use a 100 pF or more capacitor connected to CT pin, to reduce effects from parasitic capacitance and noise.

As a reference, the operating frequency fGD when the timing resistor RT and the timing capacitance CT are changed is shown in the figure 13.

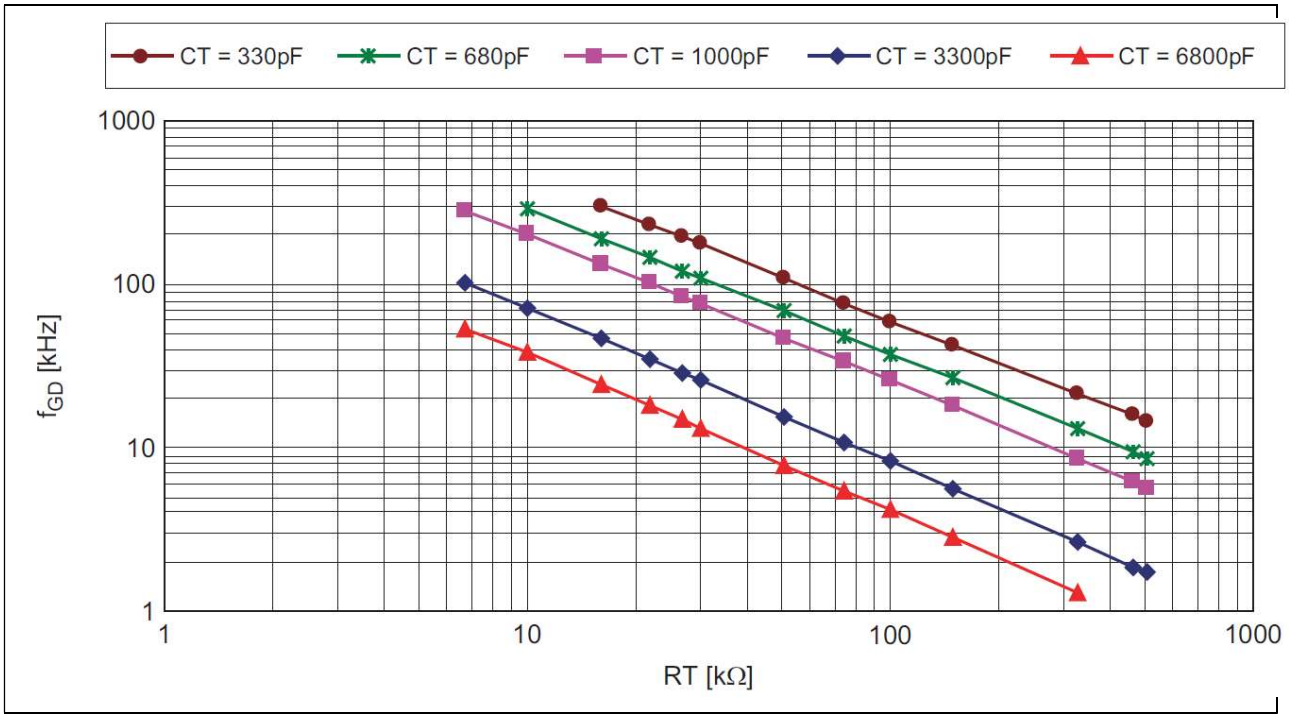


Figure 13 Operating Frequency Characteristics

4.4.2 A method to limit Max. Duty of GD

By the setting of the drive circuit, On Duty becomes a little less than 100% value in zero cross of input voltage for the delay of the MOS gate. As a result, there is the case that the input current of zero cross is not normal like figure 14. When such a waveform occurred, Max Duty is limited by connecting resistance between Vref and CT as figure 16, and an input current waveform is improved.

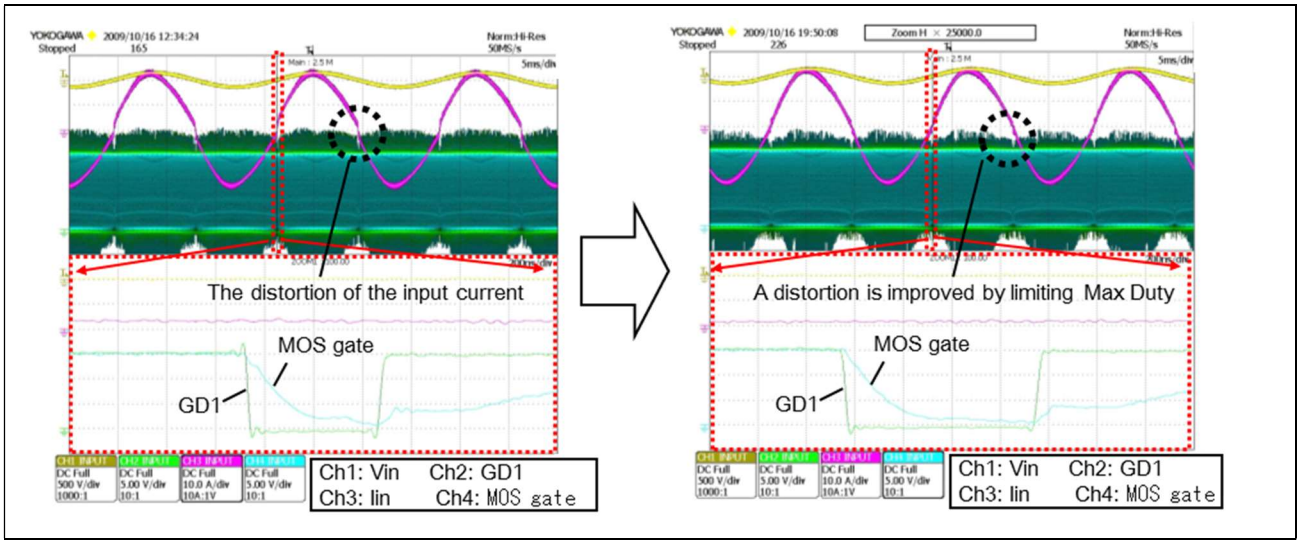


Figure 14 Input current waveform with the distortion at zero cross

Figure 15 Input current waveform after Max. Duty limit

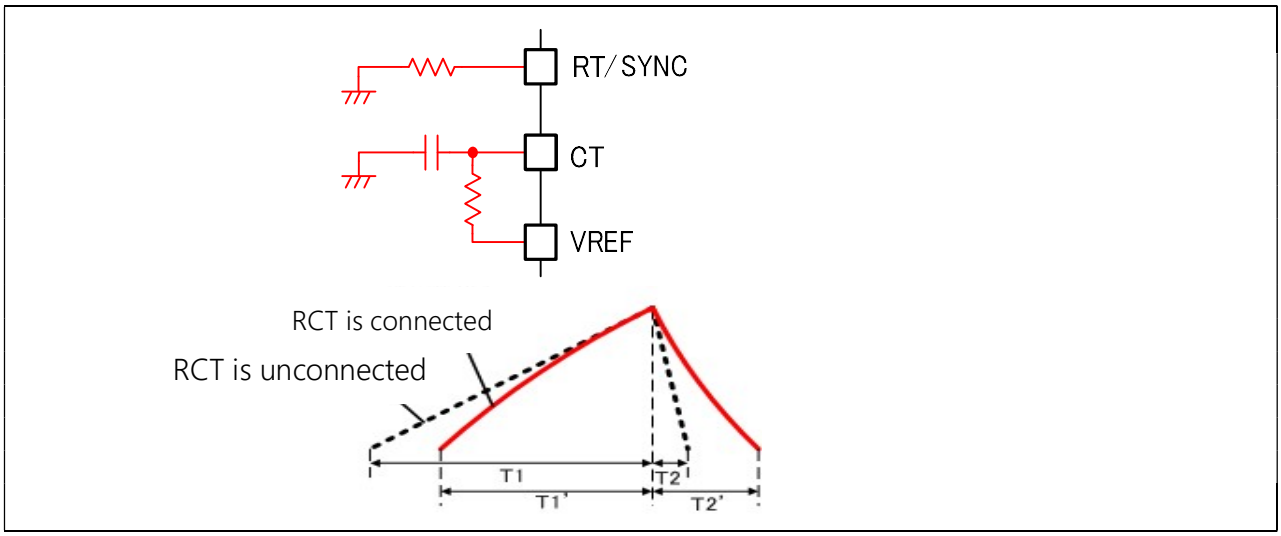


Figure 16 Max. Duty limit circuit

Only adding resistor, however, causes oscillation frequency change. Rt and Ct must be adjusted together.

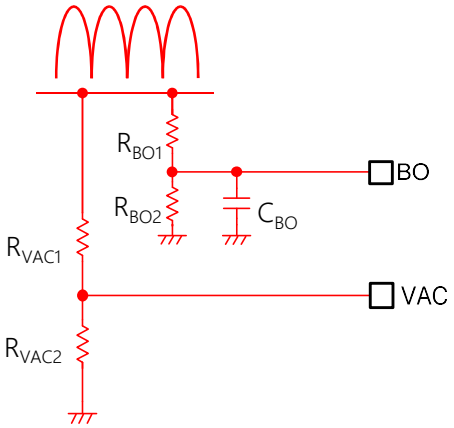
When the fixed number is decided, please decide them with the Excel sheet prepared for.

4.5 Input AC voltage sensing

To turn ON/OFF PFC operation according to input AC voltage, the full-bridge rectification wave is divided by resistors and smoothed by capacitors as expression (12), to apply to BO pin. When PFC ON/OFF is controlled by MCU and is not needed to follow AC voltage, the circuits to apply full-bridge rectifier wave into BO pin are unnecessary. Circuits from full-bridge rectifier wave to VAC pin should be connected.

$$V_{BO} = \frac{2\sqrt{2} \times R_{BO\_2} \times V_{ac}}{\pi \times (R_{BO\_1} + R_{BO\_2})} \quad (12)$$

$$C_{BO} = \frac{1}{2\pi \times f_c \cdot \left(\frac{R_{BO\_1} \times R_{BO\_2}}{R_{BO\_1} + R_{BO\_2}} \right)} \quad (13)$$



Vac : Effective value of minimum input voltage [V(rms)]

f_C : Cutoff frequency [Hz]

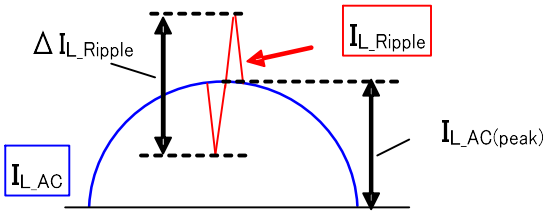
Be sure to apply signal which is full-bridge rectifier wave divided by resistors to VAC pin. First decide OVP2 pin resistors by expression (20) in 4.10.1 and then decide to meet expression (14)

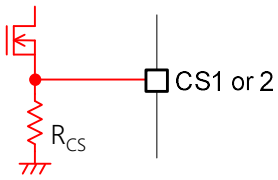
$$\frac{R_{VAC1}}{R_{VAC2}} = \frac{R_{OVP2\_1}}{R_{OVP2\_2}} \quad (14)$$

4.6 Resistor of current sensing

Current sensing resistance is determined within expression (15). Small resistance can reduce the loss by resistors, but the over-current value increase together. Need to pay attention to ratings of power elements.

$$R_{CS} \le \frac{0.6\sqrt{2} \times V_{ac} \times \eta \times F_{PFC}}{Pout \times (2+\gamma)} \quad (15)$$





Vac : Effective value of input voltage [V]

Pout : Maximum output power [W]

η : Efficiency

F_{PFC} : Power Factor

γ : Ripple of boost inductor current

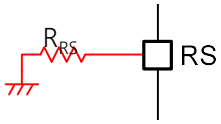
ΔIL_Ripple : Maximum ripple current of Boost inductor [A]

IL_AC(peak) : Peak current of Boost inductor [A]

4.7 Phase Compensation Circuit of Current Amplifier

4.7.1 RS pin

$$R_{RS}[\Omega] = \frac{L \times 10^9}{2.5 \times R_{CS}} \times \frac{R_{ovp2\_2}}{R_{ovp2\_1} + R_{ovp2\_2}} \quad (16)$$



L : Boost inductor [H]

Rcs : Resistor of Current sense [Ω]

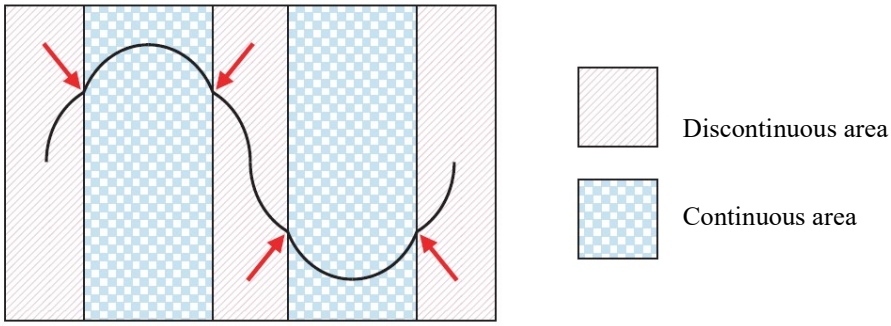
Vout : Output voltage[V]

As expression (16), RS pin resistance is in proportion to boost inductance and it's necessary to pay attention for the case where current superposition characteristics of inductance is large as dust type inductance. The expression (16) is usually calculated by inductance value at maximum current.

RS pin resistance influences AC input current waveform. Generally, in small RS pin resistance the peak point of AC input current wave tends to expand to be triangular wave as a whole, and in large RS pin resistance the peak point becomes flat to be trapezoidal wave. Please use it as a guide to adjust.

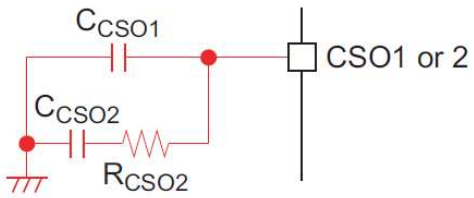
If load regulation deteriorate significantly at maximum load, ON duty may be limited (COMP pin voltage is over 3.8V). Then, adjust by reducing RS pin resistance.

In PFC control, the inductor current becomes discontinuous near zero cross point of AC voltage. This discontinuous area is expanded for smaller boost inductance. This case, at the border line of discontinuous area and continuous area, the following step may be found in AC current. This step damages a fifth harmonic wave.



For the case, reducing RS pin resistance restricts the current rising and improves the step. However too small resistance rises the peak point resulting to a third harmonic wave deterioration. The expression (16) is based on continuous operation and the calculation result will mis-match under long discontinuous area. The resistance may be as small as 1/10 of calculation results in expression (16). Please adjust to be the best harmonic current confirming the input AC current waveform in the actual devices.

4.7.2 CSO pin



CSO1 pin and CSO2 pin determine the current loop characteristics in PFC control. The current loop is important to shape the AC input current to the sine wave similar to the AC input voltage. Please adjust the following characteristics by Excel fixed values calculation sheet prepared for.

Current loop frequency characteristics should have set below conditions.

- It has enough gain at twice of AC input frequency.

・It has enough lower gain at switching frequency.

・It has enough phase margin

As a recommendation,

・Over 40 dB at twice of AC input frequency

・Set zero cross frequency of current loop around 1/10 of switching frequency.

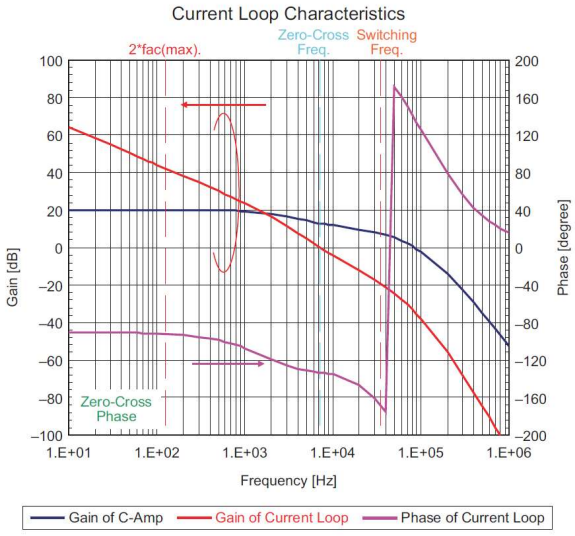
・Around -30 dB at switching frequency

・60 degrees or more phase margin

Although it's difficult to meet all conditions, please adjust as possible as it's satisfied.

Parts at CSO pin influence the waveform and stability of AC input current. For unstable AC input current, larger Ccso2 usually makes inductor current stable but increases distortion of AC input current waveform.

The same values of external parts should be used for CSO1 and CSO2 pins.

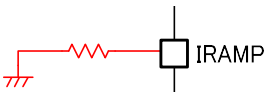


4.8 Resistor of IRAMP pin

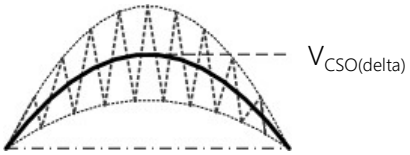
The Riramp must be adjusted to be able to output max power with the minimum input voltage. The Riramp is approximated by the expression (17) on the condition that it is operated with CCM in the minimum input voltage and the max power. The calculation by the expression is just approximation. For more accurate values, please use Excel fixed value calculation sheet prepared for. Larger Riramp deteriorates load regulation and smaller value causes current waveform distortion.

Please adjust it, confirming the output voltage and input current waveform.

$$R_{IRAMP}[\Omega] = 4\times10^{9}\times\left(\frac{\sqrt{2}\times V_{AC(\min)}}{V_{OUT}\times f_{GD}} - 2\times10^{-6}\right)\times\frac{1}{V_{CSO(delta)}} \quad (17)$$

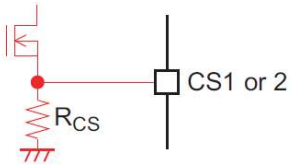


$V_{CSO(delta)}$: Peak voltage of the CSO pin [V]



The Vcso(delta) is the voltage which smooths the voltage waveform similar to inductance current which is addition of MOS current detected at CS pin and diode current calculated internally in the IC. It's expressed as (18)

$$V_{CSO(delta)}\ [V] = \frac{4.5\sqrt{2}\times P_{out}\times R_{cs}}{V_{AC}\times\eta} \quad (18)$$

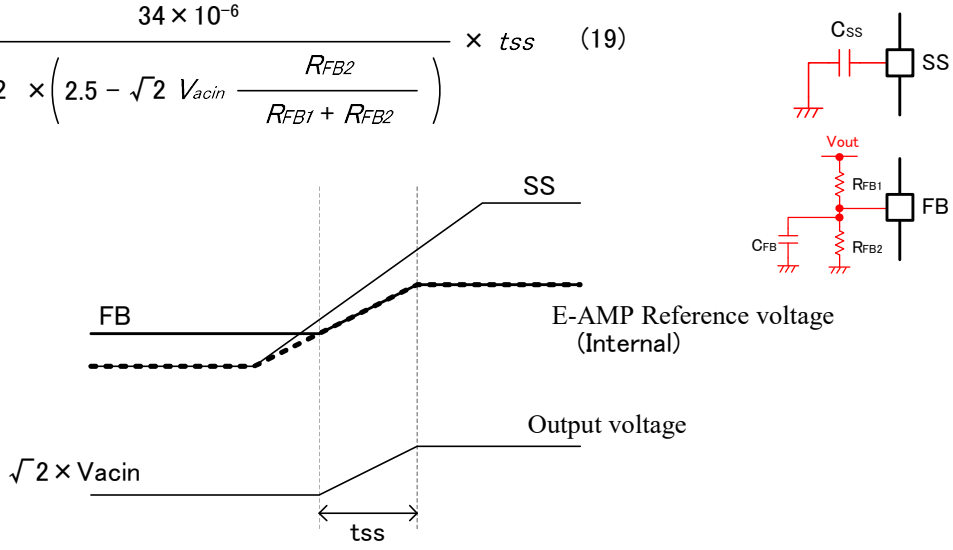


4.9 Capacitor of Soft-start

If PFC circuits does not operate at AC voltage Vacin input, the output voltage of PFC circuits is $\sqrt{2} \times$ Vacin. To set the time from PFC starting operation from the voltage to SS pin reaching the defined output voltage, the capacitance Css required to SS pin is calculated in expression (19).

Startup time varies depending on load or input/output conditions, adjust Css under the actual operation after determining the reference value by the calculation.

$$C_{SS} = \frac{34 \times 10^{-6}}{1.272 \times \left(2.5 - \sqrt{2}\, V_{acin} \dfrac{R_{FB2}}{R_{FB1} + R_{FB2}} \right)} \times tss \qquad (19)$$

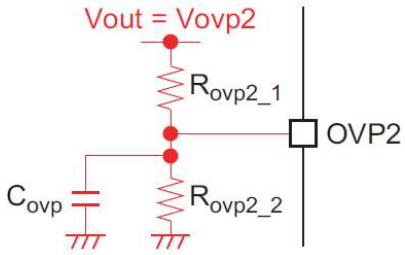


4.10 Protection Functions

4.10.1 OVP2 voltage setting

FB pin has OVP function but may continue normal control operation even if the voltage dividing resistors at FB pin are halfway destroyed to be abnormal resistance values. This case, the FB pin is doing normal control operation and the OVP function at FB pin can't detect the abnormality. OVP2 pin monitors output voltage via another resistors than FB pin and can detect such an abnormality.

$$V_{OVP2}\,[V] = \frac{R_{ovp2\_1} + R_{ovp2\_2}}{R_{ovp2\_2}} \times 2.5 \times 1.08 \qquad (20)$$



After setting the divided resistance at OVP2 pin, set the resistance at VAC pin from the expression (14).

$$\frac{R_{VAC1}}{R_{VAC2}} = \frac{R_{OVP2\_1}}{R_{OVP2\_2}} \qquad (14)$$

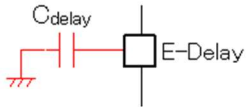
OVP2 pin voltage is used as a control signal internally in the IC, voltage corresponding to the output voltage should be applied. If OVP2 function is not used, short-circuit the FB pin and OVP2 pin.

4.10.2 E-DELAY setting

The time between entering OCP status to E_OCP signal output, tdelay is set.

If E_OCP signal output is not required when OCP continues, short-circuit E-DELAY pin to GND.

$$C_{delay}[F] = \frac{36 \times 10^{-6}}{2.45} \times t_{delay} \quad (21)$$

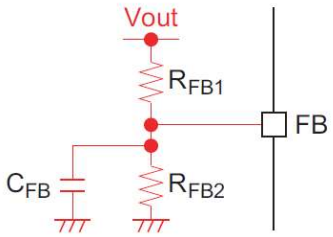


4.11 Output Voltage Setting and Frequency Characteristics of Voltage Amp.

4.11.1 Output voltage setting

R2A20114BFP is feedback controlled so that FB pin is around 2.5V at all times and the output voltage is controlled to be a constant value. The output voltage is determined by voltage dividing resistors at FB in.

$$V_{OUT} = \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \times 2.5 \quad (22)$$

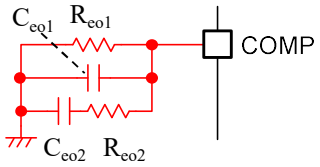


4.11.2 COMP parameter setting

Voltage and current amplifier are transconductance (gm) amplifier. It does not need to feedback for input side. Therefore, it is possible to minimize influence on input circuit by feedback circuit. Gain of gm amplifier is calculated by product of transconductance and output impedance in (23). Gm-v is transconductance of voltage amplifier. Rvo is output resistor of voltage amplifier itself.

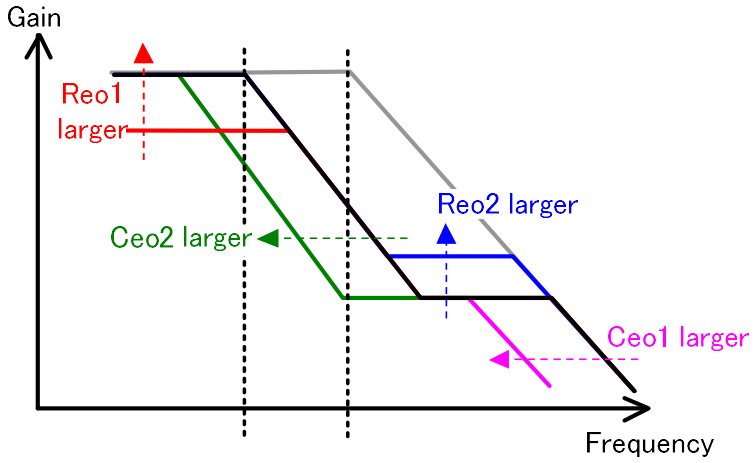
As CSO pin, please use Excel fixed value calculation sheet for COMP pin also.

$$G_V = G_{m-v} \cdot \frac{1}{\frac{1}{R_{vo}} + \frac{1}{R_{eo1}} + j\omega C_{eo1} + \frac{1}{R_{eo2} + \frac{1}{j\omega C_{eo2}}}} \quad (23)$$



Gm-v : transconductance of voltage amplifier [S]

Rvo : output resistance of voltage amplifier [Ω]



Comp pin determines voltage loop characteristics in PFC control. The voltage loop characteristics is relating to output voltage control and influences on ripple characteristics of output voltage, load regulation, response characteristics and stability.

Voltage loop frequency characteristics should be

- It has enough lower gain at twice of AC input frequency.
- Zero-cross frequency is lower than AC input frequency
- It has enough phase margin.

As a recommendation,

- Over -30 dB at twice of AC input frequency
- 60 degrees or more phase margin.

Some characteristics conflict and it's difficult to meet all conditions. Please adjust as possible as they're satisfied.

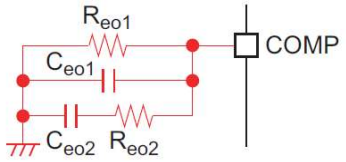
These parameters influence the following characteristics.

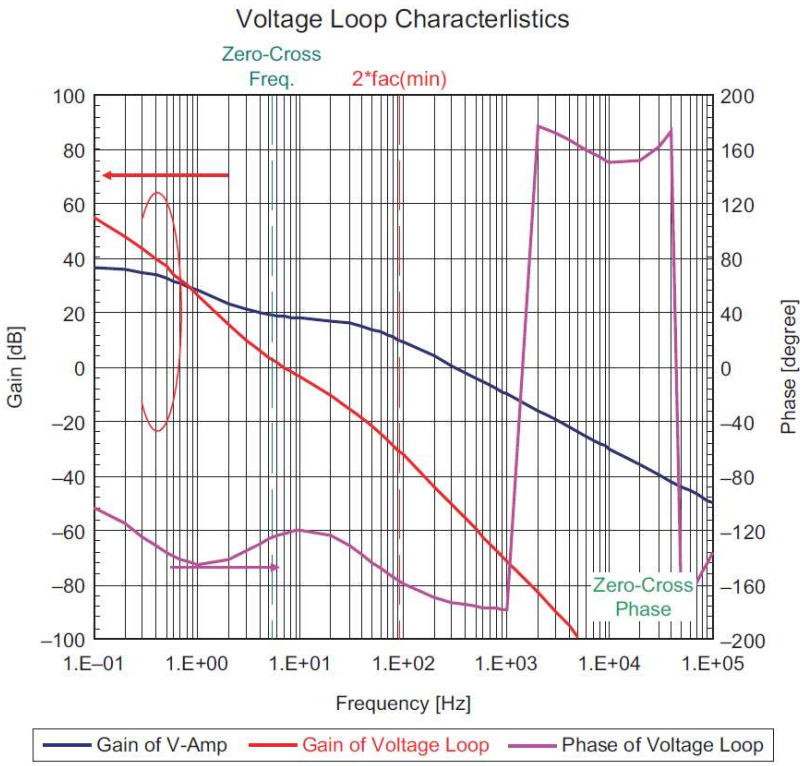
Reo1 determines load regulation of output voltage. Smaller resistance increases output voltage change.

In Ceo1, the gain of the frequency twice of AC frequency influences output voltage ripple. Lower gain reduces ripple. Larger Ceo1 reduces the gain, but the response characteristics of the output voltage becomes worse.

Reo2 and Ceo2 make zero to keep phase margin.

These recommendations are just for reference. Operation should be checked in actual power supply devices. Adjust for the required performance by confirming the operation in an actual devices.





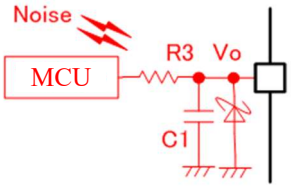
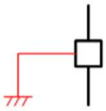
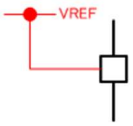
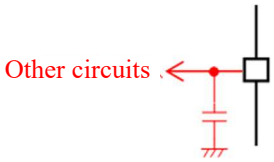
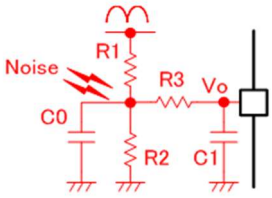
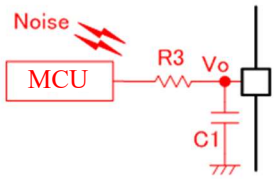
4.11.3 PFC boost voltage setting

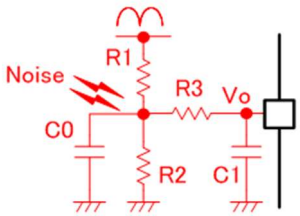
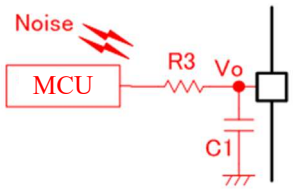
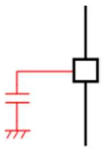
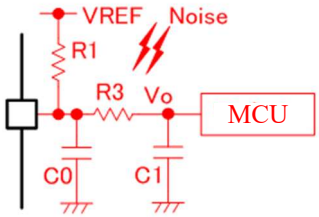
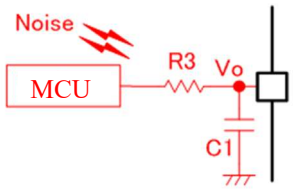
Output voltage can be changed for V_CNTL pin voltage. The output voltage is calculated by the expression (24) by V_CNTL pin voltage.

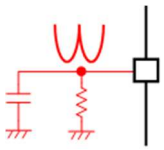
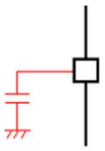
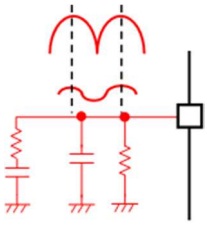
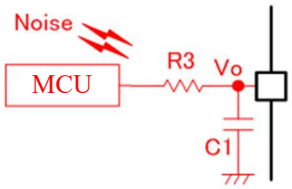
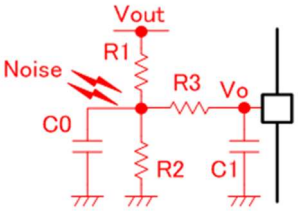
$$V_{OUT} = \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \times \left(2.5 - \frac{V_{V\_CNTL}}{4} \right) \qquad (24)$$

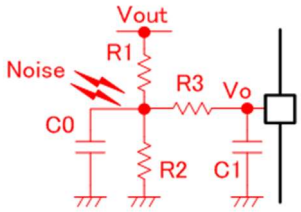
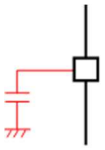
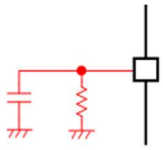
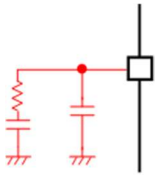
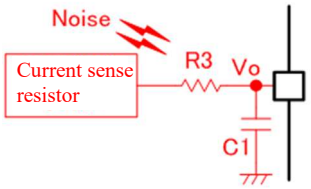
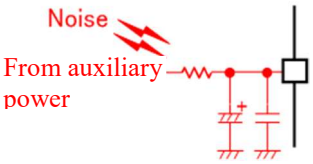
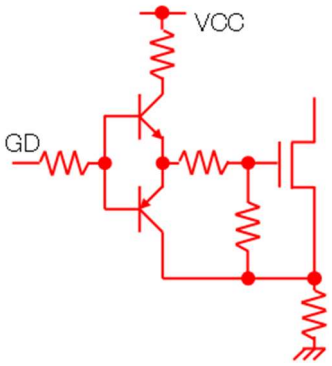
4.12 Treatment of Each Pin

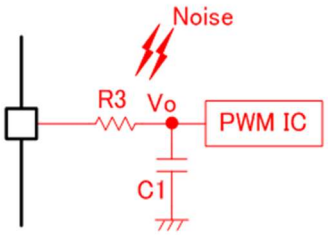
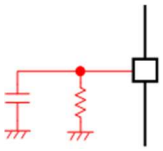
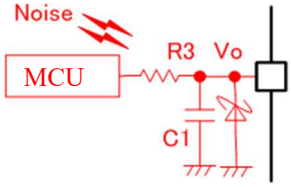
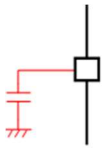
Input pins of the IC is usually in high-impedance and may be influenced by noise or overshoot/undershoot of input signals. Some output pins require decoupling capacitors for stable operation. The followings describes example setting and point to be attended of each pin. These are for just reference, and it's necessary to confirm by actual devices.

Pin no.	Pin Name	Example setting	Cautions
1	PWM_IN		Long wiring of PWM_IN signal may cause damage by overshoot, undershoot and noise. Remove unnecessary components by RC filter or SBD.
2	PWM_CNTL	PWM_IN used  PWM_IN not-used 	When PWM_IN function is not used, pull-down to GND. When PWM_IN function is used, pull-up to VREF. Please also refer to P.14.
3	VREF		Since VREF pin is the source of reference voltage in the IC, 0.1uF or more decoupling capacitor should be connected. The decoupling capacitor is connected to AGND pin as close as possible. It's possible to use as voltage source to surrounding circuits but the load should not exceed 10mA.
4	BO	ON/OFF by AC voltage  ON/OFF from MCU 	BO pin turns ON/OFF gate pulse and the malfunction by noise causes omissions in the gate pulse. In case of ON/OFF corresponding to AC voltage, set the cut off frequency of detecting circuits R1, R2 and C0 to be about 1/10 of AC frequency to reject ripple in AC frequency. If the detecting circuit can' t be placed near the IC, add RC filter R3 and C1 whose cut off frequency is about 1/10 of switching frequency to the pin directly to avoid switching noise onto the long wiring. In case of using only ON/OFF functions from MCU signals, also add RC filter R3 and C1 whose cut off frequency is about 1/10 of switching frequency to the pin directly to avoid switching noise.

Pin no.	Pin Name	Example setting	Cautions
5	VAC		Set the detecting circuit R1, R2, C0 between full-bridge rectifier wave and VAC pin to have cutoff frequency which is 20 times of AC frequency to minimize distortion and phase shift. Normally, this detecting circuit filters switching noise but RC filter R3 and C1 whose cut off frequency is about 1/10 of switching frequency may be added to the pin directly if necessary in such a case of long wiring from the detecting circuit. Set the ratio of R1/R2 to be the same as resistance ratio in detecting circuit at OVP2 pin.
6	PD		If necessary, RC filter R3 and C1 whose cut off frequency is about 1/10 of switching frequency may be added to the pin directly when PD function is used by MCU control signal.
8	E-DELAY		Connect a capacitor to the pin as close as possible.
9 10 11	E_OCP E_OVP E_PHASE		E_OCP, E_OVP, E_PHASE pins are open drain and require pull-up resistor R1 if used. Adding capacitor C0 can decrease the sensitivity of E_OCP, E_OVP, E_PHASE signals. In receiving signal by MCU, they have influence of switching noise caused by long wiring. If necessary, RC filter R3 and C1 whose cut off frequency is about 1/10 of switching frequency may be added directly to the MCU.
12	OFF		If necessary, RC filter R3 and C1 whose cut off frequency is about 1/10 of switching frequency may be added to the pin directly when OFF function is used by MCU control signal.

Pin no.	Pin Name	Example setting	Cautions
13	RS		RS pin provides voltage which is 1/5 of the difference between OVP2 pin voltage and VAC pin voltage. Since the output voltage waveform is like upside down of full-bridge rectifier waveform, set the cut off frequency to be about 20 times of AC frequency to minimize distortion and phase shift.
14	SS		Adjust the capacitance according to the required startup time of the PFC circuits.
15	COMP		Refer to 4.11.2 for the setting. The ripple voltage and the phase at COMP pin influences the harmonic current. This COMP pin circuits determines the frequency characteristics of FB pin and the frequency characteristics of voltage amp, and also determines the ripple voltage and the phase of COMP pin. Smaller ripple voltage and smaller phase shift to AC cycle improve the harmonic current.
16	V_CNTL		If necessary, RC filter R3 and C1 whose cut off frequency is about 1/10 of switching frequency may be added to the pin directly when V_CMTL function is used by DC signal from MCU. When V_CNTL function is used by PWM signal from MCU, DC voltage is input to V_CNTL pin. Then, add RC filter R3 and C1 to the pin directly to smooth PWM signal from MCU.
17	FB		Ratio of R1 and R2 determines the output voltage. Adjust the cut off frequency of detecting circuit R1, R2, C0 between output voltage to FB pin so that the phase of ripple voltage of COMP pin matches the phase of AC cycle. Normally, this detecting circuit filters switching noise but RC filter R3 and C1 whose cut off frequency is about 1/10 of switching frequency may be added to the pin directly if necessary in such a case of long wiring from the detecting circuit.

Pin no.	Pin Name	Example setting	Cautions
18	OVP2		The frequency characteristics of detecting circuit between output voltage and OVP2 pin is made to equivalent to those of FB pin. The ratio of R1/R2 is set according to the over voltage level to be detected. The resistance ratio of VAC pin is adjusted to be the same as this resistance ratio.
20	TIMER		Connect a capacitor to the pin as close as possible.
21	IRAMP		Voltage which is about 1/5 of COMP pin voltage is output at IRAMP pin. Set the cut off frequency nearly equal to the switching frequency.
22 23	CSO2 CSO1		Refer to 4.7.2 for the setting.
24 25 26 27	CS2 CS2_GND CS1_GND CS1		Between current detection resistor and CS pin, add RC filter whose cut off frequency is about 1/10 to 1/3 of the switching frequency to the pin directly. CS* pins and CS*_GND pins are connected to the resistors of current detection in a separate wiring.
28	VCC		Noise from auxiliary power may cause unstable operation. In such a case, adding RC filter to the pin directly may have effect to reject the noise for stable operation.
32 34	GD2 GD1		When driver circuit is added, place near the switching elements.

Pin no.	Pin Name	Example setting	Cautions
36	SYNC-O		Switching noise may be applied by wiring when a PWM-IC in the next stage or MCU receives the signal. If necessary, RC filter R3 and C1 whose cut off frequency is about 1/10 of noise frequency may be added directly to the PWM-IC or MCU.
37	RT/SYNC	Self-oscillating operation  Synchronous operation 	In normal operation, 1.25V voltage is output at RT/SYNC. If necessary construct RC filter whose cut off frequency is 1/10 of switching frequency. In synchronous operation, RT/SYNC pin is in high impedance, influenced by overshoot, undershoot and noise due to synchronous signals wiring. Remove unnecessary components by RC filter or SBD.
38	CT		Connect a capacitor to the pin as close as possible.

4.13 Unused Pins

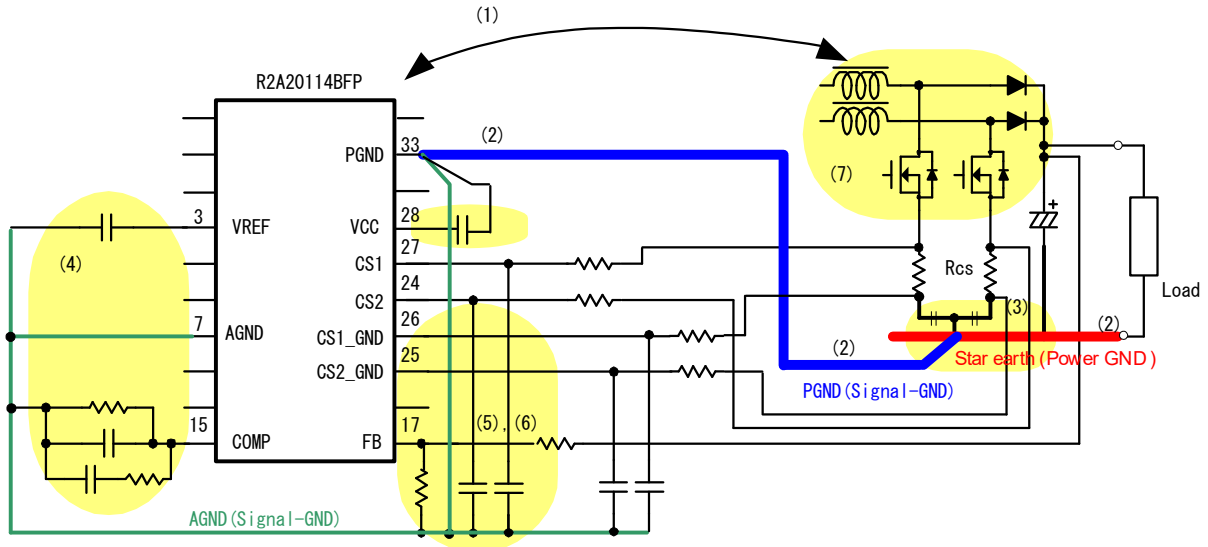
Unused pins in R2A20114BFP is connected as follows. All pins except the table below are used.

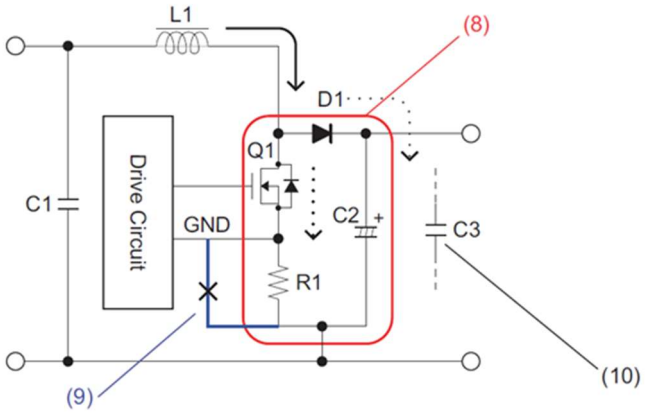
Pin No.	Pin Name	Connection when unused
1	PWM_IN	GND
2	PWM_CNTL	GND
4	BO	VREF
6	PD	GND
8	E-DELAY	Open: when E_OCP is used. GND: when E_OCP is not used.
9,10,11	E_OCP,E_OVP,E_PHASE	Open
12	OFF	GND
14	SS	Open
36	SYNC-O	Open
-	N.C.	Open

4.14 Notice for PCB Layout

The followings are notices for PCB layout.

1. Please make sure PFC IC be located as apart from power stage (MOSFET, DIODE, Boost L) as possible. Specially be careful to MOSFET drain line layout to avoid radiation noise.
2. Please separate Power-GND and Signal-GND pattern surely and connect possibly near to the IC. The pattern for Power-GND is widely from output CAP to PGND. And place the capacitor between Vcc and AGND.
3. The pattern for resistance RCS of current detection is made an even phase as short as possible, and connect it under the output CAP.
4. COMP/VREF external parts are placed as close to the IC pins as possible.
5. The filters for CS1, CS2 are placed as close to the IC as possible to avoid radiation noise. CS1, C1_GND, CS2, CS2_GND lines are connected directly to resistance RCS of current detection in separate wiring.
6. The FB resistor is placed as close to the IC as possible to avoid radiation noise.
7. The pattern for power stage (MOSFET, DIODE, Boost L) parts is shortened as much as possible.
8. For discontinuous current flowing lines, wide and short pattern restricts overshoot of power MOS drain voltage.
9. GND of drive circuit is connected to the source of power MOS (Q1). GND current is separated into large current for power circuit and small current for drive circuit.
10. When switching ripple voltage of output is too large, film capacitor C3 is added near the diode (D1). Select a film capacitor of good high frequency characteristics.





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Revision History <revision history,rh>

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Nov.07,2016	-	New
2.00	July.25.2017	P.11 etc.	Writing error correction

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