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M16C/26A, M16C/28, M16C/29 Group

Procedure to Set PLL Clock as CPU Clock Source

1. Abstract

This document describes how to set the PLL clock as the CPU clock source.

The sample program is an example when the operating voltage is 5 V and the frequency applied to the XIN pin is 10 MHz.

2. Introduction

The application example described in this document is applied to the following MCUs and parameter(s):
MCUs: M16C/26A, M16C/28, M16C/29 Group

This program can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the M16C/26A, M16C/28, and M16C/29 Group MCUs. Check the manual for any additions and modifications to functions. Careful evaluation is recommended before using this application note.

3. Example Description

The PLL clock is the main clock multiplied with the PLL frequency synthesizer.

(The PLL clock in the sample program is the main clock multiplied by 2 to use as a CPU clock source.)

Multiplying the main clock frequency of 10 MHz by 2 will yield the PLL clock frequency of 20 MHz.

Table 1 lists the PLL Clock Configuration Table.

Table 1 PLL Clock Configuration Table

XIN (MHz)	PLC02	PLC01	PLC00	Multiplication Ratio	PLL Clock (MHz) ⁽¹⁾
10	0	0	1	2	20
5	0	1	0	4	

NOTE:

1. $10 \text{ MHz} \leq \text{PLL clock frequency} \leq 20 \text{ MHz}$

Figure 1 shows the Flowchart to Set PLL Clock as CPU Clock Source.

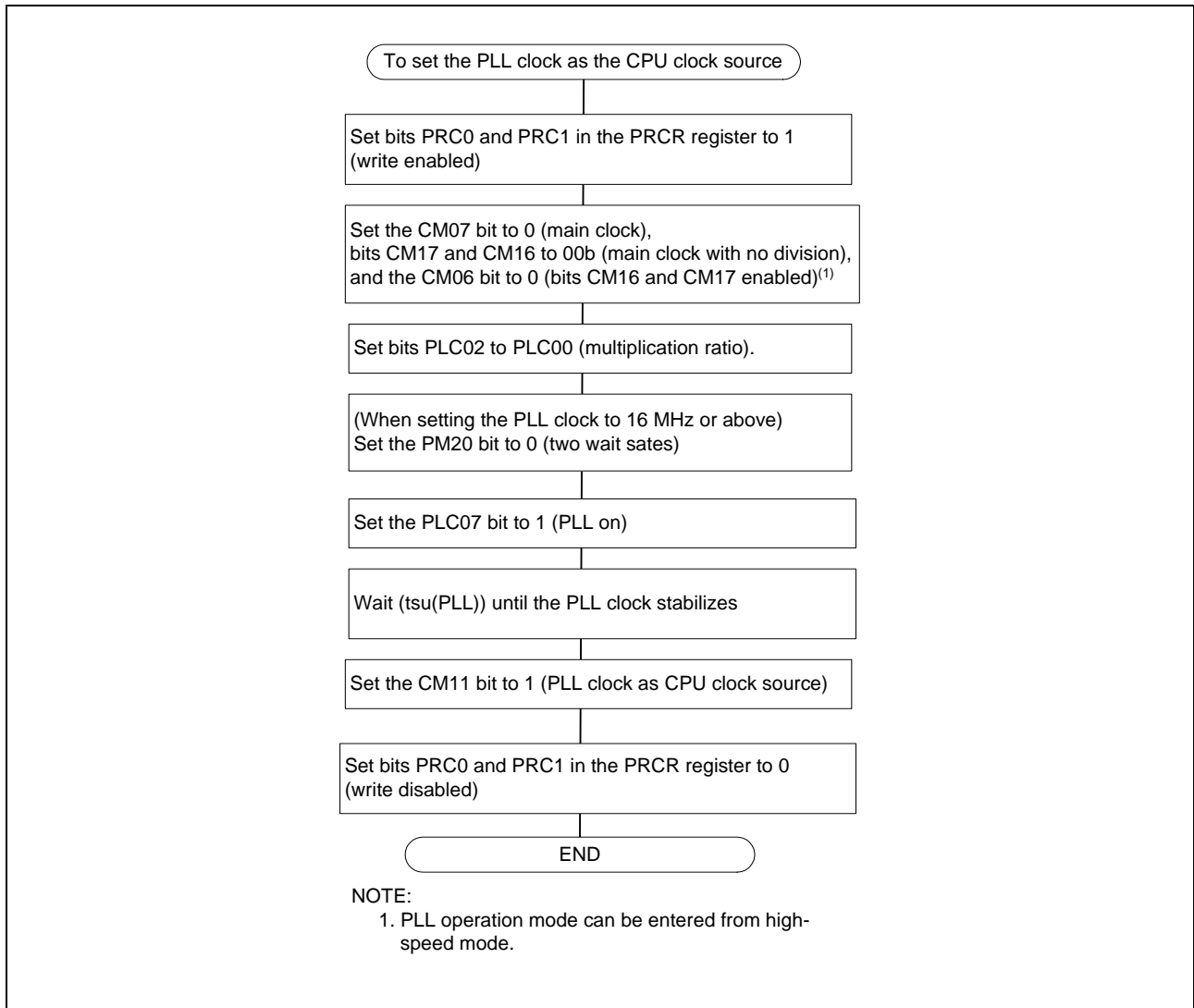


Figure 1 Flowchart to Set PLL Clock as CPU Clock Source

2. Sample Programming Code

A sample program can be downloaded from the Renesas Technology website.
For download, click “Application Notes” in the left-hand side menu of the M16C Family page.

3. Reference Documents

Hardware Manuals

M16C/26A Group Hardware Manual

M16C/28 Group Hardware Manual

M16C/29 Group Hardware Manual

The latest versions can be downloaded from the Renesas Technology website.

Technical Update/Technical News

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REVISION HISTORY	M16C/26A, M16C/28, M16C/29 Group Procedure to Set PLL Clock as CPU Clock Source
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