# RX65N/RX651 Group RX210 Group

## Points of Difference Between RX651 Group and RX210 Group

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## Introduction

This application note is intended as a reference for confirming the points of difference between the overview of functions, the I/O registers, the pin functions of the RX651 Group and RX210 Group, and notes on migration.

Unless specifically otherwise noted, the information in this application note applies to the 144-/145-pin package version of the RX651 Group and the 144-/145-pin package (chip version B) version of the RX210 Group. To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the user's manuals of the products in question.

## Target Devices

- RX651 Group (products with code flash memory capacity of 1 MB or less)
- RX210 Group

Note: Products with code flash memory capacity exceeding 1.5 MB are not included in the comparison.

## Contents

# 1. Comparison of Functions of RX651 Group and RX210 Group

A comparison of the functions of the RX651 Group and RX210 Group is provided below. For details of the functions, see section 2, Comparative Overview of Functions and section 5, Reference Documents.

Table 1.1 is a Comparison of Functions of RX651 and RX210.

**Table 1.1 Comparison of Functions of RX651 and RX210**

| Function | RX210 | RX651 |
|---|---|---|
| CPU | △ | |
| Operating modes | △ | |
| Reset | ○ | |
| Option Setting Memory | △ | |
| Voltage Detection Cirecuit (LVDA) | △ | |
| Clock Generation Circuit | △ | |
| Clock Acuracy Measurement Circuit (CAC) | △ | |
| Low Power Consumption | △ | |
| Battery Backup Function | × | ○ |
| Register Write ProtectionFunction | △ | |
| Exception Handling | △ | |
| Interrupt Controller (ICUa): RX210, (ICUB): RX651 | △ | |
| Buses | △ | |
| Memory Protection unit (MPU) | × | ○ |
| DMA Cotroller (DMACA): RX210, (DMACAa): RX651 | △ | |
| EXDMA Controller (EXDMACa) | × | ○ |
| DataTransfer Controller (DTCa): RX210, (DTCb): RX651 | △ | |
| Event Link Controller (ELC) | △ | |
| I/O Ports | △ | |
| Multi Fucntion Pin Controller (MPC) | △ | |
| Multi-Function Timer Pulse Unit 2 (MTU2a) | ○ | × |
| Multi-Function Timer Pulse Unit 3 (MTU3a) | × | ○ |
| Port Output Enable 2 (POE2a) | ○ | × |
| Port Output Enable 3 (POE3a) | × | ○ |
| 16-Bit Timer Pulse Unit (TPUa) | △ | |
| Programmable Pulse Generator (PPG) | × | ○ |
| 8-Bit Timer (TMR) | △ | |
| Compare Match Timer (CMT) | ○ | |
| Compare Match Timer W (CMTW) | × | ○ |
| Real Time Cock (RTCb): RX210, (RTCd): RX651 | △ | |
| Watchdog Timer (WDTA) | △ | |
| Indepentent Watchdog Timer (IWDTa) | △ | |
| USB2.0 FSHost/Function Module (USBb) | × | ○ |
| Serial Communication Interface (SCIc, SCId): RX210<br>Serial Communication Interface (SCIg, SCIi, SCIh): RX651 | △ | |
| I²C-bus Iterface (RIIC): RX210, (RIICa): RX651 | △ | |
| CAN Module (CAN) | × | ○ |
| Serial Peripheral Interface (RSPI): RX210, (RSPIc): RX651 | △ | |
| Quad Serial Peripheral Interface (QSPI) | × | ○ |
| CRC Caluculator (CRC): RX210, (CRCA): RX651 | △ | |
| SD Host Interface (SDHI) | × | ○ |
| SD Slave Interface (SDSI) | × | ○ |
| Multi Media Card Interface (MMCIF) | × | ○ |

| Function | RX210 | RX651 |
|---|---|---|
| Parallel Data Capture Unit (PDC) | × | ○ |
| Boundary Scan | × | ○ |
| AESa | × | ○ |
| RNGa | × | ○ |
| 12-bit A/D Converter (S12ADb): RX210, (S12ADFa): RX651 | △ | |
| D/A Converter (DA): RX210, 12-bit D/A Converter (R12DA): RX651 | △ | |
| Temperature Sensor (TMPSa): RX210, (TMPS): RX651 | △ | |
| Comparator A (CMPA) | ○ | × |
| Comparator B (CMPB) | ○ | × |
| Data Operation Circuit (DOC) | △ | |
| RAM | △ | |
| Standby RAM | × | ○ |
| Flash Memory (Code Flash) | △ | |
| Flash Memory (E2 Data Flash) | ○ | × |

Note: ○: Function implemented, ×: Function not implemented, △: Differences exist between implementation of function on RX210 and RX651.

# 2. Comparative Overview of Functions

## 2.1 CPU

Table 2.1 shows a Comparative Listing of CPU Specifications, and Table 2.2 shows a Comparative Listing of CPU Registers.

**Table 2.1 Comparative Listing of CPU Specifications**

| Item | RX210 | RX651 |
|---|---|---|
| CPU | • Maximum operating frequency: 50 MHz<br>• 32-bit RX CPU<br>• Minimum instruction execution time: One instruction per state (cycle of the system clock)<br>• Address space: 4-Gbyte linear<br>• Register set of the CPU<br>General purpose: Sixteen 32-bit registers<br>Control: Eight 32-bit registers<br>Accumulator: One 64-bit register<br>• Basic instructions: 73<br>• DSP instructions: 9<br>• Addressing modes: 10<br>• Data arrangement<br>Instructions: Little endian<br>Data: Selectable as little endian or big endian<br>• On-chip 32-bit multiplier: 32 x 32 → 64 bits<br>• On-chip divider: 32 / 32 → 32 bits<br>• Barrel shifter: 32 bits | • Maximum operating frequency: 120 MHz<br>• 32-bit RX CPU (RXv2)<br>• Minimum instruction execution time: One instruction per state (cycle of the system clock)<br>• Address space: 4-Gbyte linear<br>• Register set of the CPU<br>General purpose: Sixteen 32-bit registers<br>Control: Ten 32-bit registers<br>Accumulator: Two 72-bit registers<br>• Basic instructions: 75<br>• Floating-point instructions: 11<br>• DSP instructions: 23<br>• Addressing modes: 11<br>• Data arrangement<br>Instructions: Little endian<br>Data: Selectable as little endian or big endian<br>• On-chip 32-bit multiplier: 32 x 32 → 64 bits<br>• On-chip divider: 32 / 32 → 32 bits<br>Barrel shifter: 32 bits<br>• Memory protection unit (MPU) |
| FPU | | • Single precision (32-bit) floating point<br>• Data types and floating-point exceptions in conformance with the IEEE754 standard |

**Table 2.2 Comparative Listing of CPU Registers**

| Register | Bit | RX210 | RX651 |
|---|---|---|---|
| FPSW | — | — | Floating-point Status Word |
| EXTB | — | — | Exception Table Register |
| ACC | | ACC: 64-bits (DSP, multiply and multiply-and-accumulate) | ACC0: 72-bits (DSP, multiply and multiply-and-accumulate)<br>ACC1: 72-bits (DSP) |

## 2.2 Operating Modes

Table 2.3 shows a Comparative Listing of Operating Modes Specifications, and Table 2.4 shows a Comparative Listing of Operating Modes Registers.

**Table 2.3 Comparative Listing of Operating Modes Specifications**

| Item | RX210 | RX651 |
|---|---|---|
| Operating modes specified by mode setting pins | Single-chip mode | Single-chip mode |
| | Boot mode | Boot mode (SCI interface) |
| | — | Boot mode (USB interface) |
| | User boot mode | — |
| | — | Boot mode (FINE interface) |
| Operating modes specified by register settings | Single-chip mode | Single-chip mode |
| | User boot mode | — |
| | On-chip ROM disabled extended mode | On-chip ROM disabled extended mode |
| | On-chip ROM enabled extended mode | On-chip ROM enabled extended mode |

**Table 2.4 Comparative Listing of Operating Modes Registers**

| Register | Bit | RX210 | RX651 |
|---|---|---|---|
| MDSR | — | Mode Status Register | — |
| SYSCR1 | SBYRAME | — | Standby RAM Enable (b7) |
| | | The Value after reset is different. | |

## 2.3 Option-Setting Memory

Table 2.5 shows a Comparative Listing of Option-Setting Memory Registers.

**Table 2.5 Comparative Listing of Option-Setting Memory Registers**

| Register | Bit | RX210 | RX651 |
|---|---|---|---|
| SPCC | — | — | Serial Programmer Command Control Register |
| OSIS | — | — | OCD/Serial Programmer ID Setting Register |
| OFS0 | IWDTCKS[3:0] | IWDT Clock Frequency Division Ratio Select | IWDT-Dedicated Clock Frequency Division Ratio Select |
| | IWDTRSTIRQS | IWDT Reset Interrupt Request Select<br><br>0: Non-maskable interrupt request is enabled<br><br>1: Reset is enabled | IWDT Reset Interrupt Request Select<br><br>0: Non-maskable interrupt request or plain interrupt request is enabled<br><br>1: Reset is enabled |
| | WDTRSTIRQS | WDT Reset Interrupt Request Select<br><br>0: Non-maskable interrupt request is enabled<br><br>1: Reset is enabled | WDT Reset Interrupt Request Select<br><br>0: Non-maskable interrupt request or plain interrupt request is enabled<br><br>1: Reset is enabled |
| OFS1 | VDSEL[1:0] | Voltage Detection 0 Level Select<br><br>b1 b0<br>0 0: 3.80 V is selected<br>0 1: 2.80 V is selected<br>1 0: 1.90 V is selected<br>1 1: 1.72 V is selected | Voltage Detection 0 Level Select<br><br>b1 b0<br>0 0: Reserved<br>0 1: Selects 2.94V<br>1 0: Selects 2.87V<br>1 1: Selects 2.80V |
| MDEB | — | Endian Select Register B | — |
| MDES | — | Endian Select Register S | — |
| MDE | — | — | Endian Select Register |
| TMEF | — | — | TM Enable Flag Register |
| TMINF | — | — | TM Identification Data Register |
| FAW | — | — | Flash Access Window Setting Register |
| ROMCODE | — | — | ROM Code Protection Register |
| UB Code A | — | UB Code A | — |
| UB Code B | — | UB Code B | — |

## 2.4 Voltage Detection Circuit

Table 2.6 shows a Comparative Listing of Voltage Detection Circuit Specifications, and Table 2.7 shows a Comparative Listing of Voltage Detection Circuit Registers.

**Table 2.6 Comparative Listing of Voltage Detection Circuit Specifications**

| Item | | RX210 (LVDAa) | | | RX651 (LVDA) | | |
|---|---|---|---|---|---|---|---|
| | | **Voltage Monitoring 0** | **Voltage Monitoring 1** | **Voltage Monitoring 2** | **Voltage Monitoring 0** | **Voltage Monitoring 1** | **Voltage Monitoring 2** |
| VCC monitoring | Monitored voltage | Vdet0 | Vdet1 | Vdet2 | Vdet0 | Vdet1 | Vdet2 |
| | Detected event | Voltage drops past Vdet0 | Voltage rises or drops past Vdet1 | Voltage rises or drops past Vdet2<br>Input voltages to VCC and the CMPA2 pin can be switched using the LVCMPCR.EXVCCINP2 bit | Voltage drops past Vdet0 | Voltage rises or drops past Vdet1 | Voltage rises or drops past Vdet2 |
| | Detection voltage | Voltage selectable from four levels using OFS1 | Voltage selectable from 16 levels using LVDLVLR.LVD1LVL[3:0] bits | Varies according to whether VCC or the CMPA2 pin is selected.<br>Voltage selectable from 16 levels using LVDLVLR.LVD2LVL[3:0] bits | Selectable from among three different levels by using OFS1.VDSEL[1:0] bits | Selectable from among three different levels by using LVDLVLR.LVD1LVL[3:0] bits | Selectable from among three different levels by using LVDLVLR.LVD2LVL[3:0] bits |
| | Monitor flag | — | LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1 | LVD2SR.LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2 | — | LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1 | LVD2SR.LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2 |
| | | | LVD1SR.LVD1DET flag: Vdet1 passage detection | LVD2SR.LVD2DET flag: Vdet2 passage detection | | LVD1SR.LVD1DET flag: Vdet1 passage detection | LVD2SR.LVD2DET flag: Vdet2 passage detection |
| Process upon voltage detection | Reset | Voltage monitoring 0 reset | Voltage monitoring 1 reset | Voltage monitoring 2 reset | Voltage monitoring 0 reset | Voltage monitoring 1 reset | Voltage monitoring 2 reset |
| | | Reset when Vdet0 > VCC<br>CPU restart timing selectable:<br>after specified time with VCC > Vdet0 | Reset when Vdet1 > VCC<br>CPU restart timing selectable:<br>after specified time with VCC > Vdet1 or Vdet1 > VCC | Reset when Vdet2 > VCC<br>CPU restart timing selectable:<br>after specified time with VCC > Vdet2 or Vdet2 > VCC | Reset when Vdet0 > VCC<br>CPU restart timing selectable:<br>after specified time with VCC > Vdet0 | Reset when Vdet1 > VCC<br>CPU restart timing selectable:<br>after specified time with VCC > Vdet1 or Vdet1 > VCC | Reset when Vdet2 > VCC<br>CPU restart timing selectable:<br>after specified time with VCC > Vdet2 or Vdet2 > VCC |

| Item | | RX210 (LVDAa) Voltage Monitoring 0 | RX210 (LVDAa) Voltage Monitoring 1 | RX210 (LVDAa) Voltage Monitoring 2 | RX651 (LVDA) Voltage Monitoring 0 | RX651 (LVDA) Voltage Monitoring 1 | RX651 (LVDA) Voltage Monitoring 2 |
|---|---|---|---|---|---|---|---|
| Process upon voltage detection | Interrupt | — | Voltage monitoring 1 interrupt | Voltage monitoring 2 interrupt | — | Voltage monitoring 1 interrupt | Voltage monitoring 2 interrupt |
| | | | Non-maskable or maskable interrupt selectable | Non-maskable or maskable interrupt selectable | | Non-maskable interrupt or maskable interrupt selectable | Non-maskable interrupt or maskable interrupt selectable |
| | | | Interrupt request issued when Vdet1 > VCC and VCC > Vdet1 or either | Interrupt request issued when Vdet2 > VCC and VCC > Vdet2 or either | | Interrupt request issued when Vdet1 > VCC and VCC > Vdet1 or either | Interrupt request issued when Vdet2 > VCC and VCC > Vdet2 or either |
| Digital filter | Enable/ disable switching | Digital filter function not available | Available | Available | Digital filter function not available | Available | Available |
| | Sampling time | — | 1/n LOCO frequency x 2 (n: 1, 2, 4, 8) | 1/n LOCO frequency x 2 (n: 1, 2, 4, 8) | — | 1/n LOCO frequency x 2 (n: 2, 4, 8, 16) | 1/n LOCO frequency x 2 (n: 2, 4, 8, 16) |
| Event link function | | — | Available Vdet1 passage detection event output | Available Vdet2 passage detection event output | — | Available Output of event signals on detection of Vdet1 crossings | Available Output of event signals on detection of Vdet2 crossings |

**Table 2.7 Comparative Listing of Voltage Detection Circuit Registers**

| Register | Bit | RX210 (LVDA) | RX651 (LVDA) |
|---|---|---|---|
| LVD1CR1 | — | Voltage Monitoring 1 Circuit/Comparator A1 Control Register 1 | Voltage Monitoring 1 Circuit Control Register 1 |
| | LVD1IDTSEL[1:0] | Voltage Monitoring 1/Comparator A1 Interrupt/ELC Event Generation Condition Select | Voltage Monitoring 1 Interrupt Generation Condition Select |
| | LVD1IRQSEL | Voltage Monitoring 1/Comparator A1 Interrupt Type Select | Voltage Monitoring 1 Interrupt Type Select |
| LVD1SR | — | Voltage Monitoring 1 Circuit/Comparator A1 Status Register | Voltage Monitoring 1 Circuit Status Register |
| | LVD1DET | Voltage Monitoring 1/Comparator A1 Voltage Change Detection Flag | Voltage Monitoring 1 Voltage Change Detection Flag |
| | LVD1MON | Voltage Monitoring 1/Comparator A1 Signal Monitor Flag | Voltage Monitoring 1 Signal Monitor Flag |
| LVD2CR1 | — | Voltage Monitoring 2 Circuit/Comparator A2 Control Register 1 | Voltage Monitoring 2 Circuit Control Register 1 |
| | LVD2IDTSEL[1:0] | Voltage Monitoring 2/Comparator A2 Interrupt/ELC Event Generation Condition Select | Voltage Monitoring 2 Interrupt Generation Condition Select |
| | LVD2IRQSEL | Voltage Monitoring 2/Comparator A2 Interrupt Type Select | Voltage Monitoring 2 Interrupt Type Select |

| Register | Bit | RX210 (LVDA) | RX651 (LVDA) |
|---|---|---|---|
| LVD2SR | — | Voltage Monitoring 2 Circuit/Comparator A2 Status Register | Voltage Monitoring 2 Circuit Status Register |
| | LVD2DET | Voltage Monitoring 2/Comparator A2 Voltage Change Detection Flag | Voltage Monitoring 2 Voltage Change Detection Flag |
| | LVD2MON | Voltage Monitoring 2/Comparator A2 Signal Monitor Flag | Voltage Monitoring 2 Signal Monitor Flag |
| LVCMPCR | — | Voltage Monitoring Circuit/Comparator A Control Register | Voltage Monitoring Circuit Control Register |
| | EXVREFINP1 | Comparator A1 Reference Voltage External Input Select (b0) | — |
| | EXVCCINP1 | Comparator A1 Comparison Voltage External Input Select (b1) | — |
| | EXVREFINP2 | Comparator A2 Reference Voltage External Input Select (b2) | — |
| | EXVCCINP2 | Comparator A2 Comparison Voltage External Input Select (b3) | — |
| | LVD1E | Voltage Detection 1/Comparator A1 Enable<br>0: Voltage detection 1/comparator A1 circuit disabled<br>1: Voltage detection 1/comparator A1 circuit enabled | Voltage Detection 1 Enable*1<br>0: Voltage detection 1 circuit disabled<br>1: Voltage detection 1 circuit enabled |
| | LVD2E | Voltage Detection 2/Comparator A2 Enable<br>0: Voltage detection 2/comparator A2 circuit disabled<br>1: Voltage detection 2/comparator A2 circuit enabled | Voltage Detection 2 Enable*2<br>0: Voltage detection 2 circuit disabled<br>1: Voltage detection 2 circuit enabled |

| Register | Bit | RX210 (LVDA) | RX651 (LVDA) |
|---|---|---|---|
| LVDLVLR | LVD1LVL[3:0] | Voltage Detection 1 Level Select (Standard voltage during drop in voltage)<br>b3 b0<br>0 0 0 0: 4.15 V<br>0 0 0 1: 4.00 V<br>0 0 1 0: 3.85 V<br>0 0 1 1: 3.70 V<br>0 1 0 0: 3.55 V<br>0 1 0 1: 3.40 V<br>0 1 1 0: 3.25 V<br>0 1 1 1: 3.10 V<br>1 0 0 0: 2.95 V<br>1 0 0 1: 2.80 V<br>1 0 1 0: 2.65 V<br>1 0 1 1: 2.50 V<br>1 1 0 0: 2.35 V<br>1 1 0 1: 2.20 V<br>1 1 1 0: 2.05 V<br>1 1 1 1: 1.90 V | Voltage Detection 1 Level Select (Standard voltage during drop in voltage)<br>b3 b0<br>1 0 0 1: 2.99 V (Vdet1_1)<br>1 0 1 0: 2.92 V (Vdet1_2)<br>1 0 1 1: 2.85 V (Vdet1_3)<br>Settings other than above are prohibited. |
| | | The Value after reset is different. | |
| | LVD2LVL[3:0] | Voltage Detection 2 Level Select (Standard voltage during drop in voltage)<br>(When LVCMPCR.EXVCCINP2 = 0 (VCC select))<br>b7 b4<br>0 0 0 0: 4.15 V<br>0 0 0 1: 4.00 V<br>0 0 1 0: 3.85 V<br>0 0 1 1: 3.70 V<br>0 1 0 0: 3.55 V<br>0 1 0 1: 3.40 V<br>0 1 1 0: 3.25 V<br>0 1 1 1: 3.10 V<br>1 0 0 0: 2.95 V<br>1 0 0 1: 2.80 V<br>1 0 1 0: 2.65 V<br>1 0 1 1: 2.50 V<br>1 1 0 0: 2.35 V<br>1 1 0 1: 2.20 V<br>1 1 1 0: 2.05 V<br>1 1 1 1: 1.90 V<br>(When LVCMPCR.EXVCCINP2 = 1 (CMPA2 pin select))<br>b7 b4<br>0 0 0 1: 1.33 V<br>Settings other than above are prohibited. | Voltage Detection 2 Level Select (Standard voltage during drop in voltage)<br>b7 b4<br>1 0 0 1: 2.99 V (Vdet1_1)<br>1 0 1 0: 2.92 V (Vdet1_2)<br>1 0 1 1: 2.85 V (Vdet1_3)<br>Settings other than above are prohibited. |
| | | The Value after reset is different. | |

| Register | Bit | RX210 (LVDA) | RX651 (LVDA) |
|---|---|---|---|
| LVD1CR0 | — | Voltage Monitoring 1 Circuit/Comparator A1 Control Register 0 | Voltage Monitoring 1 Circuit Control Register 0 |
| | LVD1RIE | Voltage Monitoring 1/Comparator A1 Interrupt/Reset Enable | Voltage Monitoring 1 Interrupt/Reset Enable |
| | LVD1DFDIS | Voltage Monitoring 1/Comparator A1 Digital Filter Disable Mode Select | Voltage Monitoring 1 Digital Filter Disable Mode Select |
| | LVD1CMPE | Voltage Monitoring 1 Circuit/Comparator A1 Comparison Result Output Enable | Voltage Monitoring 1 Circuit Comparison Result Output Enable |
| | LVD1FSAMP [1:0] | Sampling Clock Select<br>b5 b4<br>0 0: LOCO divided by 1<br>0 1: LOCO divided by 2<br>1 0: LOCO divided by 4<br>1 1: LOCO divided by 8 | Sampling Clock Select<br>b5 b4<br>0 0: 1/2 LOCO frequency<br>0 1: 1/4 LOCO frequency<br>1 0: 1/8 LOCO frequency<br>1 1: 1/16 LOCO frequency |
| | LVD1RI | Voltage Monitoring 1 Circuit/Comparator A1 Mode Select | Voltage Monitoring 1 Circuit Mode Select |
| | LVD1RN | Voltage Monitoring 1/Comparator A1 Reset Negation Select | Voltage Monitoring 1 Reset Negate Select |
| LVD2CR0 | — | Voltage Monitoring 2 Circuit/Comparator A2 Control Register 0 | Voltage Monitoring 2 Circuit Control Register 0 |
| | LVD2RIE | Voltage Monitoring 2/Comparator A2 Interrupt/Reset Enable | Voltage Monitoring 2 Interrupt/Reset Enable |
| | LVD2DFDIS | Voltage Monitoring 2/Comparator A2 Digital Filter Disable Mode Select | Voltage Monitoring 2 Digital Filter Disable Mode Select |
| | LVD2CMPE | Voltage Monitoring 2 Circuit/Comparator A2 Comparison Result Output Enable | Voltage Monitoring 2 Circuit Comparison Result Output Enable |
| | LVD2FSAMP [1:0] | Sampling Clock Select<br>b5 b4<br>0 0: LOCO divided by 1<br>0 1: LOCO divided by 2<br>1 0: LOCO divided by 4<br>1 1: LOCO divided by 8 | Sampling Clock Select<br>b5 b4<br>0 0: 1/2 LOCO frequency<br>0 1: 1/4 LOCO frequency<br>1 0: 1/8 LOCO frequency<br>1 1: 1/16 LOCO frequency |
| | LVD2RI | Voltage Monitoring 2 Circuit/Comparator A2 Mode Select | Voltage Monitoring 2 Circuit Mode Select |
| | LVD2RN | Voltage Monitoring 2/Comparator A2 Reset Negation Select | Voltage Monitoring 2 Reset Negate Select |

Note 1. The voltage of VCC = AVCC0 = AVCC1 when LVD1 is enabled must be set to at least 80 mV above the maximum value of the voltage detection 1 level selected by the LVDLVLR.LVD1LVL[3:0] bits.

Note 2. The voltage of VCC = AVCC0 = AVCC1 when LVD2 is enabled must be set to at least 80 mV above the maximum value of the voltage detection 2 level selected by the LVDLVLR.LVD2LVL[3:0] bits.

## 2.5 Clock Generation Circuit

Table 2.8 shows a Comparative Listing of Clock Generation Circuit Specifications, and Table 2.9 shows a Comparative Listing of Clock Generation Circuit Registers.

**Table 2.8 Comparative Listing of Clock Generation Circuit Specifications**

| Item | RX210 | RX651 |
|---|---|---|
| Uses | • Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, ROM and RAM. | • Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, code flash memory and RAM.<br>• Generates the peripheral module clock (PCLKA) to be supplied to the ETHERC, EDMAC, RSPI, SCIi, MTU3, and AES. |
| | • Generates the peripheral module clocks (PCLKB and PCLKD) to be supplied to peripheral modules. | • Generates the peripheral module clock (PCLKB) to be supplied to peripheral modules. |
| | • The peripheral module clock used as the operating clock is PCLKD for S12AD and PCLKB for other modules. | • Generates the peripheral module clocks (for analog conversion) (PCLKC: unit 0; PCLKD: unit 1) to be supplied to S12AD. |
| | • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. | • Generates the flash-IF clock (FCLK) to be supplied to the flash interface. |
| | • Generates the external bus clock (BCLK) to be supplied to the external bus. | • Generates the external bus clock (BCLK) to be supplied to the external bus.<br>• Generates the SDRAM clock (SDCLK) to be supplied to the SDRAM.<br>• Generates the USB clock (UCLK) to be supplied to the USBb. |
| | • Generates the CAC clock (CACCLK) to be supplied to the CAC | • Generates the CAC clock (CACCLK) to be supplied to the CAC.<br>• Generates the CAN clock (CANMCLK) to be supplied to the CAN. |
| | • Generates the RTC-dedicated sub clock (RTCSCLK) to be supplied to the RTC. | • Generates the RTC sub-clock (RTCSCLK) to be supplied to the RTC.<br>• Generates the RTC main clock (RTCMCLK) to be supplied to the RTC. |
| | • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. | • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT.<br>• Generates the JTAG clock (JTAGTCK) to be supplied to the JTAG. |

| Item | RX210 | RX651 |
|---|---|---|
| Operating frequency | • ICLK: 50MHz (max)<br>• PCLKB: 32MHz (max)<br>• PCLKD: 50MHz (max)<br>• FCLK: 4 MHz to 32 MHz (for programming and erasing the ROM and E2 DataFlash)<br>32 MHz (max) (for reading from the E2 DataFlash)<br>• BCLK: 25MHz (max)<br>• BCLK pin output: 12.5 MHz (max)<br>• CACCLK: Same as frequency of each oscillator<br>• RTCSCLK: 32.768kHz<br>• WDTCLK: 125kHz | • ICLK: 120MHz (max)<br>• PCLKA: 120MHz (max)<br>• PCLKB: 60MHz (max)<br>• PCLKC: 60MHz (max)<br>• PCLKD: 60MHz (max)<br>• FCLK: 4 MHz to 60 MHz (for programming and erasing the code flash memory)<br>• BCLK: 120MHz (max)<br>• BCLK pin output: 60 MHz (max)<br>• SDCLK pin output: 60 MHz (max)<br>• UCLK: 48MHz (max)<br>• CACCLK: Same as the clock from respective oscillators<br>• CANMCLK: 24MHz (max)<br>• RTCSCLK: 32.768kHz<br>• RTCMCLK: 8MHz to 16MHz<br>• IWDTCLK: 120kHz<br>• JTAGTCK: 10MHz (max) |
| Main clock oscillator | • Resonator frequency: 1 MHz to 20 MHz<br>• External clock input frequency: 20 MHz (max)<br>• Connectable resonator or additional circuit: ceramic resonator, crystal resonator<br>• Connection pin: EXTAL, XTAL<br>• Oscillation stop detection function: When an oscillation stop is detected with the main clock, the system clock source is switched o LOCO and MTU output can be forcedly driven to the high-impedance | • Resonator frequency: 8 MHz to 24 MHz<br>• External clock input frequency: 24 MHz (max)<br>• Connectable resonator or additional circuit: ceramic resonator, crystal resonator<br>• Connection pin: EXTAL, XTAL<br>• Oscillation stop detection function: When an oscillation stop is detected with the main clock, the system clock source is switched to LOCO, and MTU3 output can be forcedly driven to the high-impedance. |
| Sub-clock oscillator | • Resonator frequency: 32.768 kHz<br>• Connectable resonator or additional circuit: crystal resonator<br>• Connection pin: XCIN, XCOUT | • Resonator frequency: 32.768 kHz<br>• Connectable resonator or additional circuit: crystal resonator<br>• Connection pin: XCIN, XCOUT |
| PLL circuit | • Input clock source: Main clock<br>• Input pulse frequency division ratio: Selectable from 1, 2, and 4<br>• Input frequency: 4 MHz to 12.5 MHz<br>• Frequency multiplication ratio: Selectable from 8, 10, 12, 16, 20, 24, and 25<br>• VCO oscillation frequency: 50 MHz to 100 MHz | • Input clock source: Main clock, HOCO<br>• Input pulse frequency division ratio: Selectable from 1, 2, and 3<br>• Input frequency: 8 MHz to 24 MHz<br>• Frequency multiplication ratio: Selectable from 10 to 30<br>• Output clock frequency of the PLL frequency synthesizer: 120 MHz to 240 MHz |
| High-speed on-chip oscillator (HOCO) | • Oscillation frequency: 32 MHz/36.864 MHz/40 MHz/50 MHz<br>• HOCO power supply control | • Selectable from 16 MHz, 18 MHz, and 20 MHz<br>• HOCO power supply control |

| Item | RX210 | RX651 |
|---|---|---|
| Low-speed on-chip oscillator (LOCO) | Oscillation frequency: 125 kHz | Oscillation frequency: 240 kHz |
| IWDT-dedicated on-chip oscillator | Oscillation frequency: 125 kHz | Oscillation frequency: 120 kHz |
| JTAG external clock input (TCK) | — | Input clock frequency: 10 MHz (max) |
| Control of output on the BCLK pin | • BCLK clock output or high-level output is selectable<br>• BCLK or BCLK/2 is selectable | • BCLK clock output or high output is selectable<br>• BCLK or BCLK/2 is selectable |
| Control of output on the SDCLK pin | — | SDCLK clock output or high output is selectable |
| Event linking (output) | — | Detection of stopping of the main clock oscillator |
| Event linking (input) | — | Switching of the clock source to the low-speed on-chip oscillator |

**Table 2.9 Comparative Listing of Clock Generation Circuit Registers**

| Register | Bit | RX210 | RX651 |
|---|---|---|---|
| SCKCR | PCKC[3:0] | — | Peripheral Module Clock C (PCLKC) Select (b7-b4) |
| | PCKA[3:0] | — | Peripheral Module Clock A (PCLKA) Select (b15-b12) |
| | PSTOP0 | — | SDCLK Pin Output Control |
| ROMWT | — | — | ROM Wait Cycle Setting Register |
| SCKCR2 | — | — | System Clock Control Register 2 |
| VRCR | — | Voltage Regulator Control Register | — |
| PLLCR | PLIDIV[1:0] | PLL Input Frequency Division Ratio Select<br>b1 b0<br>0 0: ×1<br>0 1: ×1/2<br>1 0: ×1/4<br>1 1: Setting prohibited | PLL Input Frequency Division Ratio Select<br>b1 b0<br>0 0: ×1<br>0 1: ×1/2<br>1 0: ×1/3<br>1 1: Setting prohibited |
| | PLLSRCSEL | — | PLL Clock Source Select (b4) |

| Register | Bit | RX210 | RX651 |
|---|---|---|---|
| PLLCR | STC[4:0]<br>STC[5:0] | Frequency Multiplication Factor Select (b12-b8)<br><br>b12 b8<br>0 0 1 1 1: ×8<br>0 1 0 0 1: ×10<br>0 1 0 1 1: ×12<br>0 1 1 1 1: ×16<br>1 0 0 1 1: ×20<br>1 0 1 1 1: ×24<br>1 1 0 0 0: ×25<br><br>Settings other than above are prohibited. | Frequency Multiplication Factor Select (b13-b8)<br><br>b13 b8<br>0 1 0 0 1 1: ×10.0<br>0 1 0 1 0 0: ×10.5<br>0 1 0 1 0 1: ×11.0<br>0 1 0 1 1 0: ×11.5<br>0 1 0 1 1 1: ×12.0<br>0 1 1 0 0 0: ×12.5<br>:<br>1 1 1 0 0 1: ×29.0<br>1 1 1 0 1 0: ×29.5<br>1 1 1 0 1 1: ×30.0<br>Settings other than above are prohibited |
| | | The Value after reset is different. | |
| HOCOCR2 | HCFRQ[1:0] | HOCO Frequency Setting<br>b1 b0<br>0 0: 32 MHz<br>0 1: 36.864 MHz<br>1 0: 40 MHz<br>1 1: 50 MHz | HOCO Frequency Setting<br>b1 b0<br>0 0: 16 MHz<br>0 1: 18 MHz<br>1 0: 20 MHz<br>Settings other than above are prohibited. |
| OSCOVFSR | — | — | Oscillation Stabilization Flag Register |
| MOSCWTCR*1 | MSTS[4:0] | Main Clock Oscillator Wait Time Select (b4-b0) | Main Clock Oscillator Wait Time Select (b7-b0) |
| | | The Value after reset is different. | |
| SOSCWTCR*1 | SSTS[4:0] | Sub-Clock Oscillator Wait Time Select (b4-b0) | Sub-Clock Oscillator Wait Time Select (b7-b0) |
| | | The Value after reset is different. | |
| MOFCR | MOFXIN | — | Main Clock Oscillator Forced Oscillation (b0) |
| | MODRV[2:0] | Main Clock Oscillator Drive Capability Switch (b3-b1) | — |
| | MODRV2[1:0] | Main Clock Oscillator Drive Capability Switch 2<br><br>b5 b4<br>0 1: 1 MHz to 8 MHz<br>1 0: 8.1 MHz to 15.9 MHz<br>1 1: 16 MHz to 20 MHz<br>Settings other than the above are prohibited. | Main Clock Oscillator Driving Ability 2 Switching<br><br>b5 b4<br>0 0: 20.1 to 24 MHz<br>0 1: 16.1 to 20 MHz<br>1 0: 8.1 to 16 MHz<br>1 1: 8 MHz |
| | | The Value after reset is different. | |
| PLLPCR | — | PLL Power Control Register | — |

Note 1. In the User's Manual: Hardware of the RX210 Group, MOSCWTCR and SOSCWTCR are described in section 11, Low Power Consumption.

## 2.6 Clock Frequency Accuracy Measurement Circuit

Table 2.10 shows a Comparative Listing of Clock Frequency Accuracy Measurement Circuit Specifications, and Table 2.11 shows a Comparative Listing of Clock Frequency Accuracy Measurement Circuit Registers.

**Table 2.10 Comparative Listing of Clock Frequency Accuracy Measurement Circuit Specifications**

| Item | RX210 (CAC) | RX651 (CAC) |
|---|---|---|
| Clock frequency measurement | The frequency of the following clocks can be measured.<br>• Clock output from main clock oscillator (main clock)<br>• Clock output from sub-clock oscillator (sub-clock)<br>• Clock output from high-speed on-chip oscillator (HOCO clock)<br>• Clock output from low-speed on-chip oscillator (LOCO clock)<br>• Clock output from IWDT-dedicated on-chip oscillator (IWDTCLK clock) | The frequency of the following clocks can be measured.<br>• Main clock<br>• Sub-clock<br>• HOCO clock<br>• LOCO clock<br>• IWDTCLK clock<br>• Peripheral module clock B (PCLKB) |
| Measurement reference clocks | • External clock input to the CACREF pin<br>• Main clock<br>• Sub-clock<br>• HOCO clock<br>• LOCO clock<br>• IWDTCLK clock | • External clock input to the CACREF pin<br>• Main clock<br>• Sub-clock<br>• HOCO clock<br>• LOCO clock<br>• IWDTCLK clock<br>• Peripheral module clock B (PCLKB) |
| Selectable function | Digital filter function | Digital filter function |
| Interrupt sources | • Measurement end interrupt<br>• Frequency error interrupt<br>• Overflow interrupt | • Measurement end interrupt<br>• Frequency error interrupt<br>• Overflow interrupt |
| Power consumption reduction function | Module stop state can be set. | Module stop state can be set |

**Table 2.11 Comparative Listing of Clock Frequency Accuracy Measurement Circuit Registers**

| Register | Bit | RX210 | RX651 |
|---|---|---|---|
| CACR1 | FMCS[2:0] | Frequency Measurement Clock Select<br>b3 b1<br>0 0 0: Output clock of main clock oscillator<br>0 0 1: Output clock of sub-clock oscillator<br>0 1 0: Output clock of high-speed on-chip oscillator<br>0 1 1: Output clock of low-speed on-chip oscillator<br>1 0 0: Output clock of IWDT-dedicated on-chip oscillator<br>Settings other than above are prohibited. | Measurement Target Clock Select<br>b3 b1<br>0 0 0: Main clock<br>0 0 1: Sub-clock<br>0 1 0: HOCO clock<br>0 1 1: LOCO clock<br>1 0 0: IWDTCLK clock<br>1 0 1: Peripheral module clock B (PCLKB)<br>Settings other than above are prohibited. |
| CACR2 | RSCS[2:0] | Reference Signal Generation Clock Select<br>b3 b1<br>0 0 0: Output clock of main clock oscillator<br>0 0 1: Output clock of sub-clock oscillator<br>0 1 0: Output clock of high-speed on-chip oscillator<br>0 1 1: Output clock of low-speed on-chip oscillator<br>1 0 0: Output clock of IWDT-dedicated on-chip oscillator | Measurement Reference Clock Select<br>b3 b1<br>0 0 0: Main clock<br>0 0 1: Sub-clock<br>0 1 0: HOCO clock<br>0 1 1: LOCO clock<br>1 0 0: IWDTCLK clock<br>1 0 1: Peripheral module clock B (PCLKB)<br>Settings other than above are prohibited. |
| | RCDS [1:0] | Reference Signal Generation Clock Frequency Division Ratio Select | Measurement Reference Clock Frequency Division Ration Select |

## 2.7 Low Power Consumption

Table 2.12 shows a Comparative Listing of Low Power Consumption Specifications, and Table 2.13 shows a Comparative Listing of Low Power Consumption Registers.

**Table 2.12 Comparative Listing of Low Power Consumption Specifications**

| Item | RX210 | RX651 |
|---|---|---|
| Reducing power consumption by switching clock signals | The frequency division ratio is settable independently for the system clock (ICLK), peripheral module clock (PCLKB), S12AD clock (PCLKD), external bus clock (BCLK), and Flash IF clock (FCLK). | The frequency division ratio is settable independently for the system clock (ICLK), peripheral module clock (PCLKA, PCLKB, PCLKC, PCLKD), external bus clock (BCLK), and flash interface clock (FCLK). |
| BCLK output control function | BCLK output or high-level output can be selected. | BCLK output or high-level output can be selected. |
| SDCLK output control function | — | SDCLK output or high-level output can be selected. |
| Module-stop function | Functions can be stopped independently for each peripheral module. | Functions can be stopped independently for each peripheral module. |
| Function for transition to low power consumption mode | Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled. | Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled. |
| Low power consumption modes | • Sleep mode<br>• All-module clock stop mode<br>• Software standby mode<br>• Deep software standby mode | • Sleep mode<br>• All-module clock stop mode<br>• Software standby mode<br>• Deep software standby mode |
| Function for lower operating power consumption | • Power consumption can be reduced in normal operation, sleep mode, and all-module clock stop mode by selecting an appropriate operating power consumption control mode according to the operating frequency and operating voltage.<br>• Seven operating power control modes<br>— High-speed operating mode<br>— Middle-speed operating mode 1A<br>— Middle-speed operating mode 1B<br>— Middle-speed operating mode 2A<br>— Middle-speed operating mode 2B<br>— Low-speed operating mode 1<br>— Low-speed operating mode 2 | • Power consumption can be reduced in normal operation, sleep mode, and all-module clock stop mode by selecting an appropriate operating power consumption control mode according to the operating frequency and operating voltage range.<br>• Three operating power control modes<br>— High-speed operating mode<br>— Low-speed operating mode 1<br>— Low-speed operating mode 2<br>There is no difference in power consumption when the same conditions (frequency and voltage) are set in low-speed operating modes 1 and 2. |

**Table 2.13 Comparative Listing of Low Power Consumption Registers**

| Register | Bit | RX210 | RX651 |
|---|---|---|---|
| MSTPCRA | MSTPA0 | — | Compare Match Timer W (Unit 1) Module Stop (b0) |
| | MSTPA1 | — | Compare Match Timer W (Unit 0) Module Stop (b1) |
| | MSTPA9 | Multifunction Timer Pulse Unit 3 Module Stop<br><br>Target module: MTU (MTU0 to MTU5) | Multifunction Timer Pulse Unit 3 Module Stop<br><br>Target module: MTU3 |
| | MSTPA10 | — | Programmable Pulse Generator (Unit 1) Module Stop (b10) |
| | MSTPA11 | — | Programmable Pulse Generator (Unit 0) Module Stop (b11) |
| | MSTPA13 | 16-Bit Timer Pulse Unit Module Stop | 16-Bit Timer Pulse Unit 0 (Unit 0) Module Stop |
| | MSTPA16 | — | 12-bit A/D Converter (Unit 1) Module Stop (b16) |
| | MSTPA17 | 12-Bit A/D Converter Module Stop<br>Target module: S12AD | 12-bit A/D Converter (Unit 0) Module Stop<br>Target module: S12AD unit 0 |
| | MSTPA19 | D/A Converter Module Stop<br><br>Target module: D/A | 12-bit D/A Converter Module Stop<br>Target module: 12-bit D/A |
| | MSTPA29 | Module Stop A29 | EXDMA Controller Module Stop<br>Target module: EXDMAC |
| MSTPCRB | MSTPB0 | — | CAN Module 0 Module Stop* (b0) |
| | MSTPB1 | — | CAN Module 1 Module Stop* (b1) |
| | MSTPB4 | Serial Communication Interface SCId Module Stop<br>Target module: SCId (SCI12) | Serial Communication Interface SCIh Module Stop<br>Target module: SCIh (SCI12) |
| | MSTPB6 | DOC Module Stop | Data Operation Circuit Module Stop |
| | MSTPB9 | ELC Module Stop | Event Link Controller Module Stop |
| | MSTPB10 | Comparator B Module Stop (b10) | — |
| | MSTPB15 | — | Ethernet Controller and Ethernet Controller DMA Controller (Channel 0) Modules Stop (b15) |
| | MSTPB16 | — | Serial Peripheral Interface 1 Module Stop b16) |
| | MSTPB19 | — | Universal Serial Bus 2.0 FS Interface Module Stop* (b19) |
| | MSTPB22 | — | Parallel Data Capture Unit Module Stop (b22) |

| Register | Bit | RX210 | RX651 |
|---|---|---|---|
| MSTPCRC | MSTPC1 | RAM1 Module Stop (b1) | — |
| | MSTPC7 | — | Standby RAM Module Stop (b7) |
| | MSTPC17 | — | I²C Bus Interface 2 Module Stop (b17) |
| | MSTPC22 | — | Serial Peripheral Interface 2 Module Stop (b22) |
| | MSTPC23 | — | Quad Serial Peripheral Interface Module Stop (b23) |
| MSTPCRD | — | — | Module Stop Control Register D |
| OPCCR | OPCM[2:0] | Operating Power Control Mode Select<br>b2 b0<br>0 0 0: High-speed operating mode<br>0 1 0: Middle-speed operating mode 1A<br>0 1 1: Middle-speed operating mode 1B<br>1 0 0: Middle-speed operating mode 2A<br>1 0 1: Middle-speed operating mode 2B<br>1 1 0: Low-speed operating mode 1<br>1 1 1: Low-speed operating mode 2<br>Settings other than above are prohibited. | Operating Power Control Mode Select<br>b2 b0<br>0 0 0: High-speed operating mode<br>1 1 0: Low-speed operating mode 1<br>1 1 1: Low-speed operating mode 2<br>Settings other than above are prohibited. |
| | | The Value after reset is different. | |
| MOSCWTCR*1 | MSTS[4:0]<br>MSTS[7:0] | Main Clock Oscillator Wait Time Select (b4-b0) | Main Clock Oscillator Wait Time Select (b7-b0) |
| | | The Value after reset is different. | |
| SOSCWTCR*1 | SSTS[4:0]<br>SSTS[7:0] | Sub-Clock Oscillator Wait Time Select (b4-b0) | Sub-Clock Oscillator Wait Time Select (b7-b0) |
| | | The Value after reset is different. | |
| PLLWTCR | — | PLL Wait Control Register | — |
| HOCOWTCR2 | — | HOCO Wait Control Register 2 | — |

| Register | Bit | RX210 | RX651 |
|---|---|---|---|
| DPSBYCR | DEEPCUT1<br>DEEPCUT [1:0] | Deep Cut (b1)<br><br>0: LVD and POR can be operated at deep software standby mode.<br><br>1: LVD does not operate at deep software standby mode and POR operates in the low power consumption operation mode at deep software standby mode. | Deep Cut (b1-b0)<br><br>b1 b0<br>0 0: Power is supplied to the standby RAM and USB resume detecting unit in deep software standby mode<br>0 1: Power is not supplied to the standby RAM and USB resume detecting unit in deep software standby mode<br>1 0: Setting prohibited<br>1 1: Power is not supplied to the standby RAM and USB resume detecting unit in deep software standby mode. In addition, LVD is stopped and the low power consumption function in a power-on reset circuit is enabled. |
| DPSIER1 | — | — | Deep Standby Interrupt Enable Register 1 |
| DPSIER2 | DRIICDIE | SDA-DS Deep Standby Cancel Signal Enable | SDA2-DS Deep Standby Release Signal Enable |
| | DRIICCIE | SCL-DS Deep Standby Cancel Signal Enable | SCL2-DS Deep Standby Release Signal Enable |
| | DUSBIE | — | USB Suspend/Resume Deep Standby Release Signal Enable |
| DPSIER3 | — | — | Deep Standby Interrupt Enable Register 3 |
| DPSIFR1 | — | — | Deep Standby Interrupt Flag Register 1 |
| DPSIFR2 | DRIICDIF | SDA-DS Deep Standby Cancel Flag | SDA2-DS Deep Standby Release Flag |
| | DRIICCIF | SCL-DS Deep Standby Cancel Flag | SCL2-DS Deep Standby Release Flag |
| | DUSBIF | — | USB Suspend/Resume Deep Standby Release Flag |
| DPSIFR3 | — | — | Deep Standby Interrupt Flag Register 3 |
| DPSIEGR1 | — | — | Deep Standby Interrupt Edge Register 1 |
| DPSIEGR2 | DRIICDEG | SDA-DS Edge Select | SDA2-DS Edge Select |
| | DRIICCEG | SCL-DS Edge Select | SCL2-DS Edge Select |
| DPSIEGR3 | — | — | Deep Standby Interrupt Edge Register 3 |
| FHSSBYCR | — | Flash HOCO Software Standby Control Register | — |

Note 1. In the User's Manual: Hardware of the RX651 Group, MOSCWTCR and SOSCWTCR are described in section 9, Clock Generation Circuit

## 2.8 Register Write Protection Function

Table 2.14 shows a Comparative Listing of Register Write Protection Function Specifications, and Table 2.15 shows a Comparative Listing of Register Write Protection Function Registers.

**Table 2.14 Comparative Listing of Register Write Protection Function Specifications**

| Item | RX210 | RX651 |
|---|---|---|
| PRC0 bit | • Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, HOCOCR2 | • Registers related to the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOCOCR2, OSTDCR, OSTDSR |
| PRC1 bit | • Registers related to the operating modes: SYSCR0, SYSCR1<br>• Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, OPCCR, RSTCKCR, MOSCWTCR*1, SOSCWTCR*1, PLLWTCR, DPSBYCR, DPSIER0, DPSIER2, DPSIFR0, DPSIFR2, DPSIEGR0, DPSIEGR2, FHSSBYCR, HOCOWTCR2<br>• Registers related to clock generation circuit: MOFCR, HOCOPCR, PLLPCR<br>• Software reset register: SWRR | • Registers related to the operating modes: SYSCR0, SYSCR1<br>• Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, DPSBYCR, DPSIER0, DPSIER1, DPSIER2, DPSIER3, DPSIFR0, DPSIFR1, DPSIFR2, DPSIFR3, DPSIEGR0, DPSIEGR1, DPSIEGR2. DPSIEGR3<br>• Registers related to clock generation circuit: MOSCWTCR*1, SOSCWTCR*1, MOFCR, HOCOPCR<br>• Software reset register: SWRR |
| PRC2 bit | Register related to the VRCR | |
| PRC3 bit | • Registers related to the LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR | • Registers related to the LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR |

Note 1. In the User's Manual: Hardware of RX651 Group, MOSCWTCR and SOSCWTCR are described in section 9.Clock Generation Circuit.

**Table 2.15 Comparative Listing of Register Write Protection Function Registers**

| Register | Bit | RX210 | RX651 |
|---|---|---|---|
| PRCR | PRC2 | Protect Bit 2 2 (b2) | — |

## 2.9 Exception Handling

Table 2.16 shows a Comparative Listing of Vector, and Table 2.17 shows a Comparative Listing of Return from Exception Handling Routine.

**Table 2.16 Comparative Listing of Vector**

| Exception (Event) | | RX210 | RX651 |
|---|---|---|---|
| Undefined instruction exception | | Fixed vector table | Exception vector table (EXTB) |
| Privileged instruction exception | | Fixed vector table | Exception vector table (EXTB) |
| Access exception | | — | Exception vector table (EXTB) |
| Floating-point exception | | — | Exception vector table (EXTB) |
| Reset | | Fixed vector table | Exception vector table (EXTB) |
| Non-maskable interrupt | | Fixed vector table | Exception vector table (EXTB) |
| Interrupt | Fast interrupt | FINTV | FINTV |
| | Other than above | Relocatable vector table (INTB) | Interrupt vector table (INTB) |
| Unconditional trap | | Relocatable vector table (INTB) | Interrupt vector table (INTB) |

**Table 2.17 Comparative Listing of Return from Exception Handling Routine**

| Exception | | RX210 | RX651 |
|---|---|---|---|
| Undefined instruction exception | | RTE | RTE |
| Privileged instruction exception | | RTE | RTE |
| Access exception | | — | RTE |
| Floating-point exception | | — | RTE |
| Reset | | Return is impossible | Return is impossible |
| Non-maskable interrupt | | Return is impossible | Prohibited |
| Interrupt | Fast interrupt | RTFI | RTFI |
| | Other than above | RTE | RTE |
| Unconditional trap | | RTE | RTE |

## 2.10 Interrupt Controller

Table 2.18 shows a Comparative Listing of Interrupt Controller Specifications, and Table 2.19 shows a Comparative Listing of Interrupt Controller Registers.

**Table 2.18 Comparative Listing of Interrupt Controller Specifications**

| Item | | RX210 (ICUb) | RX651 (ICUB) |
|---|---|---|---|
| Interrupt | Peripheral function interrupts | • Interrupts from peripheral modules<br>• Interrupt detection: Edge detection/level detection Edge detection or level detection is fixed for each source of connected peripheral modules. | • Interrupts from peripheral modules<br>• Interrupt detection: Edge detection/level detection (detection method is fixed for each interrupt source<br>• Group interrupt: Multiple interrupt sources are grouped together and treated as an interrupt source.<br>— Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection)<br>— Group BL0/BL1/BL2 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection)<br>— Group AL0/AL1 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection)<br>• Software configurable interrupt B: Any of the interrupt sources for peripheral modules that use PCLKB as the operating clock can be assigned to interrupt vector numbers 128 to 207.<br>• Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255. |

| Item | | RX210 (ICUb) | RX651 (ICUB) |
|---|---|---|---|
| Interrupt | External pin interrupts | • Interrupts from pins IRQ0 to IRQ7<br>• Number of sources: 8<br>• Interrupt detection: Low level/falling edge/rising edge/rising and falling edges<br>One of these detection methods can be set for each source.<br>• Digital filter function: Supported | • Interrupt by the input signal to the IRQi pin (i = 0 to 15)<br>• Number of sources: 16<br>• Interrupt detection method: Detection of low level, falling edge, rising edge, rising and falling edges<br>One of these detection methods can be set for each source.<br>• Digital filter can be used to remove noise. |
| | Software interrupt | • Interrupt generated by writing to a register<br>• One interrupt source | • Interrupt request can be generated by writing to a register.<br>• Two interrupt sources |
| | Event link Interrupt | The ELSR18I or ELSR19I interrupt is generated by an ELC event | — |
| | Interrupt priority level | Specified by registers. | Priority level can be set with interrupt source priority register r (IPRr) (r = 000 to 255). |
| | Fast interrupt function | Faster interrupt processing of the CPU can be set only for a single interrupt source. | CPU interrupt response time can be reduced. This function can be used for only one interrupt source. |
| | DTC and DMAC control | The DTC and DMAC can be activated by interrupt sources. | Interrupt sources can be used to start the DTC and DMAC. |
| | EXDMAC control | — | • Interrupt selected by software configurable interrupt B source select register 144 or software configurable interrupt A source select register 208 can be used to start EXDMAC0.<br>• Interrupt selected by software configurable interrupt B source select register 145 or software configurable interrupt A source select register 209 can be used to start EXDMAC1. |
| Non-maskable interrupts | NMI pin interrupt | • Interrupt from the NMI pin<br>• Interrupt detection: Falling edge/rising edge<br>• Digital filter function: Supported | • Interrupt by the input signal to the NMI pin<br>• Interrupt detection: Falling edge/rising edge<br>• Digital filter can be used to remove noise. |
| | Oscillation stop detection interrupt | Interrupt on detection of oscillation having stopped | This interrupt occurs when the main clock oscillator stop is detected. |
| | WDT underflow/ refresh error | Interrupt on an underflow of the down counter or occurrence of a refresh error | This interrupt occurs when the watchdog timer (WDT) underflows or a refresh error occurs. |
| | IWDT underflow/ refresh error | Interrupt on an underflow of the down counter or occurrence of a refresh error | This interrupt occurs when the independent watchdog timer (IWDT) underflows or a refresh error occurs. |

| Item | | RX210 (ICUb) | RX651 (ICUB) |
|---|---|---|---|
| Non-maskable interrupts | Voltage monitoring interrupt | • Voltage monitoring interrupt of voltage monitoring circuit 1 (LVD1)<br>• Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2) | • Interrupt from voltage detection circuit 1 (LVD1)<br>• Interrupt from voltage detection circuit 2 (LVD2) |
| | RAM error interrupt | — | This interrupt occurs when a parity check error is detected in the RAM. |
| Return from low power consumption state | Sleep mode | Return is initiated by non-maskable interrupts or any other interrupt source. | Exit sleep mode by any interrupt source. |
| | All-module clock stop mode | Return is initiated by non-maskable interrupts, IRQ0 to IRQ7 interrupts, WDT interrupts, TMR interrupts, or RTC alarm/periodic interrupts. | Exit all-module clock stop mode by the NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection interrupt, USB resume, RTC alarm, RTC period, IWDT, software configurable interrupt 146 to 157). |
| | Software standby mode | Return is initiated by non-maskable interrupts, IRQ0 to IRQ7 interrupts, or RTC alarm/periodic interrupts. | Exit all-module clock stop mode by the NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, RTC alarm, RTC period, IWDT). |
| | Deep software standby mode | — | Exit all-module clock stop mode by the NMI pin interrupt, specific external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, RTC alarm, RTC period). |

**Table 2.19 Comparative Listing of Interrupt Controller Registers**

| Register | Bit | RX210 (ICUb) | RX651 (ICUB) |
|---|---|---|---|
| IRn | — | Interrupt Request Register n<br>(n = interrupt vector number) | Interrupt Request Register n<br>(n = 016 to 255) |
| IPRn<br>IPRr | — | Interrupt Source Priority Register n<br>(n = 000 to 250) | Interrupt Source Priority Register r<br>(r = 000 to 255) |
| SWINT2R | — | — | Software Interrupt 2 Generation Register |
| DTCERn | — | DTC Activation Enable Register n<br>(n = interrupt vector number) | DTC Transfer Request Enable Register n (n = 026 to 255) |
| | DTCE | DTC Activation Enable<br><br>0: DTC Activation is disabled<br><br>1: DTC Activation is enabled | DTC Transfer Request Enable<br><br>0: The corresponding interrupt source is not selected as the DTC trigger.<br>1: The corresponding interrupt source is selected as the DTC trigger. |
| DMRSRm | — | DMAC Activation Request Select Register m<br>(m = DMAC channel number) | DMAC trigger Select Register m<br><br>(m = DMAC channel number) |
| | DMRS[7:0]<br>— | DMAC Activation Source Select<br>These bits specify the vector number for the DMAC activation request. | —<br>These bits set the interrupt vector number of the interrupt source as the DMAC trigger. |
| IRQCRi | | IRQ Control Register i (i = 0 to 7) | IRQ Control Register i (i = 0 to 15) |
| IRQFLTE1 | — | — | IRQ Pin Digital Filter Enable Register 1 |
| IRQFLTC1 | — | — | IRQ Pin Digital Filter Setting Register 1 |
| NMISR | RAMST | — | RAM Error Interrupt Status Flag (b6) |
| NMIER | RAMEN | — | RAM Error Interrupt Enable (b6) |
| GRPBE0 | — | — | Group BE0 Interrupt Request Register |
| GRPBL0/1/2 | — | — | Group BL0/BL1/BL2 Interrupt Request Register |
| GRPAL0/1 | — | — | Group AL0/AL1 Interrupt Request Register |
| GENBE0 | — | — | Group BE0 Interrupt Request Enable Register |
| GENBL0/1/2 | — | — | Group BL0/BL1/BL2 Interrupt Request Enable Register |
| GENAL0/1 | — | — | Group AL0/AL1 Interrupt Request Enable Register |
| GCRBE0 | — | — | Group BE0 Interrupt Clear Register |
| PIBRk | — | — | Software Configurable Interrupt B Request Register k<br>(k = 0h to Ah) |
| PIARk | — | — | Software Configurable Interrupt A Request Register k<br>(k = 0h to 5h, Bh) |
| SLIBXRn | — | — | Software Configurable Interrupt B Source Select Register Xn<br>(n = 128 to 143) |

| Register | Bit | RX210 (ICUb) | RX651 (ICUB) |
|---|---|---|---|
| SLIBRn | — | — | Software Configurable Interrupt B Source Select Register n (n = 144 to 207) |
| SLIARn | — | — | Software Configurable Interrupt A Source Select Register n (n = 208 to 255) |
| SELEXDR | — | — | EXDMAC Trigger Select Register |
| SLIPRCR | — | — | Software Configurable Interrupt Source Select Register Write Protect Register |

## 2.11 Buses

Table 2.20 shows a Comparative Listing of Bus Specifications, Table 2.21 shows a Comparative Listing of External Bus Specifications, and Table 2.22 shows a Comparative Listing of Bus Registers.

**Table 2.20 Comparative Listing of Bus Specifications**

| Bus Type | | RX210 | RX651 |
|---|---|---|---|
| CPU bus | Instruction bus | • Connected to the CPU (for instructions)<br>• Connected to on-chip memory (RAM, ROM)<br>• Operates in synchronization with the system clock (ICLK) | • Connected to the CPU (for instructions)<br>• Connected to on-chip memory (RAM, code flash memory)<br>• Operates in synchronization with the system clock (ICLK) |
| | Operand bus | • Connected to the CPU (for operands)<br>• Connected to on-chip memory (RAM, ROM)<br>• Operates in synchronization with the system clock (ICLK) | • Connected to the CPU (for operands)<br>• Connected to on-chip memory (RAM, code flash memory)<br>• Operates in synchronization with the system clock (ICLK) |
| Memory bus | Memory bus 1 | Connected to RAM | Connected to RAM |
| | Memory bus 2 | Connected to ROM | Connected to code flash memory |
| Internal main bus | Internal main bus 1 | • Connected to the CPU<br>• Operates in synchronization with the system clock (ICLK) | • Connected to the CPU<br>• Operates in synchronization with the system clock (ICLK) |
| | Internal main bus 2 | • Connected to the DMAC, DTC<br>• Connected to on-chip memory (RAM, ROM)<br>• Operates in synchronization with the system clock (ICLK) | • Connected to the DMAC, DTC, and SDSI<br>• Connected to on-chip memory (RAM, code flash memory)<br>• Operates in synchronization with the system clock (ICLK) |
| Internal peripheral bus | Internal peripheral bus 1 | • Connected to peripheral modules (DTC, DMAC, interrupt controller, and bus error monitoring section)<br>• Operates in synchronization with the system clock (ICLK) | • Connected to peripheral modules (DTC, DMAC, EXDMAC, interrupt controller, and bus error monitoring section)<br>• Operates in synchronization with the system clock (ICLK) (EXDMAC operates in synchronization with the BCLK) |
| | Internal peripheral bus 2 | • Connected to peripheral modules (modules other than those connected to internal peripheral bus 1)<br>• Operates in synchronization with the peripheral-module clock (PCLKB and PCLKD) | • Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, 4, and 5)<br>• Operates in synchronization with the peripheral-module clock (PCLKB) |
| | Internal peripheral bus 3 | — | • Connected to peripheral modules (USBb, PDC, and standby RAM)<br>• Operates in synchronization with the peripheral-module clock (PCLKB) |

| Bus Type | | RX210 | RX651 |
|---|---|---|---|
| Internal peripheral bus | Internal peripheral bus 4 | — | • Connected to peripheral modules (MTU3, SCIi, RSPI, and AES)<br>• Operates in synchronization with the peripheral-module clock (PCLKA) |
| | Internal peripheral bus 5 | — | Reserved area |
| | Internal peripheral bus 6 | • Connected to ROM (P/E) and E2 DataFlash memory<br>• Operates in synchronization with the Flash IF clock (FCLK) | • Connected to code flash (in P/E)<br>• Operates in synchronization with the FlashIF clock (FCLK) |
| External bus | CS area | • Connected to the external devices<br>• Operates in synchronization with the external-bus clock (BCLK) | • Connected to the external devices<br>• Operates in synchronization with the external-bus clock (BCLK) |
| | SDRAM area | — | • Connected to the SDRAM<br>• Operates in synchronization with the SDRAM clock (SDCLK) |

**Table 2.21 Comparative Listing of External Bus Specifications**

| Item | RX210 | RX651 |
|---|---|---|
| External address space | • An external address space is divided into four CS areas (CS0 to CS3) for management.<br>• Chip select signals can be output for each area.<br>• Bus width can be set for each area.<br>— Separate bus: An 8 or 16-bit bus space is selectable.<br>— Address/data multiplexed bus: An 8 or 16-bit bus space is selectable.<br>• An endian mode can be specified for each area. | • An external address space is divided into eight CS areas (CS0 to CS7) and the SDRAM area (SDCS) for management.<br>• Chip select signals can be output for each area.<br>• Bus width can be set for each area.<br>— Separate bus: An 8 or 16-bit bus space is selectable.<br>— Address/data multiplexed bus: An 8 or 16-bit bus space is selectable.<br>• An endian mode can be specified for each area. |
| CS area controller | • Recovery cycles can be inserted.<br>— Read recovery: Up to 15 cycles<br>— Write recovery: Up to 15 cycles<br>• Cycle wait function: Wait for up to 31 cycles (page access: up to 7 cycles)<br>• Wait control can be used to set up the following.<br>— Timing of assertion and negation for chip-select signals (CS0# to CS3#)<br>— The timing of assertion of the read signal (RD#) and write signals (WR#, WR0#, WR1#)<br>— The timing with which data output starts and ends<br>• Write access mode: Single write strobe mode/byte strobe mode<br>• Separate bus or address/data multiplexed bus can be set for each area. | • Recovery cycles can be inserted.<br>— Read recovery: Up to 15 cycles<br>— Write recovery: Up to 15 cycles<br>• Cycle wait function: Wait for up to 31 cycles (page access: up to 7 cycles)<br>• Wait control can be used to set up the following.<br>— Timing of assertion and negation for chip-select signals (CS0# to CS7#)<br>— The timing of assertion of the read signal (RD#) and write signals (WR0#/WR#, and WR1# to WR1#)<br>— The timing with which data output starts and ends<br>• Write access mode: Single write strobe mode/byte strobe mode<br>• Separate bus or address/data multiplexed bus can be set for each area. |
| SDRAM area controller | — | • Multiplexing output of row address/column address (8, 9, 10, or 11 bits)<br>• Self-refresh and auto-Refresh selectable<br>• CAS latency can be specified from one to three cycles |
| Write buffer function | When write data from the bus master has been written to the write buffer, write access by the bus master is completed. | When write data from the bus master has been written to the write buffer, write access by the bus master is completed. |
| Frequency | • The CS area controller (CSC) operates in synchronization with the external-bus clock (BCLK)*1. | • The CS area controller (CSC) operates in synchronization with the external-bus clock (BCLK)*1.<br>• The SDRAM area controller (SDRAMC) operates in synchronization with the SDRAM clock (SDCLK). |

Note 1. The BCLK and the SDCLK should be operated with the same frequency when the SDRAM is in use.

**Table 2.22 Comparative Listing of Bus Registers**

| Register | Bit | RX210 | RX651 |
|---|---|---|---|
| CSnCR | — | CSn Control Register<br>(n = 0 to 3) | CSn Control Register<br>(n = 0 to 7) |
| | EMODE | Endian Mode<br><br>0: Endian of area n is the same as the endian of operating mode.<br>1: Endian of area n is not the endian of operating mode.<br>(n = 0 to 3) | Endian Mode<br><br>0: Endian of area n is the same as the endian of operating mode.<br>1: Endian of area n is not the endian of operating mode.<br>(n = 0 to 7) |
| | MPXEN | Address/Data Multiplexed I/O Interface Select<br><br>0: Separate bus interface is selected for area n.<br>1: Address/data multiplexed I/O interface is selected for area n.<br>(n = 0 to 3) | Address/Data Multiplexed I/O Interface Select<br><br>0: Separate bus interface is selected for area n.<br>1: Address/data multiplexed I/O interface is selected for area n.<br>(n = 0 to 7) |
| CSnREC | — | CSn Recovery Cycle Register<br>(n = 0 to 3) | CSn Recovery Cycle Register<br>(n = 0 to 7) |
| CSnMOD | — | CSn Mode Register<br>(n = 0 to 3) | CSn Mode Register<br>(n = 0 to 7) |
| CSnWCR1 | — | CSn Wait Control Register 1<br>(n = 0 to 3) | CSn Wait Control Register 1<br>(n = 0 to 7) |
| CSnWCR2 | — | CSn Wait Control Register 2<br>(n = 0 to 3) | CSn Wait Control Register 2<br>(n = 0 to 7) |
| SDCCR | — | — | SDC Control Register |
| SDCMOD | — | — | SDC Mode Register |
| SDAMOD | — | — | SDRAM Access Mode Register |
| SDSELF | — | — | SDRAM Self-Refresh Control Register |
| SDRFCR | — | — | SDRAM Refresh Control Register |
| SDRFEN | — | — | SDRAM Auto-Refresh Control Register |
| SDICR | — | — | SDRAM Initialization Sequence Control Register |
| SDIR | — | — | SDRAM Initialization Register |
| SDADR | — | — | SDRAM Address Register |
| SDTR | — | — | SDRAM Timing Register |
| SDMOD | — | — | SDRAM Mode Register |
| SDSR | — | — | SDRAM Status Register |
| BERSR1 | MST[2:0] | Bus Master Code<br><br>b6 b4<br>0 0 0: CPU<br>0 0 1: Reserved<br>0 1 0: Reserved<br>0 1 1: DTC/DMAC<br>1 0 0: Reserved<br>1 0 1: Reserved<br>1 1 0: Reserved<br>1 1 1: Reserved | Bus Master Code<br><br>b6 b4<br>0 0 0: CPU<br>0 0 1: Reserved<br>0 1 0: Reserved<br>0 1 1: DTC/DMAC<br>1 0 0: Reserved<br>1 0 1: Reserved<br>1 1 0: SDSI<br>1 1 1: EXDMAC |

| Register | Bit | RX210 | RX651 |
|---|---|---|---|
| BUSPRI | BPGB[1:0] | Internal Peripheral Bus 2 Priority Control | Internal Peripheral Bus 2 and 3 Priority Control |
| | BPHB[1:0] | | Internal Peripheral Bus 4 Priority Control (b9-b8) |

## 2.12 DMA Controller

Table 2.23 shows a Comparative Listing of DMA Controller Specifications, and Table 2.24 shows a Comparative Listing of DMA Controller Registers.

**Table 2.23 Comparative Listing of DMA Controller Specifications**

| Item | | RX210 (DMACA) | RX651 (DMACAa) |
|---|---|---|---|
| Number of channels | | 4 (DMACm (m = 0 to 3)) | 8 (DMACm (m = 0 to 7)) |
| Transfer space | | 512 Mbytes<br>(0000 0000h to 0FFF FFFFh and F000 0000h to FFFF FFFFh excluding reserved areas) | 512 Mbytes<br>(0000 0000h to 0FFF FFFFh and F000 0000h to FFFF FFFFh excluding reserved areas) |
| Maximum transfer volume | | 1M data<br>(Maximum number of transfers in block transfer mode: 1,024 data × 1,024 blocks) | 64 Mbytes<br>(Maximum number of transfers in block transfer mode: 1,024 data × 65,536 blocks) |
| DMA request source | | Activation source selectable for each channel<br>• Software trigger<br>• Interrupt requests from peripheral modules or trigger input to external interrupt input pins | Request source selectable for each channel<br>• Software trigger<br>• Interrupt requests from peripheral modules or trigger input to external interrupt input pins |
| Channel priority | | Channel 0 > Channel 1 > Channel 2 > Channel 3 (Channel 0: Highest) | Channel 0 > Channel 1 > Channel 2 > Channel 3... > Channel 7<br>(Channel 0: Highest) |
| Transfer data | Single data | Bit length: 8, 16, 32 bits | Bit length: 8, 16, 32 bits |
| | Block size | Number of data: 1 to 1,024 | Number of data: 1 to 1,024 |
| Transfer mode | Normal transfer mode | • One data transfer by one DMA transfer request<br>• Free running mode (setting in which total number of data transfers is not specified) settable | • One data transfer by one DMA transfer request<br>• Free running mode (setting in which total number of data transfers is not specified) settable |
| | Repeat transfer mode | • One data transfer by one DMA transfer request<br>• Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination.<br>• Maximum settable repeat size: 1,024 | • One data transfer by one DMA transfer request<br>• Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination.<br>• Maximum settable repeat size: 1,024 |
| | Block transfer mode | • One block data transfer by one DMA transfer request<br>• Maximum settable block size: 1,024 data | • One block data transfer by one DMA transfer request<br>• Maximum settable block size: 1,024 data |

| Item | | RX210 (DMACA) | RX651 (DMACAa) |
|---|---|---|---|
| Selective functions | Extended repeat area function | • Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed<br>• Area of 2 bytes to 128 Mbytes separately settable as extended repeat area for transfer source and destination | • Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed<br>• Area of 2 bytes to 128 Mbytes separately settable as extended repeat area for transfer source and destination |
| Interrupt request | Transfer end interrupt | Generated on completion of transferring data volume specified by the transfer counter. | Generated on completion of transferring data volume specified by the transfer counter. |
| | Transfer escape end interrupt | Generated when the repeat size of data transfer is completed or the extended repeat area overflows. | Generated when the repeat size of data transfer is completed or the extended repeat area overflows. |
| Event link function | | Event link request is generated after one data transfer (for block, after one block transfer). | An event link request is generated after each data transfer (for block transfer, after each block is transferred). |
| Power consumption reduction function | | Module stop state can be set. | Module-stop state can be set. |

**Table 2.24 Comparative Listing of DMA Controller Registers**

| Register | Bit | RX210 (DMACA) | RX651 (DMACAa) |
|---|---|---|---|
| DMCRB | — | DMA Block Transfer Count Register (b9-b0)<br><br>001h to 3FFh (1 to 1023)<br>000h (1024) | DMA Block Transfer Count Register (b15-b0)<br><br>0001h to FFFFh (1 to 65535)<br>0000h (65536) |
| DMIST | — | — | DMAC74 Interrupt Status Monitor Register |

## 2.13 Data Transfer Controller

Table 2.25 shows a Comparative Listing of Data Transfer Controller Specifications, and Table 2.26 shows a Comparative Listing of Data Transfer Controller Registers.

**Table 2.25 Comparative Listing of Data Transfer Controller Specifications**

| Item | RX210 (DTCa) | RX651 (DTCb) |
|---|---|---|
| Number of channels | Channel transfer corresponding to the interrupt source is possible (transferred by DTC activation request from the ICU). | The same number as all interrupt sources that can start the DTC transfer |
| Transfer mode | • Normal transfer mode<br>— A single activation leads to a single data transfer.<br>• Repeat transfer mode<br>— A single activation leads to a single data transfer.<br>— The transfer address is returned to the transfer start address after the number of data transfers corresponding to “repeat size”.<br>— The maximum repeat size is 256.<br>• Block transfer mode<br>— A single activation leads to the transfer of a single block.<br>— The maximum block size is 256 data. | • Normal transfer mode<br>— A single transfer request leads to a single data transfer.<br>• Repeat transfer mode<br>— A single transfer request leads to a single data transfer.<br>— The transfer address is returned to the transfer start address after the number of data transfers corresponding to “repeat size”.<br>— The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, 1024 bytes.<br>• Block transfer mode<br>— A single transfer request leads to the transfer of a single block.<br>— The maximum block size is 256 × 32 bits = 1024 byte |
| Chain transfer | • Data of multiple channels can be transferred on a single activation source (chain transfer).<br>• Either “executed when the counter is 0” or “always executed” can be selected for chain transfer. | • Multiple types of data transfers can sequentially be executed in response to a single request.<br>• Either “performed only when the transfer counter becomes 0” or “every time” can be selected. |
| Sequence transfer | — | A series of complicated transfers can be registered as a sequence. Any sequence can be selected by the transfer data and executed.<br>• Only one trigger source can be set at a time.<br>• Up to 256 sequences for a single trigger source<br>• The data that is initially transferred in response to a transfer request determines a sequence<br>• The whole sequence can be executed on a single request, or be suspended in the middle of the sequence and resumed on the next transfer request (division of sequence). |

| Item | RX210 (DTCa) | RX651 (DTCb) |
|---|---|---|
| Transfer space | • In short-address mode: 16 Mbytes (Areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh excepting reserved areas)<br>• In full-address mode: 4 Gbytes (Area from 0000 0000h to FFFF FFFFh excepting reserved areas) | • In short-address mode: 16 Mbytes (Areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh except reserved areas)<br>• In full-address mode: 4 Gbytes (Area from 0000 0000h to FFFF FFFFh except reserved areas) |
| Data transfer units | • Length of a single data: 8, 16, or 32 bits<br>• Number of data for a single block: 1 to 256 data | • Single data: 1 byte (8 bits), 1 word (16 bits), 1 longword (32 bits)<br>• Single block size: 1 to 256 data |
| CPU interrupt source | • An interrupt request can be generated to the CPU on a DTC activation interrupt.<br>• An interrupt request can be generated to the CPU after a single data transfer.<br>• An interrupt request can be generated to the CPU after data transfer of specified volume. | • An interrupt request can be generated to the CPU on a request source for a data transfer.<br>• An interrupt request can be generated to the CPU after a single data transfer.<br>• An interrupt request can be generated to the CPU after data transfer of specified volume |
| Event link function | Event link request is generated after one data transfer (for block, after one block transfer). | An event link request is generated after one data transfer (for block, after one block transfer). |
| Read skip | Transfer data read skip can be specified. | Reading of the transfer information can be skipped when the same transfer is repeated. |
| Write-back skip | When “fixed” is selected for transfer source address and/or transfer destination address, writeback skip execution is provided. | Write-back of the transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed. |
| Write-back disable | — | Allows disabling the write-back of transfer information. |
| Displacement addition | — | The displacement value can be added to the transfer source address (for each transfer information) |
| Lower power consumption function | Module stop state can be specified | Module stop state can be specified |

**Table 2.26 Comparative Listing of Data Transfer Controller Registers**

| Register | Bit | RX210 (DTCa) | RX651 (DTCb) |
|---|---|---|---|
| MRA | WBDIS | — | Write-back Disable (b0) |
| MRB | SQEND | — | Sequence Transfer End (b0) |
| | INDX | — | Index Table Reference (b1) |
| MRC | — | — | DTC Mode Register C |
| DTCVBR | — | DTC Vector Base Address<br><br>Lower 12 bits:<br>These bits are read as 0. The write value should be 0.<br><br>Upper 4bits:<br>The upper 4 bits (b31 to b28) are ignored, and the address of this register is extended by the value specified by b27.<br><br>It can be set in the range of 0000 0000h to 07FF F000h and F800 0000h to FFFF F000h in 4-Kbyte units | DTC Vector Base Register<br><br>Lower 10 bits:<br>These bits are read as 0. The write value should be 0.<br><br>Upper 4bits:<br>The upper 4 bits (b31 to b28) are ignored, and the address of this register is extended by the value specified by b27<br><br>It can be set in the range of 0000 0000h to 07FF FC00h and F800 0000h to FFFF FC00h in 1-Kbyte units. |
| DTCIBR | — | — | DTC Index Table Base Register |
| DTCOR | — | — | DTC Operation Register |
| DTCSQE | — | — | DTC Sequence Transfer Enable Register |
| DTCDISP | — | — | DTC Address Displacement Register |

## 2.14 Event Link Controller

Table 2.27 shows a Comparative Listing of Event Link Controller Specifications, and Table 2.28 shows a Comparative Listing of Event Link Controller Registers.

**Table 2.27 Comparative Listing of Event Link Controller Specifications**

| Item | RX210 (ELC) | RX651 (ELC) |
|---|---|---|
| Event link | • 59 types of event signals can be directly connected to modules.<br>• The operation of timer modules can be selected when an event is input to the timer module.<br>• Event link operation is possible for ports B and E.<br>— Single-port*1: An event link can be set for a specified 1-bit in a port.<br>— Port group*1: An event link can be set for a group of specified bits within an 8-bit port. | • 82 types of event signals can be directly connected to modules.<br>• The operation of timer modules can be selected when an event is input to the timer module.<br>• Event link operation is possible for port B and port E.<br>— Single port*1: An event link can be set for a single bit specified in a port.<br>— Port group*1: An event link can be set for a group of single bits specified within eight I/O ports. |
| Low power consumption function | Module stop state can be specified | Module stop state can be specified |

**Table 2.28 Comparative Listing of Event Link Controller Registers**

| Register | Bit | RX210 (ELC) | RX651 (ELC) |
|---|---|---|---|
| ELSRn | — | Event Link Setting Register n<br>(n = 1 to 4, 7, 10, 12, 15, 16, 18 to 29) | Event Link Setting Register n<br>(n = 0, 3, 4, 7, 10 to 13, 15, 16, 18 to 28, 33, 35 to 38, 45) |
| | ELS[7:0] | Event Link Select b7 b0<br>00000000: Event link function is disabled.<br>00000001 to 01101001: Set the number for the event signal to be linked.<br>Settings other than above are prohibited. | Event Link Select 00h: Event output to the corresponding peripheral module is disabled.<br>01h to BDh: Set the number for the event signal to be linked.<br>Settings other than above are prohibited |
| ELOPA | MTU0MD[1:0] | — | MTU0 Operation Select (b1-b0) |
| | MTU1MD[1:0] | MTU1 Operation Select (b3-b2) | — |
| | MTU2MD[1:0] | MTU2 Operation Select (b5-b4) | — |
| ELOPD | TMR1MD[1:0] | — | TMR1 Operation Select (b3-b2) |
| | TMR3MD[1:0] | — | TMR3 Operation Select (b7-b6) |
| ELOPF | — | — | Event Link Option Setting Register F |
| ELOPH | — | — | Event Link Option Setting Register H |

## 2.15 I/O Ports

Table 2.29 shows a Comparative Listing of I/O Ports Specifications, and Table 2.30 shows a Comparative Listing of I/O Port Registers.

**Table 2.29 Comparative Listing of I/O Ports Specifications**

| | RX210 | | RX651 | |
|---|---|---|---|---|
| **Port** | **145 or 144Pins** | **100pins** | **145 or 144Pins** | **100pins** |
| PORT0 | P00 to P03, P05, P07 | P03, P05, P07 | P00 to P03, P05, P07 | P05, P07 |
| PORT1 | P12 to P17 | P12 to P17 | P12 to P17 | P12 to P17 |
| PORT2 | P20 to P27 | P20 to P27 | P20 to P27 | P20 to P27 |
| PORT3 | P30 to P37 | P30 to P37 | P30 to P37 | P30 to P37 |
| PORT4 | P40 to P47 | P40 to P47 | P40 to P47 | P40 to P47 |
| PORT5 | P50 to P56 | P50 to P55 | P50 to P56 | P50 to P55 |
| PORT6 | P60 to P67 | None | P60 to P67 | None |
| PORT7 | P70 to P77 | None | P70 to P77 | None |
| PORT8 | P80 to P83, P86, P87 | None | P80 to P83, P86, P87 | None |
| PORT9 | P90 to P93 | None | P90 to P93 | None |
| PORTA | PA0 to PA7 | PA0 to PA7 | PA0 to PA7 | PA0 to PA7 |
| PORTB | PB0 to PB7 | PB0 to PB7 | PB0 to PB7 | PB0 to PB7 |
| PORTC | PC0 to PC7 | PC0 to PC7 | PC0 to PC7 | PC0 to PC7 |
| PORTD | PD0 to PD7 | PD0 to PD7 | PD0 to PD7 | PD0 to PD7 |
| PORTE | PE0 to PE7 | PE0 to PE7 | PE0 to PE7 | PE0 to PE7 |
| PORTF | PF5 | None | PF5 | None |
| PORTH | PH0 to PH3 | PH0 to PH3 | None | None |
| PORTJ | PJ1, PJ3, PJ5 | PJ1, PJ3 | PJ3, PJ5 | PJ3 |
| PORTK | PK2 to PK5 | None | None | None |
| PORTL | PL0, PL1 | None | None | None |
| Total | 123 | 85 | 112 | 79 |

**Table 2.30 Comparative Listing of I/O Port Registers**

| Register | Bit | RX210 | RX651 |
|---|---|---|---|
| PDR | — | Port Direction Register<br>Pmn I/O Select<br>n = 0 to 7<br>m = 0 to 9, A to F, H, J, K, L | Port Direction Register<br>Pmn I/O Select<br>n = 0 to 7<br>m = 0 to 9, A to F, J |
| PODR | — | Port Output Data Register<br>Pmn Output Data Store<br>n = 0 to 7<br>m = 0 to 9, A to F, H, J, K, L | Port Output Data Register<br>Pmn Output Data Store<br>n = 0 to 7<br>m = 0 to 9, A to F, J |
| PIDR | — | Port Input Data Register<br>Pmn<br>n = 0 to 7<br>m = 0 to 9, A to F, H, J, K, L | Port Input Register<br>Pmn<br>n = 0 to 7<br>m = 0 to 9, A to F, J |
| PMR | — | Port Mode Register<br>Pmn Pin Mode Control<br>n = 0 to 7<br>m = 9 to 0, A to F, H, J, K, L | Port Mode Register<br>Pmn Pin Mode Control<br>n = 0 to 7<br>m = 9 to 0, A to F, J |
| ODR0 | — | Open Drain Control Register 0<br>m = 0 to 3, 5 to 9, A to C, E, K | Open Drain Control Register 0<br>m = 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, J |
| | Pm1 Output Type Select | Pm1 Output Type Select<br>• P01, P21, P31, P51, P61, P81, P91, PA1, PB1, PC1<br>b2 0: CMOS Output<br>1: N channel Open drain<br>b3: This bit is read as 0. The write value should be 0.<br>• PE1<br>b3 b2<br>0 0: CMOS Output<br>0 1: N channel Open drain<br>1 0: P channel Open drain<br>1 1: Hi-Z | • In case of except Port E1<br>Odd-bit Even-bit<br>x 0: CMOS Output<br>x 1: N channel Open drain<br>(b1, b3, b5, b7: Reserved)<br>• In case of Port PE1<br>b3 b2<br>0 0: CMOS Output<br>0 1: N channel Open drain<br>1 0: P channel Open drain<br>1 1: Setting prohibit |
| ODR1 | — | Open Drain Control Register 1<br>m = 1, 2, 3, 7, A to C, E, K | Open Drain Control Register 1<br>m = 0, 1, 2, 3, 4, 5, 6, 7, 8, A to F, J |
| PCR | — | Pull-Up Resistor Control Register<br>m = 0 to 9, A to F, H, J to L | Pull-Up Resistor Control Register<br>m = 0 to 9, A to F, J |
| DSCR | — | Drive Capacity Control Register<br>m = 0, 1, 2, 3, 5, 6, 7, 8, 9, A to E, H, J, K | Drive Capacity Control Register<br>m = 0, 2, 5, 9, A to E |
| DSCR2 | — | — | Drive Capacity Control Register 2 |

## 2.16 Multi-Function Pin Controller

Table 2.31 shows a Comparative Listing of Multi-Function Pin Controller Registers.

**Table 2.31 Comparative Listing of Multi-Function Pin Controller Registers**

| Register | Bit | RX210 (MPC) | RX651 (MPC) |
|---|---|---|---|
| PmnPFS | — | Refer to the user's manual for descriptions of the pin function control registers. | |
| PFCSE | CS0E | CS0 Enable of PC7 | CS0 Enable |
| | CS1E | CS1 Enable of PC6 | CS1 Enable |
| | CS2E | CS2 Enable of P26 | CS2 Enable |
| | CS3E | CS3 Enable of P27 | CS3 Enable |
| | CS4E | CS0 Enable of P24 | CS4 Enable |
| | CS5E | CS1 Enable of P25 | CS5 Enable |
| | CS6E | CS2 Enable of PC5 | CS6 Enable |
| | CS7E | CS3 Enable of PC4 | CS7 Enable |
| PFCSS0 | — | — | CS Output Pin Select Register 0 |
| PFCSS1 | — | — | CS Output Pin Select Register 1 |
| PFBCR0 | ADRHMS | — | A16 to A23 Output Enable (b1) |
| | ADRHMS2 | — | A16 to A23 Output Enable 2 (b2) |
| | BCLKO | — | BCLK Forced Output (b3) |
| PFBCR1 | MDSDE | — | SDRAM Pin Enable (b4) |
| | DQM1E | — | DQM1 Enable (b6) |
| | SDCLKE | — | SDCLK Enable (b7) |

## 2.17 16-Bit Timer Pulse Unit

Table 2.32 shows a Comparative Listing of 16-Bit Timer Pulse Unit Specifications, and Table 2.33 shows a Comparative Listing of Multi-Function Pin Controller Registers.

**Table 2.32 Comparative Listing of 16-Bit Timer Pulse Unit Specifications**

| Item | RX210 (TPUa) | RX651 (TPUa) |
|---|---|---|
| Pulse input/output | Maximum 16 | Maximum 16 |
| Count clock | Seven or eight types are provided for each channel | Seven or eight types are provided for each channel |
| Settable operations | • Waveform output at compare match<br>• Input capture function (noise filters can be set)<br>• Counter clear operation<br>• Simultaneous writing to multiple timer counters (TCNT)<br>• Simultaneous clearing by compare match and input capture<br>• Synchronous input/output for registers by counter synchronous operation<br>• Maximum of 15-phase PWM output by combination with synchronous operation<br>• Cascaded operation | • Waveform output at compare match<br>• Input capture function (noise filters can be set)<br>• Counter clear operation<br>• Simultaneous writing to multiple timer counters (TCNT)<br>• Simultaneous clearing by compare match and input capture<br>• Synchronous input/output for registers by counter synchronous operation<br>• Maximum of 15-phase PWM output by combination with synchronous operation<br>• Cascaded operation |
| TPU0, TPU3 | Buffer operation can be set | Buffer operation can be set |
| TPU1, TPU2, TPU4, TPU5 | Phase counting mode can be set | Phase counting mode can be set |
| Interrupt source | 26 sources | 26 sources |
| Buffer operation | Automatic transfer of register data | Automatic transfer of register data |
| Generation of trigger | — | Programmable pulse generator (PPG) output trigger can be generated |
| | Conversion start trigger for the A/D converter can be generated. | Conversion start trigger for the A/D converter can be generated. |
| Event linking (output) | — | Six types of event signal can be output to the ELC.<br>• Compare match A (TPU0 to TPU3)<br>• Compare match B (TPU0 to TPU3)<br>• Compare match C (TPU0, TPU3)<br>• Compare match D (TPU0, TPU3)<br>• Overflow (TPU0 to TPU3)<br>Underflow (TPU1, TPU2) |
| Event linking (input) | — | Any of the three operations in response to event input is possible.<br>• Starting counts (TPU0 to TPU3)<br>• Restarting counts (TPU0 to TPU3)<br>• Input capture operation (TPU0 to TPU3) |
| Low power consumption function | Module stop state can be set for each unit. | Module stop state can be set |

**Table 2.33 Comparative Listing of Multi-Function Pin Controller Registers**

| Register | Bit | RX210 | RX651 |
|---|---|---|---|
| TIER | TTGE | A/D Conversion Start Request Enable | A/D Conversion Start Request Enable*1 |

Note 1. Bit 7 in TIER of TPU5 is reserved. This bit is read as 0. The write value should be 0.

## 2.18 8-Bit Timer

Table 2.34 shows a Comparative Listing of 8-Bit Timer Specifications, and Table 2.35 shows a Comparative Listing of 8-Bit Timer Registers.

**Table 2.34 Comparative Listing of 8-Bit Timer Specifications**

| Item | RX210 (TMR) | RX651 (TMR) |
|---|---|---|
| Count clocks | • Frequency divided clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192<br>• External clock | • Frequency divided clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192<br>• External clock |
| Number of channels | (8 bits x 2 channels) x 2 units | (8 bits x 2 channels) x 2 units |
| Compare match | • 8-bit mode (compare match A, compare match B)<br>• 16-bit mode (compare match A, compare match B) | • 8-bit mode (compare match A, compare match B)<br>• 16-bit mode (compare match A, compare match B) |
| Counter clear | Selected by compare match A or B, or an external reset signal. | Selected by compare match A or B, or an external reset signal. |
| Timer output | Output pulses with a desired duty cycle or PWM output | Output pulses with a desired duty cycle or PWM output |
| Cascading of two channels | • 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits)<br>• Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches). | • 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits)<br>• Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches). |
| Interrupt sources | Compare match A, compare match B, and overflow | Compare match A, compare match B, and overflow |
| Event link function (output) | Compare match A, compare match B, and overflow (TMR0, TMR2) | Compare match A, compare match B, and overflow (TMR0 to TMR3) |
| Event link function (input) | (1) Count start operation (TMR0, TMR2)<br>(2) Event counter operation (TMR0, TMR2)<br>(3) Count restart operation (TMR0, TMR2) | One of the following three operations proceeds in response to an event reception:<br>(1) Counting start operation (TMR0 to TMR3)<br>(2) Event counting operation (TMR0 to TMR3)<br>(3) Counting restart operation (TMR0 to TMR3) |
| DTC activation | DTC can be activated by compare match A interrupts or compare match B interrupts. | DTC can be activated by compare match A interrupts or compare match B interrupts. |
| A/D conversion start trigger of the A/D converter | — | Compare match A of TMR0 or TMR2 |
| Capable of generating baud rate clock for SCI | Generates baud rate clock for SCI. | Generation of baud rate clock for SCI |

| Item | RX210 (TMR) | RX651 (TMR) |
|---|---|---|
| Low power consumption function | Each unit can be placed in a module stop state | Each unit can be placed in a module stop state |

**Table 2.35 Comparative Listing of 8-Bit Timer Registers**

| Register | Bit | RX210 (TMR) | RX651 (TMR) |
|---|---|---|---|
| TCSR | ADTE | — | A/D Trigger Enable (b4) |

## 2.19 Realtime Clock

Table 2.36 shows a Comparative Listing of Realtime Clock Specifications, and Table 2.37 shows a Comparative Listing of Realtime Clock Registers.

**Table 2.36 Comparative Listing of Realtime Clock Specifications**

| Item | RX210 (RTCb) | RX651 (RTCd) |
|---|---|---|
| Count modes | Calendar count mode | Calendar count mode/binary count mode |
| Count source | Sub-clock (XCIN) | Sub-clock (XCIN) or main clock (EXTAL) |
| Clock and calendar functions | • Calendar count mode<br>— Year, month, date, day of the week, hours, minutes, and seconds are counted and represented in BCD<br>— Selection of 12- or 24-hour mode<br>— 30-second adjustment (30 seconds or less are rounded down to 00 second, and 30 seconds or more are rounded up to one minute)<br>— Automatic leap year adjustment<br>— Start/stop function<br>— Indicates the state of 1, 2, 4, 8, 16, 32, or 64-Hz in binary<br>— Time error adjustment function<br>— Output a 1-Hz clock | • Calendar count mode<br>— Year, month, date, day-of-week, hour, minute, second are counted, BCD display<br>— 12 hours/24 hours mode switching function<br>— 30 seconds adjustment function (a number less than 30 is rounded down to 00 seconds, and 30 seconds or more are rounded up to one minute)<br>— Automatic adjustment function for leap years<br>• Binary count mode<br>— Count seconds in 32 bits, binary display<br>• Common to both modes<br>— Start/stop function<br>— The sub-second digit is displayed in binary units (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, or 64 Hz).<br>— Clock error correction function<br>— Clock (1 Hz/64 Hz) output |

| Item | RX210 (RTCb) | RX651 (RTCd) |
|---|---|---|
| Interrupt | • Alarm interrupt (ALM)<br>Year, month, date, day of the week, hours, minutes, and seconds can be selected as conditions for the alarm interrupt | • Alarm interrupt (ALM)<br>As an alarm interrupt condition, selectable which of the below is compared with:<br>— Calendar count mode: Year, month, date, day-of-week, hour, minute, or second can be selected<br>— Binary count mode: Each bit of the 32-bit binary counter |
| | • Periodic interrupt (PRD)<br>2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, or 1/256 second can be selected as an interrupt period. | • Periodic interrupt (PRD)<br>2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second can be selected as an interrupt period. |
| | • Carry interrupt (CUP)<br>Indicates occurrence of a carry to the seconds counter or a carry to the 64-Hz counter during reading of the 64-Hz counter | • Carry interrupt (CUP)<br>An interrupt is generated at either of the following timings:<br>— When a carry from the 64-Hz counter to the second counter is generated.<br>— When the 64-Hz counter is changed and the R64CNT register is read at the same time. |
| | • Recovery from software standby mode or deep software standby mode can be performed by an alarm interrupt or periodic interrupt | • Recovery from software standby mode or deep software standby mode can be performed by an alarm interrupt or periodic interrupt |
| Time-capture function | • Times when any of three event signals are input can be captured | • Times can be captured when the edge of the time capture event input pin is detected. |
| | • The month, date, hour, minute, and second are captured for each event | • For every event input, month, date, hour, minute, and second are captured or 32-bit binary counter value is captured. |
| Event link function | Periodic event output | Periodic event output |

**Table 2.37 Comparative Listing of Realtime Clock Registers**

| Register | Bit | RX210 (RTCb) | RX651 (RTCd) |
|---|---|---|---|
| BCNT0*1 | — | — | Binary Counter 0 |
| BCNT1*1 | — | — | Binary Counter 1 |
| BCNT2*1 | — | — | Binary Counter 2 |
| BCNT3*1 | — | — | Binary Counter 3 |
| RSECCNT | SEC1[3:0] | Ones Place of Seconds | 1-Second Count |
| | SEC10[2:0] | Tens Place of Seconds | 10-Second Count |
| RMINCNT | MIN1[3:0] | Ones Place of Minutes | 1-Minute Count |
| | MIN10[2:0] | Tens Place of Minutes | 10-Minute Count |
| RHRCNT | HR1[3:0] | Ones Place of Hours | 1-Hour Count |
| | HR10[1:0] | Tens Place of Hours | 10-Hour Count |
| RDAYCNT | DATE1[3:0] | Ones Place of Days | 1-Day Count |
| | DATE10[1:0] | Tens Place of Days | 10-Day Count |
| RMONCNT | MON1[3:0] | Ones Place of Months | 1-Month Count |
| | MON10 | Tens Place of Months | 10-Month Count |

| Register | Bit | RX210 (RTCb) | RX651 (RTCd) |
|---|---|---|---|
| RYRCNT | YR1[3:0] | Ones Place of Years | 1-Year Count |
| | YR10[3:0] | Tens Place of Years | 10-Year Count |
| BCNT0AR*1 | — | — | Binary Counter 0 Alarm Register |
| BCNT1AR*1 | — | — | Binary Counter 1 Alarm Register |
| BCNT2AR*1 | — | — | Binary Counter 2 Alarm Register |
| BCNT3AR*1 | — | — | Binary Counter 3 Alarm Register |
| BCNT0AER*1 | — | — | Binary Counter 0 Alarm Enable Register |
| BCNT1AER*1 | — | — | Binary Counter 1 Alarm Enable Register |
| BCNT2AER*1 | — | — | Binary Counter 2 Alarm Enable Register |
| BCNT3AER*1 | — | — | Binary Counter 3 Alarm Enable Register |
| RCR1 | RTCOS | — | RTCOUT Output Select (b3) |
| RCR2 | CNTMD | — | Count Mode Select (b7) |
| RCR4 | — | — | RTC Control Register 4 |
| RFRH/L | — | — | Frequency Register H/L |
| RSECCPy | SEC1[3:0] | Ones Place of Seconds Captured | 1-Second Capture |
| | SEC10[2:0] | Tens Place of Seconds Captured | 10-Second Capture |
| RMINCPy | MIN1[3:0] | Ones Place of Minutes Captured | 1-Minute Capture |
| | MIN10[2:0] | Tens Place of Minutes Captured | 10-Minute Capture |
| RHRCPy | HR1[3:0] | Ones Place of Hours Captured | 1-Hour Capture |
| | HR10[1:0] | Tens Place of Hours Captured | 10-Hour Capture |
| RDAYCPy | DATE1[3:0] | Ones Place of Days Captured | 1-Day Capture |
| | DATE10[1:0] | Tens Place of Days Captured | 10-Day Capture |
| RMONCPy | MON1[3:0] | Ones Place of Months Captured | 1-Month Capture |
| | MON10 | Tens Place of Months Captured | 10-Month Capture |
| BCNT0CPy*1 | — | — | BCNT0 Capture Register y (y = 0 to 2) |
| BCNT1CPy*1 | — | — | BCNT1 Capture Register y (y = 0 to 2) |
| BCNT2CPy*1 | — | — | BCNT2 Capture Register y (y = 0 to 2) |
| BCNT3CPy*1 | — | — | BCNT3 Capture Register y (y = 0 to 2) |

Note 1. In binary count mode

## 2.20 Watchdog Timer

Table 2.38 shows a Comparative Listing of Watchdog Timer Specifications, and Table 2.39 shows a Comparative Listing of Watchdog Timer Registers.

**Table 2.38 Comparative Listing of Watchdog Timer Specifications**

| Item | RX210 (WDTA) | RX651 (WDTA) |
|---|---|---|
| Count source | Peripheral clock (PCLK) | Peripheral module clock (PCLK) |
| Clock division ratio | Divide by 4, 64, 128, 512, 2,048, or 8,192 | Divide by 4, 64, 128, 512, 2,048, or 8,192 |
| Counter operation | Counting down using a 14-bit down-counter | Counting down using a 14-bit down-counter |
| Conditions for starting the counter | • Counting automatically starts after a reset (auto-start mode)<br>• Counting is started by refreshing the WDTRR register (writing 00h and then FFh) (register start mode) | • Auto-start mode: Counting automatically starts after a reset or after an underflow or refresh error occurs<br>• Register start mode: Counting is started by refresh operation (writing to the WDTRR register) |
| Conditions for stopping the counter | • Reset generated by the RES# pin (the down-counter and registers return to their initial values)<br>• A counter underflows or a refresh error is generated Count restarts (Auto-start mode: Count restarts automatically after a reset or non-maskable interrupt request is issued. Register start mode: Count restarts after refreshing the counter) | • Reset (the down-counter and other registers return to their initial values)<br>• A counter underflows or a refresh error is generated |
| Window function | Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods) | Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods) |
| Watchdog timer Reset sources | • Down-counter underflows<br>• Refreshing outside the refresh-permitted period (refresh error) | • Down-counter underflows<br>• Refreshing outside the refresh-permitted period (refresh error) |
| Interrupt sources | • A non-maskable interrupt (WUNI) is generated by an underflow of the down-counter<br>• Refreshing outside the refresh-permitted period (refresh error) | Non-maskable interrupt/interrupt sources<br>• Down-counter underflows<br>• Refreshing outside the refresh-permitted period (refresh error) |
| Reading the counter value | The down-counter value can be read by the WDTSR register. | The down-counter value can be read by the WDTSR register. |

**Table 2.39 Comparative Listing of Watchdog Timer Registers**

| Register | Bit | RX210 (WDTA) | RX651 (WDTA) |
|---|---|---|---|
| WDTRCR | RSTIRQS | Reset Interrupt Request Selection<br><br>0: Non-maskable interrupt request output is enabled<br>1: Reset output is enabled | Reset Interrupt Request Selection<br><br>0: Non-maskable interrupt request or interrupt request output is enabled<br>1: Reset output is enabled |

## 2.21 Independent Watchdog Timer

Table 2.40 shows a Comparative Listing of Independent Watchdog Timer Specifications, and Table 2.41 shows a Comparative Listing of Independent Watchdog Timer Registers.

**Table 2.40 Comparative Listing of Independent Watchdog Timer Specifications**

| Item | RX210 (IWDTA) | RX651 (IWDTa) |
|---|---|---|
| Count source | IWDT-dedicated clock (IWDTCLK) | IWDT-dedicated clock (IWDTCLK) |
| Clock divide ratio | Division by 1, 16, 32, 64, 128, or 256 | Division by 1, 16, 32, 64, 128, or 256 |
| Counter operation | Counting down using a 14-bit down-counter | Counting down using a 14-bit down-counter |
| Conditions for starting the counter | • Counting automatically starts after a reset (auto-start mode)<br>• Counting is started by refreshing the IWDTRR register (writing 00h and then FFh) (register start mode) | • Counting automatically starts after a reset (auto-start mode)<br>• Counting is started by refreshing the IWDTRR register (writing 00h and then FFh) (register start mode) |
| Conditions for stopping the counter | • Reset (the down-counter and other registers return to their initial values)<br>• A counter underflows or a refresh error is generated<br>Count restarts automatically in auto-start mode after a reset or output for non-maskable interrupt request/ interrupt request, or by refreshing the counter in register start Mode | • Reset (the down-counter and other registers return to their initial values)<br>• A counter underflows or a refresh error is generated<br>Counting restarts (In auto-start mode, counting automatically restarts after a reset or after a nonmaskable interrupt request/ interrupt request is output. In register start mode, counting restarts after refreshing.) |
| Window function | Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods) | Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods) |
| Reset output sources | • Down-counter underflows<br>• Refreshing outside the refresh-permitted period (refresh error) | • Down-counter underflows<br>• Refreshing outside the refresh-permitted period (refresh error) |
| interrupt sources | Non-maskable interrupt<br>• A non-maskable interrupt (WUNI) is generated by an underflow of the down-counter<br>• When refreshing is done outside the refresh-permitted period (refresh error) | Non-maskable interrupt/ interrupt sources<br>• Down-counter underflows<br>• Refreshing outside the refresh-permitted period (refresh error) |
| Reading the counter value | The down-counter value can be read by the IWDTSR register. | The down-counter value can be read by the IWDTSR register. |
| Event link function (output) | • Down-counter underflows<br>• Refreshing outside the refresh-permitted period (refresh error) | • Down-counter underflow event output<br>• Refresh error event output |
| Output signal (internal signal) | • Reset output<br>• Interrupt request output<br>• Sleep mode count stop control output | • Reset output<br>• Interrupt request output<br>• Sleep mode count stop control output |

| Item | RX210 (IWDTA) | RX651 (IWDTa) |
|---|---|---|
| Auto-start mode (controlled by option function select register 0 (OFS0)) | • Selecting the clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits)<br>• Selecting the time-out period of the watchdog timer (OFS0.IWDTTOPS[1:0] bits)<br>• Selecting the window start position in the watchdog timer (OFS0.IWDTRPSS[1:0] bits)<br>• Selecting the window end position in the watchdog timer (OFS0.IWDTRPES[1:0] bits)<br>• Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit)<br>• Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (OFS0.IWDTSLCSTP bit) | • Selecting the clock frequency divide ratio after a reset (OFS0.IWDTCKS[3:0] bits)<br>• Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits)<br>• Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits)<br>• Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits)<br>• Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit)<br>• Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (OFS0.IWDTSLCSTP bit) |
| Register start mode (controlled by the IWDT registers) | • Selecting the clock frequency division ratio after refreshing (IWDTCR.CKS[3:0] bits)<br>• Selecting the time-out period of the watchdog timer (IWDTCR.TOPS[1:0] bits)<br>• Selecting the window start position in the watchdog timer (IWDTCR.RPSS[1:0] bits)<br>• Selecting the window end position in the watchdog timer (IWDTCR.RPES[1:0] bits)<br>• Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit)<br>• Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (IWDTCSTPR.SLCSTP bit) | • Selecting the clock frequency divide ratio after refreshing (IWDTCR.CKS[3:0] bits)<br>• Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits)<br>• Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits)<br>• Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits)<br>• Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit)<br>• Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (IWDTCSTPR.SLCSTP bit) |

**Table 2.41 Comparative Listing of Independent Watchdog Timer Registers**

| Register | Bit | RX210 (IWDT) | RX651 (IWDTa) |
|---|---|---|---|
| IWDTRCR | RSTIRQS | Reset Interrupt Request Selection<br><br>0: Non-maskable interrupt request output is enabled.<br>1: Reset output is enabled. | Reset Interrupt Request Select<br><br>0: Non-maskable interrupt request or interrupt request output is enabled.<br>1: Reset output is enabled. |

## 2.22 Serial Communications Interface

The RX210 Group has 13 independent serial communications interface channels (SCIc: 12 channels, SCId: 1 channel).

The RX651 Group has 13 independent serial communications interface channels (SCIg: 10 channels, SCIi: 2 channels, SCIh: 1 channel).

Table 2.42 shows a Comparative Listing of SCIc and SCIg Specifications, Table 2.43 shows a Comparative Listing of SCIc and **SCIi Specifications**, Table 2.44 shows a Comparative Listing of SCId and SCIh Specifications, Table 2.45 shows a Comparative Listing of Serial Communications Interface Channels Specifications, and Table 2.46 shows a Comparative Listing of Serial Communications Interface Registers.

**Table 2.42 Comparative Listing of SCIc and SCIg Specifications**

| Item | | RX210 (SCIc) | RX651 (SCIg) |
|---|---|---|---|
| Number of channels | | 12 channels | 10 channels |
| Serial communications modes | | • Asynchronous operation<br>• Clock synchronous operation<br>• Smart card interface<br>• Simple I²C bus<br>• Simple SPI bus | • Asynchronous operation<br>• Clock synchronous operation<br>• Smart card interface<br>• Simple I²C bus<br>• Simple SPI bus |
| Transfer speed | | Bit rate specifiable with on-chip baud rate generator. | Bit rate specifiable with on-chip baud rate generator. |
| Full-duplex communications | | • Transmitter: Enables continuous transmission by double-buffering.<br>• Receiver: Enables continuous reception by double-buffering. | • Transmitter: Enables continuous transmission by double-buffering.<br>• Receiver: Enables continuous reception by double-buffering. |
| Data transfer | | Selectable as LSB-first or MSB-first transfer*1 | Selectable as LSB-first or MSB-first transfer*1 |
| Interrupt sources | | Transmit-end, transmit-data-empty, receive-data-full, and receive error<br>Completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode) | Transmit-end, transmit-data-empty, receive-data-full, and receive error<br>Completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode) |
| Power consumption reduction function | | Module stop state can be set for each channel. | Module stop state can be set for each channel. |
| Asynchronous mode | Data length | 7 or 8 bits | 7, 8, or 9 bits |
| | Transmission stop bit | 1 or 2 bits | 1 or 2 bits |
| | Parity | Even, odd, or none | Even, odd, or none |
| | Receive error detection | Parity, overrun, and framing errors | Parity, overrun, and framing errors |
| | Hardware flow control | CTSn and RTSn pins can be used in transfer control. | CTSn and RTSn pins can be used in transfer control. |
| | Start-bit detection | Low is detected | Low level or falling edge is selectable. |
| | Break detection | Break can be detected by reading RXDn pin level directly in case of a framing error | When a framing error occurs, a break can be detected by reading the RXDn pin level directly |

| Item | | RX210 (SCIc) | RX651 (SCIg) |
|---|---|---|---|
| Asynchronous mode | Clock source | • Selectable from internal or external clock<br>• Enables transfer rate clock input from TMR (SCI5 and SCI6) | • An internal or external clock can be selected.<br>• Transfer rate clock input from the TMR can be used. (SCI5, SCI6) |
| | Double-speed mode | — | Baud rate generator double-speed mode is selectable. |
| | Multi-processor communications function | Serial communication among multiple processors | Serial communication among multiple processors |
| | Noise cancellation | The signal paths from input on the RXDn pins incorporate digital noise filters. | The signal paths from input on the RXDn pins incorporate digital noise filters. |
| Clock synchronous mode | Data length | 8 bits | 8 bits |
| | Receive error detection | Overrun errors | Overrun errors |
| | Hardware flow control | CTSn and RTSn pins can be used in transfer control. | CTSn and RTSn pins can be used in transfer control. |
| Smart card interface mode | Error processing | An error signal can be automatically transmitted on detection of a parity error during reception | An error signal can be automatically transmitted on detection of a parity error during reception |
| | | Data can be automatically re-transmitted on receiving an error signal during transmission | Data can be automatically re-transmitted on receiving an error signal during transmission |
| | Data type | Both direct convention and inverse convention are supported. | Both direct convention and inverse convention are supported. |
| Simple $I^2C$ mode | Transfer format | $I^2C$ bus format (MSB-first transfer only) | $I^2C$ bus format (MSB-first transfer only) |
| | Operating mode | Master (single-master operation only) | Master (single-master operation only) |
| | Transfer rate | Up to 384 kbps | Fast mode is supported. |
| | Noise cancellation | The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable. | The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable. |
| Simple SPI bus | Data length | 8 bits | 8 bits |
| | Detection of errors | Overrun errors | Overrun errors |
| | SS input pin function | Applying the high level to the SS# pin can cause the output pins to enter the highimpedance state. | Applying the high level to the SS# pin can cause the output pins to enter the highimpedance state. |
| | Clock settings | Four kinds of settings for clock phase and clock sense are selectable. | Four kinds of settings for clock phase and clock sense are selectable. |
| Bit rate modulation function | | — | Correction of outputs from the on-chip baud rate generator can reduce errors. |

| Item | RX210 (SCIc) | RX651 (SCIg) |
|---|---|---|
| Event link function | Error (receive error or error signal detection) event output | Error (receive error or error signal detection) event output |
| | Receive data full event output | Receive data full event output |
| | Transmit data empty event output | Transmit data empty event output |
| | Transmit end event output | Transmit end event output |

Note 1. In simple $I^2C$ mode, only MSB-first is available

**Table 2.43 Comparative Listing of SCIc and SCIi Specifications**

| Item | | RX210 (SCIc) | RX651 (SCIi) |
|---|---|---|---|
| Number of channels | | 12 channels | 2 channels |
| Serial communications modes | | • Asynchronous operation<br>• Clock synchronous operation<br>• Smart card interface<br>• Simple I2C bus<br>• Simple SPI bus | • Asynchronous operation<br>• Clock synchronous operation<br>• Smart card interface<br>• Simple I2C bus<br>• Simple SPI bus |
| Transfer speed | | Bit rate specifiable with on-chip baud rate generator. | Bit rate specifiable with on-chip baud rate generator. |
| Full-duplex communications | | • Transmitter: Enables continuous transmission by double-buffering.<br>• Receiver: Enables continuous reception by double-buffering. | • Transmitter: Enables continuous transmission by double-buffering.<br>• Receiver: Enables continuous reception by double-buffering. |
| Data transfer | | Selectable as LSB-first or MSB-first transfer*1 | Selectable as LSB-first or MSB-first transfer*1 |
| Interrupt sources | | Transmit-end, transmit-data-empty, receive-data-full, and receive error<br>Completion of generation of a start condition, restart condition, or stop condition (for simple $I^2C$ mode) | Transmit end, transmit data empty, receive data full, receive error, receive data ready, and data match<br>Completion of generation of a start condition, restart condition, or stop condition (for simple $I^2C$ mode) |
| Power consumption reduction function | | Module stop state can be set for each channel | Module stop state can be set for each channel |
| Asynchronous mode | Data length | 7 or 8 bits | 7, 8, or 9 bits |
| | Transmission stop bit | 1 or 2 bits | 1 or 2 bits |
| | Parity | Even, odd, or none | Even, odd, or none |
| | Receive error detection | Parity, overrun, and framing errors | Parity, overrun, and framing errors |
| | Hardware flow control | CTSn and RTSn pins can be used in transfer control. | CTSn and RTSn pins can be used in transfer control. |
| | Transmit/receive FIFO | — | 16-stage FIFOs for transmit and receive buffers |
| | Data match detection | — | Compares receive data and comparison data, and generates interrupt when they are matched |
| | Start-bit detection | Low is detected | Low level or falling edge is selectable. |
| | Break detection | Break can be detected by reading RXDn pin level directly in case of a framing error | When a framing error occurs, a break can be detected by reading the RXDn pin level directly |
| | Clock source | • Selectable from internal or external clock<br>• Enables transfer rate clock input from TMR (SCI5 and SCI6) | • An internal or external clock can be selected. |
| | Double-speed mode | — | Baud rate generator double-speed mode is selectable. |

| Item | | RX210 (SCIc) | RX651 (SCIi) |
|---|---|---|---|
| Asynchronous mode | Multi-processor communications function | Serial communication among multiple processors | Serial communication among multiple processors |
| | Noise cancellation | The signal paths from input on the RXDn pins incorporate digital noise filters. | The signal paths from input on the RXDn pins incorporate digital noise filters. |
| Clock synchronous mode | Data length | 8 bits | 8 bits |
| | Receive error detection | Overrun errors | Overrun errors |
| | Hardware flow control | CTSn and RTSn pins can be used in transfer control. | CTSn and RTSn pins can be used in transfer control. |
| | Transmit/receive FIFO | — | 16-stage FIFOs for transmit and receive buffers |
| Smart card interface mode | Error processing | An error signal can be automatically transmitted on detection of a parity error during reception | An error signal can be automatically transmitted on detection of a parity error during reception |
| | | Data can be automatically re-transmitted on receiving an error signal during transmission | Data can be automatically re-transmitted on receiving an error signal during transmission |
| | Data type | Both direct convention and inverse convention are supported. | Both direct convention and inverse convention are supported. |
| Simple $I^2C$ mode | Transfer format | $I^2C$ bus format (MSB-first transfer only) | $I^2C$ bus format (MSB-first transfer only) |
| | Operating mode | Master (single-master operation only) | Master (single-master operation only) |
| | Transfer rate | Up to 384 kbps | Fast mode is supported |
| | Noise cancellation | The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable. | The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable |
| Simple SPI bus | Data length | 8 bits | 8 bits |
| | Detection of errors | Overrun errors | Overrun errors |
| | SS input pin function | Applying the high level to the SS# pin can cause the output pins to enter the high-impedance state. | Applying the high level to the SS# pin can cause the output pins to enter the high-impedance state. |
| | Clock settings | Four kinds of settings for clock phase and clock sense are selectable. | Four kinds of settings for clock phase and clock sense are selectable. |
| Bit rate modulation function | | — | Correction of outputs from the on-chip baud rate generator can reduce errors. |

Note 1. In simple $I^2C$ mode, only MSB-first is available

**Table 2.44 Comparative Listing of SCId and SCIh Specifications**

| Item | | RX210 (SCId) | RX651 (SCIh) |
|---|---|---|---|
| Number of channels | | 1 channel | 1 channel |
| Serial communications modes | | • Asynchronous operation<br>• Clock synchronous operation<br>• Smart card interface<br>• Simple I2C bus<br>• Simple SPI bus | • Asynchronous operation<br>• Clock synchronous operation<br>• Smart card interface<br>• Simple I2C bus<br>• Simple SPI bus |
| Transfer speed | | Bit rate specifiable with on-chip baud rate generator. | Bit rate specifiable with on-chip baud rate generator. |
| Full-duplex communications | | • Transmitter: Enables continuous transmission by double-buffering.<br>• Receiver: Enables continuous reception by double-buffering. | • Transmitter: Enables continuous transmission by double-buffering.<br>• Receiver: Enables continuous reception by double-buffering. |
| Data transfer | | Selectable as LSB-first or MSB-first transfer*1 | Selectable as LSB-first or MSB-first transfer*1 |
| Interrupt sources | | Transmit-end, transmit-data-empty, receive-data-full, and receive error<br>Completion of generation of a start condition, restart condition, or stop condition (for simple $I^2C$ mode) | Transmit-end, transmit-data-empty, receive-data-full, and receive error<br>Completion of generation of a start condition, restart condition, or stop condition (for simple $I^2C$ mode) |
| Power consumption reduction function | | Module stop state can be set. | Module stop state can be set. |
| Asynchronous mode | Data length | 7 or 8 bits | 7, 8, or 9 bits |
| | Transmission stop bit | 1 or 2 bits | 1 or 2 bits |
| | Parity | Even, odd, or none | Even, odd, or none |
| | Receive error detection | Parity, overrun, and framing errors | Parity, overrun, and framing errors |
| | Hardware flow control | CTSn and RTSn pins can be used in transfer control. | CTSn and RTSn pins can be used in transfer control. |
| | Start-bit detection | Low is detected | Low level or falling edge is selectable. |
| | Break detection | Break can be detected by reading RXDn pin level directly in case of a framing error | Break can be detected by reading RXDn pin level directly in case of a framing error |
| | Clock source | • Selectable from internal or external clock<br>• Enables transfer rate clock input from TMR (SCI5 and SCI6) | • Selectable from internal or external clock<br>• Enables transfer rate clock input from TMR (SCI5 and SCI6) |
| | Double-speed mode | — | Baud rate generator double-speed mode is selectable. |
| | Multi-processor communications function | Serial communication among multiple processors | Serial communication among multiple processors |
| | Noise cancellation | The signal paths from input on the RXDn pins incorporate digital noise filters. | The signal paths from input on the RXDn pins incorporate digital noise filters. |

| Item | | RX210 (SCId) | RX651 (SCIh) |
|---|---|---|---|
| Clock synchronous mode | Data length | 8 bits | 8 bits |
| | Receive error detection | Overrun errors | Overrun errors |
| | Hardware flow control | CTSn and RTSn pins can be used in transfer control. | CTSn and RTSn pins can be used in transfer control. |
| Smart card interface mode | Error processing | An error signal can be automatically transmitted on detection of a parity error during reception | An error signal can be automatically transmitted on detection of a parity error during reception |
| | | Data can be automatically re-transmitted on receiving an error signal during transmission | Data can be automatically re-transmitted on receiving an error signal during transmission |
| | Data type | Both direct convention and inverse convention are supported. | Both direct convention and inverse convention are supported. |
| Simple $I^2C$ mode | Transfer format | $I^2C$ bus format (MSB-first transfer only) | $I^2C$ bus format (MSB-first transfer only) |
| | Operating mode | Master (single-master operation only) | Master (single-master operation only) |
| | Transfer rate | Up to 384 kbps | Fast mode is supported |
| | Noise cancellation | The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable. | The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable. |
| Simple SPI bus | Data length | 8 bits | 8 bits |
| | Detection of errors | Overrun errors | Overrun errors |
| | SS input pin function | Applying the high level to the SS# pin can cause the output pins to enter the high-impedance state. | Applying the high level to the SS# pin can cause the output pins to enter the high-impedance state. |
| | Clock settings | Four kinds of settings for clock phase and clock sense are selectable. | Four kinds of settings for clock phase and clock sense are selectable. |
| Extended serial mode | Start Frame transmission | • Output of a low level as the Break Field over a specified width and generation of interrupts on completion<br>• Detection of bus collisions and the generation of interrupts on detection | • Output of a low level as the Break Field over a specified width and generation of interrupts on completion<br>• Detection of bus collisions and the generation of interrupts on detection |

| Item | | RX210 (SCId) | RX651 (SCIh) |
|---|---|---|---|
| Extended serial mode | Start Frame reception | • Detection of the Break Field low width and generation of an interrupt on detection<br>• Comparison of Control Fields 0 and 1 and generation of an interrupt when the two match<br>• Two kinds of data for comparison (primary and secondary) can be set in Control Field 1.<br>• A priority interrupt bit can be set in Control Field 1.<br>• Handling of Start Frames that do not include a Break Field<br>• Handling of Start Frames that do not include a Control Field<br>• Function for measuring bit rates | • Detection of the Break Field low width and generation of an interrupt on detection<br>• Comparison of Control Fields 0 and 1 and generation of an interrupt when the two match<br>• Two kinds of data for comparison (primary and secondary) can be set in Control Field 1.<br>• A priority interrupt bit can be set in Control Field 1.<br>• Handling of Start Frames that do not include a Break Field<br>• Handling of Start Frames that do not include a Control Field<br>• Function for measuring bit rates |
| Extended serial mode | I/O control function | • Selectable polarity for TXDX12 and RXDX12 signals<br>• Selection of a digital filter for RXDX12<br>• Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin<br>• Selectable timing for the sampling of data received through RXDX12<br>• Signals received on RXDX12 can be passed though to SCIc when the extended serial mode control section is off. | • Selectable polarity for TXDX12 and RXDX12 signals<br>• Selection of a digital filter for RXDX12<br>• Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin<br>• Selectable timing for the sampling of data received through RXDX12<br>• Signals received on RXDX12 can be passed though to SCIc when the extended serial mode control section is off. |
| | Timer function | Usable as a reloading timer | Usable as a reloading timer |
| Bit rate modulation function | | — | Correction of outputs from the on-chip baud rate generator can reduce errors. |

Note 1. In simple I²C mode, only MSB-first is available

**Table 2.45 Comparative Listing of Serial Communications Interface Channels Specifications**

| Item | RX210 (SCIc, SCId) | RX651 (SCIg, SCIi, SCIh) |
|---|---|---|
| Asynchronous mode | SCI0 to SCI12 | SCI0 to SCI12 |
| Clock synchronous mode | SCI0 to SCI12 | SCI0 to SCI12 |
| Smart card interface mode | SCI0 to SCI12 | SCI0 to SCI12 |
| Simple I²C mode | SCI0 to SCI12 | SCI0 to SCI12 |
| Simple SPI mode | SCI0 to SCI12 | SCI0 to SCI12 |
| Extended serial mode | SCI12 | SCI12 |
| TMR clock input | SCI5, SCI6, SCI12 | SCI5, SCI6, SCI12 |
| Event link function | SCI5 | SCI5 |
| FIFO mode | — | SCI10, SCI11 |

**Table 2.46 Comparative Listing of Serial Communications Interface Registers**

| Register | Bit | RX210 (SCIc, SCId) | RX651 (SCIg, SCIi, SCIh) |
|---|---|---|---|
| RDRH | — | — | Receive Data Register H |
| RDRL | — | — | Receive Data Register L |
| RDRHL | — | — | Receive Data Register HL |
| FRDR | — | — | Receive FIFO Data Register |
| TDRH | — | — | Transmit Data Register H |
| TDRL | — | — | Transmit Data Register L |
| TDRHL | — | — | Transmit Data Register HL |
| FTDR | — | — | Transmit FIFO Data Register |
| SMR | CHR | Character Length<br>(Valid only in asynchronous mode)<br><br>0: Selects 8 bits as the data length<br><br>1: Selects 7 bits as the data length | Character Length<br>(Valid only in asynchronous mode)<br>Selects in combination with the SCMR.CHR1 bit.<br><br>CHR1 CHR<br>0 0: Transmit/receive in 9-bit data length<br>0 1: Transmit/receive in 9-bit data length<br>1 0: Transmit/receive in 8-bit data length (initial value)<br>1 1: Transmit/receive in 7-bit data length |
| | CM | Communications Mode<br>0: Asynchronous mode<br><br>1: Clock synchronous mode | Communications Mode<br>0: Asynchronous mode or simple $I^2C$ mode<br><br>1: Clock synchronous mode or simple SPI mode |
| SSR | RDRF | — | Receive Data Full Flag (b6) |
| | TDRE | — | Transmit Data Empty Flag (b7) |
| SSRFIFO | — | — | Serial Status Register |
| SCMR | CHR1 | — | Character Length 1 (b4) |
| BRR | — | Bit Rate Register<br><br>In the Asynchronous mode and the Multiprocessor communication mode, the set value and the bitrate depends on SEMR.ABCS bit setting. For more related information, refer to the user's manual. | Bit Rate Register<br><br>In the Asynchronous mode and the Multiprocessor communication mode, the set value and the bitrate depends on SEMR.BGDM and SEMR.ABCS bit setting. For more related information, refer to the user's manual.<br><br>In case of SCI10 & SCI11, when SMR.CM = "1" (Clock synchronous mode or simple SPI mode), FCR.FM = "1" (FIFO mode) and SMR.CKS[1:0] ="00b", do not write the value of "00h" to BBR Register |
| MDDR | — | — | Modulation Duty Register |
| SEMR | BRME | — | Bit Rate Modulation Enable (b2) |
| | BGDM | — | Baud Rate Generator Double-Speed Mode Select (b6) |
| | RXDESEL | — | Asynchronous Start Bit Edge Detection Select (b7) |
| FCR | — | — | FIFO Control Register |
| FDR | — | — | FIFO Data Count Register |

| Register | Bit | RX210 (SCIc, SCId) | RX651 (SCIg, SCIi, SCIh) |
|---|---|---|---|
| LSR | — | — | Line Status Register |
| CDR | — | — | Comparison Data Register |
| DCCR | — | — | Data Comparison Control Register |
| SPTR | — | — | Serial Port Register |
| CR2 | BCCS [1:0] | Bus Collision Detection Clock Select<br><br>b5 b4<br>0 0: SCI base clock<br>0 1: SCI base clock frequency divided by 2<br>1 0: SCI base clock frequency divided by 4<br>1 1: Setting prohibited | Bus Collision Detection Clock Select<br><br>When SEMR.BGDM = 0 or SEMR.BGDM = 1 and SMR.CKS[1:0] = a value other than 00b<br>b5 b4<br>0 0: SCI base clock<br>0 1: SCI base clock frequency divided by 2<br>1 0: SCI base clock frequency divided by 4<br>1 1: Setting prohibited<br><br>When SEMR.BGDM = 1 and SMR.CKS[1:0] = 00b<br>b5 b4<br>0 0: SCI base clock frequency divided by 2<br>0 1: SCI base clock frequency divided by 4<br>1 0: Setting prohibited<br>1 1: Setting prohibited |

## 2.23 I²C-bus Interface

Table 2.47 shows a Comparative Listing of I²C-bus Interface Specifications, and Table 2.48 shows a Comparative Listing of I²C-bus Interface Registers.

**Table 2.47 Comparative Listing of I²C-bus Interface Specifications**

| Item | RX210 (RIIC) | RX651 (RIICa) |
|---|---|---|
| Number of channels | 1 channel | 2 channels |
| Communication format | • I2C bus format or SMBus format<br>• Master mode or slave mode selectable<br>• Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate | • I2C bus format or SMBus format<br>• Master mode or slave mode selectable<br>• Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate |
| Transfer speed | Up to 400kbps | Fast-mode Plus is supported (up to 1 Mbps) |
| SCL clock | For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%. | For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%. |
| Issuing and detection conditions | Start, restart, and stop conditions are generated automatically. Start conditions (including restart conditions) and stop conditions are detectable. | Start, restart, and stop conditions are generated automatically. Start conditions (including restart conditions) and stop conditions are detectable. |
| Slave addresses | • Up to three different slave addresses can be set.<br>• 7-bit and 10-bit address formats are supported (along with the use of both at once).<br>• General call addresses, device ID addresses, and SMBus host addresses are detectable. | • Up to three different slave addresses can be set.<br>• 7-bit and 10-bit address formats are supported (along with the use of both at once).<br>• General call addresses, device ID addresses, and SMBus host addresses are detectable. |
| Acknowledgement | • For transmission, the acknowledge bit is automatically loaded.<br>— Transfer of the next data for transmission can be automatically suspended on detection of a not-acknowledge bit.<br>• For reception, the acknowledge bit is automatically transmitted.<br>— If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible. | • For transmission, the acknowledge bit is automatically loaded.<br>— Transfer of the next data for transmission can be automatically suspended on detection of a not-acknowledge bit.<br>• For reception, the acknowledge bit is automatically transmitted.<br>— If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible. |
| Wait function | In reception, the following periods of waiting can be obtained by holding the SCL clock at the low level:<br>• Waiting between the eighth and ninth clock cycles<br>• Waiting between the ninth clock cycle and the first clock cycle of the next transfer | In reception, the following periods of waiting can be obtained by holding the SCL clock at the low level:<br>• Waiting between the eighth and ninth clock cycles<br>• Waiting between the ninth clock cycle and the first clock cycle of the next transfer |

| Item | RX210 (RIIC) | RX651 (RIICa) |
|---|---|---|
| SDA output delay function | Timing of the output of transmitted data, including the acknowledge bit, can be delayed. | Timing of the output of transmitted data, including the acknowledge bit, can be delayed. |
| Arbitration | • For multi-master operation<br>— Operation to synchronize the SCL clock in cases of conflict with the SCL signal from another master is possible.<br>— When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line.<br>— In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line.<br>• Loss of arbitration due to detection of the start condition while the bus is busy is detectable (to prevent the issuing of double start conditions).<br>• Loss of arbitration in transfer of a not-acknowledge bit due to the internal signal for the SDA line and the level on the SDA line not matching is detectable.<br>• Loss of arbitration due to non-matching of internal and line levels for data is detectable in slave transmission. | • For multi-master operation<br>— Operation to synchronize the SCL clock in cases of conflict with the SCL signal from another master is possible.<br>— When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line.<br>— In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line.<br>• Loss of arbitration due to detection of the start condition while the bus is busy is detectable (to prevent the issuing of double start conditions).<br>• Loss of arbitration in transfer of a not-acknowledge bit due to the internal signal for the SDA line and the level on the SDA line not matching is detectable.<br>• Loss of arbitration due to non-matching of internal and line levels for data is detectable in slave transmission. |
| Timeout detection function | The internal timeout function is capable of detecting long-interval stop of the SCL clock. | The internal timeout function is capable of detecting long-interval stop of the SCL clock. |
| Noise canceler | The interface incorporates digital noise filters for both the SCL and SDA signals, and the width for noise cancellation by the filters is adjustable by software. | The interface incorporates digital noise filters for both the SCL and SDA signals, and the width for noise cancellation by the filters is adjustable by software. |
| Interrupt sources | Four sources<br>• Error in transfer or occurrence of events<br>Detection of arbitration, NACK, timeout, a start condition including a restart condition, or a stop condition<br>• Receive data full (including matching with a slave address)<br>• Transmit data empty (including matching with a slave address)<br>• Transmit end | Four sources<br>• Error in transfer or occurrence of events<br>Detection of arbitration, NACK, timeout, a start condition including a restart condition, or a stop condition<br>• Receive data full (including matching with a slave address)<br>• Transmit data empty (including matching with a slave address)<br>• Transmit end |
| Low power consumption function | Module stop state can be set. | Module stop state can be set. |

| Item | RX210 (RIIC) | RX651 (RIICa) |
|---|---|---|
| RIIC operating modes | Four modes<br>Master transmit mode, master receive mode, slave transmit mode, and slave receive mode | Four modes<br>Master transmit mode, master receive mode, slave transmit mode, and slave receive mode |
| Event link function | Four sources (RIIC):<br>• Error in transfer or occurrence of events<br>Detection of arbitration, NACK, timeout, a start condition including a restart condition, or a stop condition<br>• Receive data full (including matching with a slave address)<br>• Transmit data empty (including matching with a slave address)<br>• Transmit end | Four sources (RIIC0):<br>• Error in transfer or occurrence of events<br>Detection of arbitration, NACK, timeout, a start condition including a restart condition, or a stop condition<br>• Receive data full (including matching with a slave address)<br>• Transmit data empty (including matching with a slave address)<br>• Transmit end |

**Table 2.48 Comparative Listing of I²C-bus Interface Registers**

| Register | Bit | RX210 (RIIC) | RX651 (RIICa) |
|---|---|---|---|
| ICMR2 | TMWE | Timeout internal counter write enable bit (b3) | — |
| ICFER | FMPE | — | Fast-Mode Plus Enable (b7) |
| TMOCNT | — | Timeout internal counter | — |

## 2.24 Serial Peripheral Interface

Table 2.49 shows a Comparative Listing of Serial Peripheral Interface Specifications, and Table 2.50 shows a Comparative Listing of Serial Peripheral Interface Registers.

**Table 2.49 Comparative Listing of Serial Peripheral Interface Specifications**

| Item | RX210 (RSPI) | RX651 (RSPIc) |
|---|---|---|
| Number of channels | 1 channel | 3 channels |
| RSPI transfer functions | • Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (four-wire method) or clock synchronous operation (three-wire method).<br>• Transmit-only operation is available.<br>• Capable of serial communications in master/slave mode<br>• Switching of the polarity of the serial transfer clock<br>• Switching of the phase of the serial transfer clock | • Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method).<br>• Transmit-only operation is available.<br>• Communication mode: Full-duplex or transmit-only can be selected<br>• Switching of the polarity of RSPCK<br>• Switching of the phase of RSPCK |
| Data format | • MSB first/LSB first selectable<br>• Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits.<br>• 128-bit transmit/receive buffers<br>• Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits) | • MSB first/LSB first selectable<br>• Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits.<br>• 128-bit transmit/receive buffers<br>• Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits)<br>• Byte swapping of transmit and receive data is selectable |
| Bit rate | • In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the maximum divisor is 4096).<br>• In slave mode, the externally input clock is used as the serial clock (the maximum frequency is that of PCLK divided by 8).<br>Width at high level: 4 cycles of PCLK; width at low level: 4 cycles of PCLK | • In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4096).<br>• In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 4). Width at high level: 2 cycles of PCLK; width at low level: 2 cycles of PCLK. |
| Buffer configuration | • Double buffer configuration for the transmit/receive buffers | • Double buffer configuration for the transmit/receive buffers.<br>• 128 bits for the transmit/receive buffers. |
| Error detection | • Mode fault error detection<br>• Overrun error detection<br>• Parity error detection | • Mode fault error detection<br>• Overrun error detection*1<br>• Parity error detection<br>• Underrun error detection |

| Item | RX210 (RSPI) | RX651 (RSPIc) |
|---|---|---|
| SSL control function | • Four SSL signals (SSLA0 to SSLA3) for each channel<br>• In single-master mode, SSLA0 to SSLA3 signals are output.<br>• In multi-master mode:<br>SSLA0 signal for input, and SSLA1 to SSLA3 signals for either output or unused.<br>• In slave mode:<br>SSLA0 signal for input, and SSLA1 to SSLA3 signals for unused.<br>• Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay)<br>Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units)<br>• Controllable delay from RSPCK stop to SSL output negation (SSL negation delay)<br>Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units)<br>• Controllable wait for next-access SSL output assertion (next-access delay)<br>Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units)<br>• Function for changing SSL polarity | • Four SSL pins (SSLn0 to SSLn3) for each channel<br>• In single-master mode, SSLn0 to SSLn3 pins are output.<br>• In multi-master mode:<br>SSLn0 pin for input, and SSLn1 to SSLn3 pins for either output or unused.<br>• In slave mode:<br>SSLn0 pin for input, and SSLn1 to SSLn3 pins for unused.<br>• Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay)<br>Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units)<br>• Controllable delay from RSPCK stop to SSL output negation (SSL negation delay)<br>Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units)<br>• Controllable wait for next-access SSL output assertion (next-access delay)<br>Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units)<br>• Function for changing SSL polarity |
| Control in master transfer | • A transfer of up to eight commands can be executed sequentially in looped execution.<br>• For each command, the following can be set:<br>SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay<br>• A transfer can be initiated by writing to the transmit buffer.<br>• MOSI signal value specifiable in SSL negation | • A transfer of up to eight commands can be executed sequentially in looped execution.<br>• For each command, the following can be set<br>SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay<br>• A transfer can be initiated by writing to the transmit buffer.<br>• MOSI signal value specifiable in SSL negation<br>• RSPCK auto-stop function |
| Interrupt sources | Maskable interrupt sources<br>• RSPI receive interrupt (receive buffer full)<br>• RSPI transmit interrupt (transmit buffer empty)<br>• RSPI error interrupt (mode fault, overrun, parity error)<br>• RSPI idle interrupt (RSPI idle) | Interrupt sources<br>• Receive buffer full interrupt<br>• Transmit buffer empty interrupt<br>• RSPI error interrupt (mode fault, overrun, underrun, or parity error)<br>• RSPI idle interrupt (RSPI idle) |

| Item | RX210 (RSPI) | RX651 (RSPIc) |
|---|---|---|
| Event link function (output) | The following five types of events can be output to the event link controller.<br>• Reception-buffer full event output<br>• Transmission-buffer empty event output<br>• Mode fault, overrun, or parity error event output<br>• RSPI idle event output<br>• Transmission-completed event output | The following events can be output to the event link controller. (RSPI0)<br>• Receive buffer full signal<br>• Transmit buffer empty signal<br>• Mode fault, overrun, underrun, or parity error signal<br>• RSPI idle signal<br>• Transmission-completed signal |
| Other functions | • Function for switching between CMOS output and open-drain output<br>• Function for initializing the RSPI<br>• Loopback mode | • Function for switching between CMOS output and open-drain output<br>• Function for initializing the RSPI<br>• Loopback mode |
| Low power consumption function | Module stop state can be set. | Module stop state can be set. |

Note 1. In master reception and when the RSPCK auto-stop function is enabled, an overrun error does not occur because the transfer clock is stopped at the timing of overrun error detection.

**Table 2.50 Comparative Listing of Serial Peripheral Interface Registers**

| Register | Bit | RX210 (RSPI) | RX651 (RSPIc) |
|---|---|---|---|
| SPSR | UDRF | — | Underrun Error Flag (b4) |
| | SPTEF | — | Transmit Buffer Empty Flag (b5) |
| | SPRF | — | Receive Buffer Full Flag (b7) |
| SPDR | — | RSPI Data Register<br><br>Available access size<br>• Long word access (SPDCR.SPLW = 1)<br>• Word access (SPDCR.SPLW = 0) | RSPI Data Register<br><br>Available access size<br>• Long word access (SPDCR.SPLW = 1, SPBYTE = 0)<br>• Word access (SPDCR.SPLW = 0, SPBYTE = 0)<br>• Byte access (SPDCR.SPBYT = 1) |
| SPDCR | SPBYT | — | RSPI Byte Access Specification (b6) |
| SPDCR2 | — | — | RSPI Data Control Register 2 |
| SPCR2 | SCKASE | — | RSPCK Auto-Stop Function Enable (b4) |

## 2.25 CRC Calculator

Table 2.51 shows a Comparative Listing of CRC Calculator Specifications, and Table 2.52 shows a Comparative Listing of CRC Calculator Registers.

**Table 2.51 Comparative Listing of CRC Calculator Specifications**

| Item | RX210 (CRC) | RX651 (CRCA) | |
|---|---|---|---|
| Data size | 8 bits | 8 bits | 32 bits |
| Data for CRC calculation | CRC code generated for any desired data in 8n-bit units (where n is a whole number) | CRC codes are generated for any desired data in 8n-bit units (where n is a whole number) | CRC codes are generated for any desired data in 32n-bit units (where n is a whole number) |
| CRC processor unit | Operation executed on eight bits in parallel | 8-bit parallel processing | 32-bit parallel processing |
| CRC generating polynomial | One of three generating polynomials selectable<br>• 8-bit CRC<br>— $X^8 + X^2 + X + 1$<br>• 16-bit CRC<br>— $X^{16} + X^{15} + X^2 + 1$<br>— $X^{16} + X^{12} + X^5 + 1$ | One of five generating polynomials selectable:<br>• 8-bit CRC<br>— $X^8 + X^2 + X + 1$<br>• 16-bit CRC<br>— $X^{16} + X^{15} + X^2 + 1$<br>— $X^{16} + X^{12} + X^5 + 1$ | One of five generating polynomials selectable:<br>• 32-bit CRC<br>— $X^{32} + X^{26} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$<br>— $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$ |
| CRC calculation switching | CRC code generation for LSB-first or MSB-first communication selectable | The order of the bits produced by CRC calculation can be switched for LSB first or MSB first communication | |
| Data size | Module stop state can be set. | Module stop state can be set. | |

**Table 2.52 Comparative Listing of CRC Calculator Registers**

| Register | Bit | RX210 (CRC) | RX651 (CRCA) |
|---|---|---|---|
| CRCCR | GPS[1:0]<br>GPS[2:0] | CRC Generating Polynomial Switching (b1-b0)<br><br>b1 b0<br>0 0: No calculation is executed.<br>0 1: $X^8 + X^2 + X + 1$<br>1 0: $X^{16} + X^{15} + X^2 + 1$<br>1 1: $X^{16} + X^{12} + X^5 + 1$ | CRC Generating Polynomial Switching (b2-b0)<br><br>b2 b0<br>0 0 0: No calculation is executed.<br>0 0 1: 8-bit CRC ($X^8 + X^2 + X + 1$)<br>0 1 0: 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$)<br>0 1 1: 16-bit CRC ($X^{16} + X^{12} + X^5 + 1$)<br>1 0 0: 32-bit CRC ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$)<br>1 0 1: 32-bit CRC ($X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$)<br>1 1 0: No calculation is executed.<br>1 1 1: No calculation is executed. |
| | LMS | CRC Calculation Switching (b2) | CRC Calculation Switching (b6) |
| CRCDIR | — | CRC Data Input Register (8-bits)<br><br>Available Access size<br><br>• Byte access | CRC Data Input Register (32-bits)<br><br>Available Access size<br>• Long word access (When 32-bit CRC is selected<br>• Byte access (When 16-bit or 8-bit CRC is selected |
| CRCDOR | — | CRC Data Output Register (16-bits)<br><br>Available Access size<br><br>• Word access<br>When an 8-bit CRC is in use, the valid CRC code is obtained in the lower-order byte (b7 to b0). | CRC Data Output Register (32-bits)<br><br>Available Access size<br>• Long word access (When 32-bit CRC is selected)<br>• Word access (When 16-bit CRC is selected)<br>• Byte access (When 8-bit CRC is selected) |

## 2.26 12-Bit A/D Converter

Table 2.53 shows a Comparative Listing of 12-Bit A/D Converter Specifications, and Table 2.54 shows a Comparative Listing of 12-Bit A/D Converter Registers.

**Table 2.53 Comparative Listing of 12-Bit A/D Converter Specifications**

| Item | RX210 (S12ADb) | RX651 (S12ADFa) |
|---|---|---|
| Number of units | 1 unit | 2 unit (S12AD, S12AD1) |
| Input channels | Up to 16 channels | • 8 channels for S12AD<br>• 21 channels for S12AD1<br>+ 1 extension |
| Extended analog function | Temperature sensor output, internal reference voltage | Temperature sensor output, internal reference voltage |
| A/D conversion method | Successive approximation method | Successive approximation method |
| Resolution | 12 bits | 12 bits |
| Conversion time | • 1.0μs per channel<br>(when A/D conversion clock ADCLK = 50 MHz) | • 0.48 μs per channel (12-bit conversion mode)<br>• 0.45 μs per channel (10-bit conversion mode)<br>• 0.42 μs per channel (8-bit conversion mode)<br>(A/D conversion clock: when ADCLK operates at 60 MHz) |
| A/D conversion clock | Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency division ratio should be one of the following.<br>PCLK to ADCLK frequency division ratio = 1:1, 1:2, 1:4, 1:8, 2:1, 4:1<br>ADCLK is set using the clock generation circuit | Peripheral module clock PCLK*1 and A/D conversion clock ADCLK*1 can be set so that the frequency ratio should be one of the following.<br>PCLK to ADCLK frequency ratio = 1:1, 2:1, 4:1, 8:1<br>ADCLK is set using the clock generation circuit |

| Item | RX210 (S12ADb) | RX651 (S12ADFa) |
|---|---|---|
| Data register | • For analog input: 16 data registers<br>• For duplication of A/D conversion data in double trigger mode: One data register | • 29 registers for analog input (eight for S12AD and 21 for S12AD1), 1 for A/D-converted data duplication in double trigger mode per unit, and 2 for A/D-converted data duplication during extended operation in double trigger mode per unit. |
| | • For temperature sensor: One data register<br>• For internal reference voltage: One data register | • One register for temperature sensor (S12AD1)<br>• One register for internal reference (S12AD1)<br>• One register for self-diagnosis per unit |
| | • The A/D conversion result is stored in 12-bit A/D data registers. | • The results of A/D conversion are stored in 12-bit A/D data registers.<br>• 8-, 10-, and 12-bit accuracy output for the results of A/D conversion |
| | • In addition mode, A/D conversion results are added and stored in A/D data registers as 14-bit data.<br>• Duplication of A/D conversion data | • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode. |
| | • A/D conversion data of one selected analog input channel is stored into A/D data register y when conversion is started by the first trigger and into the duplication register when started by the second trigger.<br>Duplication is available only in double trigger mode in single scan mode or group scan mode. | • Double trigger mode (selectable in single scan and group scan modes):<br>The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register.<br>• Extended operation in double trigger mode (available for specific triggers):<br>A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger. |

| Item | RX210 (S12ADb) | RX651 (S12ADFa) |
|---|---|---|
| Operating modes | • Single scan mode:<br>— A/D conversion is performed for only once on the analog inputs of up to 16 arbitrarily selected channels.<br>— A/D conversion is performed only once on the temperature sensor output.<br>— A/D conversion is performed only once on the internal reference voltage. | • Single scan mode:<br>— A/D conversion is performed only once on the analog inputs arbitrarily selected.<br>— A/D conversion is performed only once on the temperature sensor output (S12AD1).<br>— A/D conversion is performed only once on the internal reference voltage (S12AD1).<br>— A/D conversion is performed only once on the extended analog input (S12AD1). |
| | • Continuous scan mode:<br>— A/D conversion is performed repeatedly on the analog inputs of up to 16 arbitrarily selected channels. | • Continuous scan mode:<br>— A/D conversion is performed repeatedly on the analog input, temperature sensor output (S12AD1), and internal reference voltage (S12AD1) of the arbitrarily selected channel.<br>— A/D conversion is performed repeatedly on the extended analog input (S12AD1). |

| Item | RX210 (S12ADb) | RX651 (S12ADFa) |
|---|---|---|
| Operating modes | | • Group scan mode:<br>— Two (groups A and B) or three (groups A, B, and C) can be selected as the number of the groups to be used. Only the combination of groups A and B can be selected when the number of the groups is two.<br>— Analog inputs, temperature sensor output (S12AD1), and internal reference voltage (S12AD1) that are arbitrarily selected are divided into two groups (group A and B) or three groups (group A, B, and C), and A/D conversion of the analog input selected on a group basis is performed only once.<br>— The conditions for scanning start of groups A, B, and C (synchronous trigger) can be independently selected, thus allowing A/D conversion of each group to be started independently. |
| | • Group scan mode:<br>— Up to 16 channels of analog inputs are divided into group A and group B and A/D conversion is performed only once on all the selected channels on a group basis. The scan start conditions of group A and group B can be independently selected, thus allowing A/D conversion of group A and group B to be started independently | • Group scan mode (when group priority control selected):<br>— If a priority-group trigger is input during scanning of the low-priority group, scan of the low-priority group is stopped and scan of the priority group is started. The priority order is group A (highest) > group B > group C (lowest).<br>— Whether or not to restart scanning of the low-priority group after processing for the high-priority group completes, is selectable. Rescan can also be set to start either from the beginning of the selected channel or the channel on which A/D conversion is not completed. |

| Item | RX210 (S12ADb) | RX651 (S12ADFa) |
|---|---|---|
| Conditions for A/D conversion start | • Software trigger<br>• Synchronous trigger<br>Trigger by MTU, ELC, or temperature sensor<br>• Asynchronous trigger<br>A/D conversion can be triggered from the ADTRG0# pin | • Software trigger<br>• Synchronous trigger<br>Trigger by the multi-function timer pulse unit (MTU), 8-bit timer (TMR), 16-bit timer pulse unit (TPU), or event link controller (ELC).<br>• Asynchronous trigger<br>A/D conversion can be triggered by the external trigger ADTRG0# (S12AD) or ADTRG1# (S12AD1) pin (independently for two units). |
| Functions | • Sample-and-hold function<br>• Channel-dedicated sample-and-hold function (0.25 V ≤ analog voltage input ≤ AVCC0 - 0.25 V)<br>• Variable sampling state count<br>• Self-diagnosis of 12-bit A/D converter<br>• A/D-converted value addition mode<br>• Analog input disconnection detection assist<br>• Double trigger mode (duplication of A/D conversion data) | • Channel-dedicated sample-and-hold function (three channels for S12AD only)<br>• Variable sampling state count (settable for each channel)<br>• Self-diagnosis of 12-bit A/D converter<br>• Selectable A/D-converted value addition mode or average mode<br>• Analog input disconnection detection assist function (discharge function/precharge function)<br>• Double trigger mode (duplication of A/D conversion data)<br>• 12-/10-/8-bit conversion switching<br>• Automatic clear function of A/D data registers<br>• Extended analog input<br>• Comparison function (windows A and B) |

| Item | RX210 (S12ADb) | RX651 (S12ADFa) |
|---|---|---|
| Interrupt sources | • In the modes except double trigger mode and group scan mode, A/D scan end interrupt (S12ADI0) request can be generated on completion of single scan.<br>• In double trigger mode, A/D scan end interrupt (S12ADI0) request can be generated on completion of double scan.<br>• In group scan mode, A/D scan end interrupt (S12ADI0) request can be generated on completion of group A scan, whereas A/D scan end interrupt specially for group B (GBADI) request can be generated on completion of group B scan.<br>• In group scan mode with double trigger mode, A/D scan end interrupt (S12ADI0) request can be generated on completion of double scan of group A, whereas A/D scan end interrupt specially for group B (GBADI) request can be generated on completion of group B scan.<br>• S12ADI0 or GBADI interrupt can activate DMA controller (DMAC) or data transfer controller (DTC). | • In the modes except double trigger mode and group scan mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of single scan. (independently for two units).<br>• In double trigger mode, a scan end interrupt request (S12ADI or 12ADI1) can be generated on completion of double scan. (independently for two units).<br>• In group scan mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of group A scan, whereas a scan end interrupt request (GBADI or GBADI1) for group B can be generated on completion of group B scan, and a group C scan end interrupt request (GCADI or GCADI1) can be generated on completion of group C scan.<br>• When double trigger mode is selected in group scan mode, an A/D scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of double scan of group A, and the corresponding scan end interrupt request (GBADI/GCADI or GBADI1/GCADI1) can be generated on completion of group B and group C scan.<br>• A compare interrupt request (S12CMPAI, S12CMPAI1, S12CMPBI, or S12CMPBI1) can be generated upon a match with the comparison condition for the digital compare function.<br>• The S12ADI/S12ADI1, GBADI/GBADI1, and GCADI/GCADI1 interrupts can activate the DMA controller (DMAC) and data transfer controller (DTC). |
| Event link | • An ELC event can be generated on completion of scans except for group B scan in group scan mode.<br>• A/D conversion can be started by the trigger from ELC. | • An ELC event is generated upon completion of all scans<br>• Able to start scanning by a trigger from the ELC |
| Low power consumption function | Module stop state can be specified | Module stop state can be specified |

**Table 2.54 Comparative Listing of 12-Bit A/D Converter Registers**

| Register | Bit | RX210 (S12AD) | RX651 (S12ADFa) |
|---|---|---|---|
| ADDRy | — | A/D Data Registers y (y = 0 to 15) | A/D Data Registers y (y = 0 to 20)<br>(y = 0 to 7: S12AD,<br>y = 0 to 20: S12AD1) |
| ADDBLDR | AD[11:0]<br>— | — | — |
| ADDBLDRA | — | — | A/D data duplication register A |
| ADDBLDRB | — | — | A/D data duplication register B |
| ADTSDR | AD[11:0]<br>— | — | — |
| ADOCDR | AD[11:0]<br>— | — | — |
| ADRD | AD[11:0]<br>— | —<br>12-bit A/D-converted value<br>ADCER.ADRFMT = 0 (Setting for right-alignment) (b11-b0)<br>ADCER.ADRFMT = 1 (Setting for left-alignment) (b15-b4) | —<br>12-bit A/D-converted value<br>ADCER.ADRFMT = 0 (Setting for right-alignment) (b11-b0)<br>ADCER.ADRFMT = 1 (Setting for left-alignment) (b15-b4)<br><br>10-bit A/D-converted value<br>ADCER.ADRFMT = 0 (Setting for right-alignment) (b9-b0)<br>ADCER.ADRFMT = 1 (Setting for left-alignment) (b15-b6)<br><br>8-bit A/D-converted value<br>ADCER.ADRFMT = 0 (Setting for right-alignment) (b7-b0)<br>ADCER.ADRFMT = 1 (Setting for left-alignment) (b15-b8) |
| | DIAGST[1:0]<br>— | Self-Diagnosis Status | Self-Diagnosis Status |
| ADCSR | GBADIE | Group B Scan End Interrupt Enable<br>0: Disables GBADI interrupt generation upon group B scan completion.<br>1: Enables GBADI interrupt generation upon group B scan completion. | Group B Scan End Interrupt Enable<br>0: Disables interrupt generation upon group B scan completion.<br>1: Enables interrupt generation upon group B scan completion. |
| | ADIE | Scan End Interrupt Enable<br>0: Disables S12ADI0 interrupt generation upon scan completion.<br>1: Enables S12ADI0 interrupt generation upon scan completion. | Scan End Interrupt Enable<br>0: Disables interrupt generation upon scan completion.<br>1: Enables interrupt generation upon scan completion. |

| Register | Bit | RX210 (S12AD) | RX651 (S12ADFa) |
|---|---|---|---|
| ADANSA<br>ADANSA0 | — | A/D Channel Select Register A | A/D Channel Select Register A0 |
| | ANSA[15:0]<br>ANSAn<br>(n = 000 to 007) | A/D Conversion Channels Select (b15-b0)<br><br>0: AN000 to AN015 are not subjected to conversion.<br>1: AN000 to AN015 are subjected to scan conversion. | A/D Conversion Channel Select (b7-b0)<br><br>0: AN000 to AN007 are not subjected to conversion.<br>1: AN000 to AN007 are subjected to conversion. |
| ADANSA1 | — | — | A/D Channel Select Register A1 |
| ADANSB<br>ADANSB0 | — | A/D Channel Select Register B | A/D Channel Select Register B0 |
| | ANSB[15:0]<br>ANSBn<br>(n = 000 to 007) | A/D Conversion Channels Select (b15-b0)<br><br>0: AN000 to AN015 are not subjected to conversion.<br>1: AN000 to AN015 are subjected to scan conversion. | A/D Conversion Channel Select (b7-b0)<br><br>0: AN000 to AN007 are not subjected to conversion.<br>1: AN000 to AN007 are subjected to conversion. |
| ADANSB1 | — | — | A/D Channel Select Register B1 |
| ADANSC0 | — | — | A/D Channel Select Register C0 |
| ADANSC1 | — | — | A/D Channel Select Register C1 |
| ADADS<br>ADADS0 | — | A/D-Converted Value Addition Mode Select Register | A/D-Converted Value Addition/Average Function Select Register 0 |
| | ADS[15:0]<br>ADSn<br>(n = 000 to 007) | A/D-Converted Value Addition Channel Select<br>0: A/D-converted value addition mode for AN000 to AN015 is not selected.<br>1: A/D-converted value addition mode for AN000 to AN015 is selected. | A/D-Converted Value Addition/ Average Channel Select<br>0: A/D-converted value addition/average mode for AN000 to AN007 is not selected.<br>1: A/D-converted value addition/average mode for AN000 to AN007 is selected. |
| ADADS1 | — | — | A/D-Converted Value Addition/Average Function Select Register 1 |
| ADADC | — | A/D-Converted Value Addition Count Select Register | A/D-Converted Value Addition/Average Count Select Register |
| | ADC[1:0]<br>ADC[2:0] | Addition Count Select (b1-b0)<br>b1 b0<br>0 0: 1-time conversion (no addition; same as normal conversion)<br>0 1: 2-time conversion (addition once)<br>1 0: 3-time conversion (addition twice)<br>1 1: 4-time conversion (addition three times) | Addition Count Select (b2-b0)<br>b2 b0<br>0 0 0: 1-time conversion (no addition; same as normal conversion)<br>0 0 1: 2-time conversion (addition once)<br>0 1 0: 3-time conversion (addition twice)*1<br>0 1 1: 4-time conversion (addition three times)<br>1 0 1: 16-time conversion (addition 15 times)*1<br>Settings other than above are prohibited. |

| Register | Bit | RX210 (S12AD) | RX651 (S12ADFa) |
|---|---|---|---|
| ADADC | AVEE | — | Average Mode Enable (b7) |
| ADCER | ADPRC[1:0] | — | A/D Conversion Resolution Setting (b2-b1) |
| | ACE | Automatic Clearing Enable | A/D Data Register Automatic Clearing Enable |
| ADSTRGR | TRSB[3:0]<br>TRSB[5:0] | A/D Conversion Start Trigger Select<br>for Group B (b3-b0) | A/D Conversion Start Trigger Select<br>for Group B (b5-b0) |
| | TRSA[3:0]<br>TRSA[5:0] | A/D Conversion Start Trigger Select (b11-b8) | A/D Conversion Start Trigger Select (b13-b8) |
| ADEXICR | TSSAD | — | Temperature Sensor Output A/D Converted Value Addition/Averaging Mode Select (b0) |
| | TSS<br>TSSA | Temperature Sensor Output A/D Conversion Select<br><br>0: A/D conversion of temperature sensor output is not performed<br>1: A/D conversion of temperature sensor output is performed | Temperature Sensor Output A/D Conversion Select<br><br>Conversion for group A in single scan mode, sequence scan mode, and group scan mode |
| | OCS<br>OCSA | Internal Reference Voltage A/D Conversion Select | Internal Reference Voltage A/D Conversion Select |
| | TSSB | — | Temperature Sensor Output A/D Conversion Select (b10) |
| | OCSB | — | Internal Reference Voltage A/D Conversion Select (b11) |
| | EXSEL[1:0] | — | Extended Analog Input Select (b14-b13) |
| | EXCEN | — | Extended Analog Output Control (b15) |
| ADGCEXCR | — | — | A/D Group C Extended Input Control Register |
| ADGCTRGR | — | — | A/D Group C Trigger Select Register |
| ADSSTRn | — | A/D Sampling State Register n (n = 0 to 7, L, T, O) | A/D Sampling State Register n (n = 0 to 15, L, T, O) |
| | SST[7:0]<br>— | Sampling Time Setting<br><br>The set value for sampling time should be 12 or more states and 255 or less states. | Sampling Time Setting |
| ADSHMSR | — | — | A/D Sample-and-Hold Operating Mode Select Register |
| ADGSPCR | — | — | A/D Group Scan Priority Control Register |
| ADCMPCR | — | — | A/D Comparison Function Control Register |
| ADCMPANSR0 | — | — | A/D Comparison Function Window A Channel Select Register 0 |
| ADCMPANSR1 | — | — | A/D Comparison Function Window A Channel Select Register 1 |

| Register | Bit | RX210 (S12AD) | RX651 (S12ADFa) |
|---|---|---|---|
| ADCMPANSER | — | — | A/D Comparison Function Window A Extended Input Select Register |
| ADCMPLR0 | — | — | A/D Comparison Function Window A Comparison Condition Setting Register 0 |
| ADCMPLR1 | — | — | A/D Comparison Function Window A Comparison Condition Setting Register 1 |
| ADCMPLER | — | — | A/D Comparison Function Window A Extended Input Comparison Condition Setting Register |
| ADCMPDR0 | — | — | A/D Comparison Function Window A Lower Level Setting Register |
| ADCMPDR1 | — | — | A/D Comparison Function Window A Upper Level Setting Register |
| ADCMPSR0 | — | — | A/D Comparison Function Window A Channel Status Register 0 |
| ADCMPSR1 | — | — | A/D Comparison Function Window A Channel Status Register 1 |
| ADCMPSER | — | — | A/D Comparison Function Window A Extended Input Channel Status Register |
| ADWINMON | — | — | A/D Comparison Function Window A/B Status Monitoring Register |
| ADCMPBNSR | — | — | A/D Comparison Function Window B Channel Select Register |
| ADWINLLB | — | — | A/D Comparison Function Window B Lower Level Setting Register |
| ADWINULB | — | — | A/D Comparison Function Window B Upper Level Setting Register |
| ADCMPBSR | — | — | A/D Comparison Function Window B Channel Status Register |
| ADSAM | — | — | A/D Conversion Time Setting Register |
| ADSAMPR | — | — | A/D Conversion Time Setting Protection Release Register |

## 2.27 D/A Converter

Table 2.55 shows a Comparative Listing of D/A Converter Specifications, and Table 2.56 shows a Comparative Listing of D/A Converter Registers.

**Table 2.55 Comparative Listing of D/A Converter Specifications**

| Item | RX210 (DA) | RX651 (R12DA) |
|---|---|---|
| Resolution | 10 bits | 12 bits |
| Output channel | 2 channels | 2 channels |
| Countermeasure against mutual interference between analog modules | — | Measure against interference between D/A and A/D conversion:<br>D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable input signal from the 12-bit A/D converter (unit 1).<br>Therefore, the degradation of A/D conversion accuracy due to interference is reduced by controlling the timing in which the 12-bit D/A converter inrush current occurs, with the enable signal. |
| Low power consumption function | Module stop state can be set. | Module stop state can be set. |
| Event link function (input) | DA0 conversion can be started when an event signal is input. | DA0 conversion can be started when an event signal is input. |
| Output buffer amplifier control function | — | Buffered output (gain = 1) or unbuffered can be selected. |

**Table 2.56 Comparative Listing of D/A Converter Registers**

| Register | Bit | RX210 (DA) | RX651 (R12DA) |
|---|---|---|---|
| DADRm | — | D/A Data Register m (DADRm) (m = 0, 1)<br><br>10-bit data can be relocated by setting the DPSEL bit in DADPR. | D/A Data Register m (DADRm) (m = 0, 1)<br><br>12-bit data can be relocated by setting the DADPR.DPSEL bit. |
| DAADSCR | — | — | D/A A/D Synchronous Start Control Register |
| DAADUSR | — | — | D/A A/D Synchronous Unit Select Register |
| DAAMPCR | — | — | D/A Output Amplifer Control Register |
| DAASWCR | — | — | D/A Output Amplifer Stabilization Wait Control Register |

## 2.28 Temperature Sensor

Table 2.57 shows a Comparative Listing of Temperature Sensor Specification, and Table 2.58 shows a Comparative Listing of Temperature Sensor Registers.

**Table 2.57 Comparative Listing of Temperature Sensor Specification**

| Item | RX210 (TEMPSa) | RX651 (TEMPS) |
|---|---|---|
| Temperature sensor voltage output | Temperature sensor outputs a voltage to the 12-bit A/D converter via a programmable gain amplifier (PGA). | Temperature sensor outputs a voltage to the 12-bit A/D converter unit 1. |
| Low-power consumption function | Module stop state can be set. | Module stop state can be set. |
| Temperature Sensor Calibration Data | — | Reference data measured for each chip at factory shipment is stored. |

**Table 2.58 Comparative Listing of Temperature Sensor Registers**

| Register | Bit | RX210 (TEMPSa) | RX651 (TEMPS) |
|---|---|---|---|
| TSCR | PGAGAIN [1:0] | PGA Gain Select (b1-b0) | — |
| | TSOE | — | Temperature Sensor Output Enable (b4) |
| | PGAEN | PGA Enable (b6) | — |
| TSCDR | — | — | Temperature Sensor Calibration Data Register |

## 2.29 Data Operation Circuit

Table 2.59 shows a Comparative Listing of Temperature Sensor RegistersComparative Listing of Data Operation Circuit Specification.

**Table 2.59 Comparative Listing of Data Operation Circuit Specification**

| Item | RX210 (DOC) | RX651 (DOC) |
|---|---|---|
| Data operation function | 16-bit data comparison, addition, and subtraction | 16-bit data comparison, addition, and subtraction |
| Lower power consumption function | Module stop state can be set. | Module stop state can be set. |
| Interrupts | • The condition selected by the DOCR.DCSEL bit being met<br>• The result of data addition being greater than FFFFh<br>• The result of data subtraction being less than 0000h | • The compared values either match or mismatch<br>• The result of data addition is greater than FFFFh<br>• The result of data subtraction is less than 0000h |
| Event link function (output) | — | • The compared values either match or mismatch<br>• The result of data addition is greater than FFFFh<br>• The result of data subtraction is less than 0000h |

## 2.30 RAM

Table 2.60 shows a Comparative Listing of RAM Specifications, and Table 2.61 shows a Comparative Listing of RAM Registers.

**Table 2.60 Comparative Listing of RAM Specifications**

| Item | RX210 | RX651 (Without ECC Error Correction) |
|---|---|---|
| RAM capacity | • 96KB<br>RAM0: 64KB, RAM1: 32KB<br>• 64KB<br>RAM0: 64KB<br>• 32KB<br>RAM0: 32KB<br>• 20KB<br>RAM0: 20KB<br>• 16KB<br>RAM0: 16KB<br>• 12KB<br>RAM0: 12KB | 256 KB<br>RAM0: 256 KB |
| RAM address | • RAM Capacity 96KB<br>RAM0: 0000 0000h to 0000 FFFFh<br>RAM1: 0001 0000h to 0001 7FFFh<br>• RAM Capacity 64KB<br>RAM0: 0000 0000h to 0000 FFFFh<br>RAM1: None<br>• RAM Capacity 32KB<br>RAM0: 0000 0000h to 0000 7FFFh<br>RAM1: None<br>• RAM Capacity 20KB<br>RAM0: 0000 0000h to 0000 4FFFh<br>RAM1: None<br>• RAM Capacity 16KB<br>RAM0: 0000 0000h to 0000 3FFFh<br>RAM1: None<br>• RAM Capacity 12KB<br>RAM0: 0000 0000h to 0000 2FFFh<br>RAM1: None | RAM0: 0000 0000h to 0003 FFFFh |
| Access | • Single-cycle access is possible for both reading and writing.<br>• On-chip RAM can be enabled or disabled | • Single-cycle access is possible for both reading and writing.*1<br>• Enabling or disabling of the RAM is selectable. |
| Data retention function | Not available in deep software standby mode. | Not available in deep software standby mode (Data in Standby RAM can be retained) |
| Low power consumption function | The module-stop state is independently selectable for RAM0 and RAM1. | The module-stop state is selectable. |
| Error checking function | — | • Detection of 1-bit errors<br>• A non-maskable interrupt or interrupt is generated in response to an error. |

Note 1. When accessing across the 8-byte boundary, the number of cycles is doubled.

**Table 2.61 Comparative Listing of RAM Registers**

| Register | Bit | RX210 | RX651 |
|---|---|---|---|
| RAMMODE | — | — | RAM Operating Mode Control Register |
| RAMSTS | — | — | RAM Error Status Register |
| RAMECAD | — | — | RAM Error Address Capture Register |
| RAMPRCR | — | — | RAM Protection Register |

## 2.31 Flash Memory (Code Flash)

Table 2.62 shows a Comparative Listing of Flash Memory (Code Flash) Specifications, and Table 2.63 shows a Comparative Listing of Flash Memory Registers.

**Table 2.62 Comparative Listing of Flash Memory (Code Flash) Specifications**

| Item | RX210 | RX651 |
|---|---|---|
| Memory space | • User area: 1 Mbyte max.<br>• User boot area: 16 Kbytes | User area: 1 Mbyte max. |
| ROM cache | — | • Capacity: 256 Bytes<br>• Mapping method: 8-way set associative<br>• Replace method: LRU method<br>• Line size: 16 bytes |
| Read cycle | A read operation takes one cycle of ICLK | When the cache is hit: One cycle<br>When the cache is missed:<br>One cycle if ICLK ≤ 50 MHz<br>Two cycles if 50 MHz < ICLK ≤ 100 MHz<br>Three cycles if ICLK > 100 MHz |
| Value after erase | FFh | FFh |
| Programming/erasing method | • The chip incorporates a dedicated sequencer (FCU) for programming of the ROM.<br>• Programming and erasing the ROM are handled by issuing commands to the FCU.<br>• FFFF FFFFh is read from the erased ROM in 32 bits. | • The chip incorporates a dedicated sequencer (FCU) for programming and erasure of the flash memory.<br>• Programming and erasing the code flash memory is handled by the FACI commands specified in the FACI command issuing area (007E 0000h)<br>• Programming/erasure through transfer by a dedicated flash-memory programmer via a serial interface (serial programming)<br>• Programming/erasure of flash memory by a user program (self-programming) |
| Security function | Protects against illicit tampering with or reading out of data in flash memory | Protects against illicit tampering with or reading out of data in flash memory |
| Protection function | • Software Protection:<br>The ROM programming/erasure is prohibited by the settings of the control registers or user area lock bit.<br>• Command-Locked State P/E<br>The FCU detects malfunctions caused by FCU command issuance errors and prohibited access occurrences, and an FCU command is prohibited from being received. | Protects against erroneous programming of the flash memory |
| Trusted Memory (TM) function | — | Protects against illicit reading of blocks 8 and 9 in the code flash memory |

| Item | RX210 | RX651 |
|---|---|---|
| Background Operation (BGO) | • Execution of program code from the ROM is possible while the E2 DataFlash memory is being programmed or erased.<br>• The CPU is able to execute program code from areas other than the ROM or E2 DataFlash while the ROM is being programmed or erased. | — |
| Suspension and resumption | • The CPU is able to execute program code from the ROM during suspension of programming or erasure.<br>• Programming and erasure of the ROM can be restarted (resumed) after suspension. | • The CPU is able to execute program code from the Code Flash during suspension of programming or erasure.<br>• Programming and erasure of the Code Flash can be restarted (resumed) after suspension. |
| Units of programming and erasure | • Units of programming for the user area or user boot area: 2, 8, or 128 bytes<br>• Units of erasure for the user area: In block units<br>• Units of erasure for the user boot area: 16 Kbytes | • Units of programming for the user area: 128 bytes<br>• Units of erasure for the user area: Block units |
| Other functions | — | Interrupts can be accepted during self-programming (When interrupt and exception vector addresses are set other than code flash memory.) |
| | — | The startup area of the code flash memory is selectable from blocks 0 and 1. |

| Item | RX210 | RX651 |
|---|---|---|
| On-board programming | • Reprogramming in boot mode<br>— The clock synchronous serial interface (SCI1) is used.<br>— The bit rate is automatically adjusted.<br>— The user boot area is also programmable<br>• Reprogramming in user boot mode<br>— The user-specific boot program can be programmed.<br>• Reprogramming using the ROM reprogramming routine in the user program<br>— ROM is reprogrammable without resetting the system. | • Programming/erasure in boot mode (for the SCI interface)<br>— The asynchronous serial interface (SCI1) is used.<br>— The transfer rate is adjusted automatically.<br>• Programming/erasure in boot mode (for the USB interface)<br>— USBb is used<br>— Dedicated hardware is not required, so direct connection to a PC is possible.<br>• Programming/erasure in boot mode (for the FINE interface)<br>— FINE is used.<br>• Programming/erasure by a routine for code flash memory programming within the user program<br>— This allows code flash memory programming without resetting the system |
| Programming and Erasure by Dedicated Parallel Programmer | A PROM programmer can be used to program the user area and user boot area. | A flash programmer can be used to program or erase the user area. |
| Unique ID | — | 16-byte ID code provided for each MCU |

**Table 2.63 Comparative Listing of Flash Memory Registers**

| Register | Bit | RX210 | RX651 |
|---|---|---|---|
| FWEPROR | — | Flash Write Erase Protection Register | Flash P/E Protect Register |
| | FLWE[1:0] | Flash Programming/Erasure | Flash Programming and Erasure Enable |
| FMODR | — | Flash Mode Register | — |
| FASTAT | DFLWPE | E2 DataFlash Programming/Erasure Protection Violation (b0) | — |
| | DFLRPE | E2 DataFlash Read Protection Violation (b1) | — |
| | DFLAE | E2 DataFlash Access Violation (b3) | — |
| | ROMAE | ROM Access Violation (b7) | — |
| | CFAE | — | Code Flash Memory Access Violation Flag (b7) |

| Register | Bit | RX210 | RX651 |
|---|---|---|---|
| FAEINT | DFLWPEIE | E2 DataFlash Programming/Erasure Protection Violation Interrupt Enable (b0) | — |
| | DFLRPEIE | E2 DataFlash Read Protection Violation Interrupt Enable (b1) | — |
| | DFLAEIE | E2 DataFlash Access Violation Interrupt Enable (b3) | — |
| | ROMAEIE | ROM Access Violation Interrupt Enable (b7) | — |
| | CFAEIE | — | Code Flash Memory Access Violation Interrupt Enable (b7) |
| FSADDR | — | — | FACI Command Start Address Register |
| FCURAME | — | FCU RAM Enable Register | — |
| FSTATR0 | — | Flash Status Register 0 | — |
| FSTATR1 | — | Flash Status Register 1 | — |
| FSTATR | — | — | Flash Status Register |
| FENTRYR | FENTRY0 | ROM P/E Mode Entry 0 (b0) | — |
| | FENTRYC | — | Code Flash Memory P/E Mode Entry (b0) |
| | FENTRY1 | ROM P/E Mode Entry 1 (b1) | — |
| | FENTRYD | E2 DataFlash P/E Mode Entry (b7) | — |
| | FEKEY[7:0]<br>KEY[7:0] | Key Code (b15-b8) | Key Code (b15-8) |
| FPROTR | — | Flash Protection Register | — |
| FRESETR | — | Flash Reset Register | — |
| FCMDR | — | FCU Command Register | FACI Command Register |
| FSUINITR | — | — | Flash Sequencer Set-Up Initialization Register |
| FAWMON | — | — | Flash Access Window Monitor Register |
| FCPSR | — | FCU Processing Switching Register | Flash Sequencer Processing Switching Register |
| | ESUSPMD | Programming/Erasure Suspend Mode<br>0: Suspension priority mode<br>1: Programming/erasure priority mode | Erasure Suspend Mode<br>0: Suspension priority mode<br>1: Erasure priority mode |
| FPESTAT | — | Flash P/E Status Register | — |
| FPCKAR | — | — | Flash Sequencer Processing Clock Notification Register |
| FSUACR | — | — | Start-Up Area Control Register |
| PCKAR | — | Peripheral Clock Notification Register | — |
| ROMCE | — | — | ROM Cache Enable Register |
| ROMCIV | — | — | ROM Cache Invalidate Register |
| UIDRn | — | — | Unique ID Register n (n = 0 to 3) |

# 3. Comparison of Pin Functions

A comparison of the pin functions, power supply, clock, system control pins is provided below.

Blue character : Items that exist only in either group.

Red character : Items that exist in both group, but they have differences.

Black character : Items that are same specification.

## 3.1 144pin Package

Table 3.1 shows a Comparative Listing of Pin Functions (144pin Package).

**Table 3.1 Comparative Listing of Pin Functions (144pin Package)**

| 144pin LFQFP | RX210 | RX651 |
|---|---|---|
| 1 | AVSS0 | AVSS0 |
| 2 | P05/DA1 | P05/IRQ13/DA1 |
| 3 | VREFH | AVCC1 |
| 4 | P03/DA0 | P03/IRQ11/DA0 |
| 5 | VREFL | AVSS1 |
| 6 | P02/TMCI1/SCK6 | P02/TMCI1/SCK6/IRQ10/AN120 |
| 7 | P01/TMCI0/RXD6/SMISO6/SSCL6 | P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/AN119 |
| 8 | P00/TMRI0/TXD6/SMOSI6/SSDA6 | P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/AN118 |
| 9 | PF5/IRQ4 | PF5/IRQ4 |
| 10 | NC | EMLE |
| 11 | PJ5 | PJ5/POE8#/CTS2#/RTS2#/SS2# |
| 12 | VSS | VSS |
| 13 | PJ3/MTIOC3C/CTS6#/RTS6#/SS6#/CTS0#/RTS0#/SS0# | PJ3/EDACK1/MTIOC3C/CTS6#/RTS6#/CTS0#/RTS0#/SS6#/SS0# |
| 14 | VCL | VCL |
| 15 | PJ1/MTIOC3A | VBATT |
| 16 | MD/FINED | MD/FINED |
| 17 | XCIN | XCIN |
| 18 | XCOUT | XCOUT |
| 19 | RES# | RES# |
| 20 | XTAL/P37 | XTAL/P37 |
| 21 | VSS | VSS |
| 22 | EXTAL/P36 | EXTAL/P36 |
| 23 | VCC | VCC |
| 24 | P35/NMI | UPSEL/P35/NMI |
| 25 | P34/MTIOC0A/TMCI3/POE2#/SCK6/SCK0/IRQ4 | TRST#/P34/MTIOC0A/TMCI3/PO12/POE10#/SCK6/SCK0/IRQ4 |
| 26 | P33/MTIOC0D/TMRI3/POE3#/TIOCD0/RXD6/SMISO6/SSCL6/RXD0/SMISO0/SSCL0/IRQ3-DS | P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/POE4#/POE11#/RXD6/RXD0/SMISO6/SMISO0/SSCL6/SSCL0/CRX0/PCKO/IRQ3-DS |
| 27 | P32/MTIOC0C/TMO3/TIOCC0/TXD6/SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/IRQ2-DS/RTCOUT/RTCIC2 | P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCOUT/RTCIC2/POE0#/POE10#/TXD6/TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS |

| 144pin LFQFP | RX210 | RX651 |
|---|---|---|
| 28 | P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/IRQ1-DS/RTCIC1 | TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS |
| 29 | P30/MTIOC4B/TMRI3/POE8#/RXD1/SMISO1/SSCL1/IRQ0-DS/RTCIC0 | TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS |
| 30 | P27/CS3#/MTIOC2B/TMCI3/SCK1 | TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB-A |
| 31 | P26/CS2#/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/SS3# | TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/MOSIB-A |
| 32 | P25/CS1#/MTIOC4C/MTCLKB/TIOCA4/RXD3/SMISO3/SSCL3/ADTRG0# | P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/HSYNC/ADTRG0# |
| 33 | P24/CS0#/MTIOC4A/MTCLKA/TMRI1/TIOCB4/SCK3 | P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/PIXCLK |
| 34 | P23/MTIOC3D/MTCLKD/TIOCD3/CTS0#/RTS0#/SS0#/TXD3/SMOSI3/SSDA3 | P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/SSDA3/PIXD7 |
| 35 | P22/MTIOC3B/MTCLKC/TMO0/TIOCC3/SCK0 | P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0/USB0_OVRCURB/PIXD6 |
| 36 | P21/MTIOC1B/TMCI0/TIOCA3/RXD0/SMISO0/SSCL0 | P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/USB0_EXICEN/PIXD5/IRQ9 |
| 37 | P20/MTIOC1A/TMRI0/TIOCB3/TXD0/SMOSI0/SSDA0 | P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/USB0_ID/PIXD4/IRQ8 |
| 38 | P17/MTIOC3A/MTIOC3B/TMO1/POE8#/TIOCB0/TCLKD/SCK1/MISOA/SDA-DS/TXD3/SMOSI3/SSDA3/IRQ7 | P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/PIXD3/IRQ7/ADTRG1# |
| 39 | P87/TIOCA2 | P87/MTIOC4C/TIOCA2/TXD10/SMOSI10/SSDA10/PIXD2 |
| 40 | P16/MTIOC3C/MTIOC3D/TMO2/TIOCB1/TCLKC/TXD1/SMOSI1/SSDA1/MOSIA/SCL-DS/RXD3/SMISO3/SSCL3/IRQ6/RTCOUT/ADTRG0# | P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/SMISO3/SSDA1/SSCL3/SCL2-DS/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB/IRQ6/ADTRG0# |
| 41 | P86/TIOCA0 | P86/MTIOC4D/TIOCA0/RXD10/SMISO10/SSCL10/PIXD1 |
| 42 | P15/MTIOC0B/MTCLKB/TMCI2/TIOCB2/TCLKB/RXD1/SMISO1/SSCL1/SCK3/IRQ5 | P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/CRX1-DS/PIXD0/IRQ5 |
| 43 | P14/MTIOC3A/MTCLKA/TMRI2/TIOCB5/TCLKA/CTS1#/RTS1#/SS1#/IRQ4 | P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_OVRCURA/IRQ4 |
| 44 | P13/MTIOC0B/TMO3/TIOCA5/SDA/TXD2/SMOSI2/SSDA2/IRQ3 | P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG1# |
| 45 | P12/TMCI1/SCL/RXD2/SMISO2/SSCL2/IRQ2 | P12/TMCI1/RXD2/SMISO2/SSCL2/SCL0[FM+]/IRQ2 |
| 46 | PH3/TMCI0 | VCC_USB |
| 47 | PH2/TMRI0/IRQ1 | USB0_DM |
| 48 | PH1/TMO0/IRQ0 | USB0_DP |
| 49 | PH0/CACREF | VSS_USB |

| 144pin LFQFP | RX210 | RX651 |
|---|---|---|
| 50 | P56/MTIOC3C/TIOCA1 | P56/EDACK1/MTIOC3C/TIOCA1 |
| 51 | P55/WAIT#/MTIOC4D/TMO3 | TRDATA3/P55/WAIT#/EDREQ0/MTIOC4D/TMO3/CRX1/IRQ10 |
| 52 | P54/ALE/MTIOC4B/TMCI1/CTS2#/RTS2#/SS2# | TRDATA2/P54/ALE/EDACK0/MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/CTX1 |
| 53 | BCLK/P53 | BCLK/P53 |
| 54 | P52/RD#/RXD2/SMISO2/SSCL2 | P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A |
| 55 | P51/WR1#/BC1#/WAIT#/SCK2 | P51/WR1#/BC1#/WAIT#/SSLB2-A/SCK2 |
| 56 | P50/WR0#/WR#/TXD2/SMOSI2/SSDA2 | P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1-A |
| 57 | VSS | VSS |
| 58 | P83/MTIOC4C/CTS10#/RTS10# | TRCLK/P83/EDACK1/MTIOC4C/CTS10#/SS10#/SCK10 |
| 59 | VCC | VCC |
| 60 | PC7/A23/CS0#/MTIOC3A/TMO2/MTCLKB/TXD8/SMOSI8/SSDA8/MISOA/CACREF | UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/TMO2/TOC0/PO31/CACREF/TXD8/SMOSI8/SSDA8/MISOA-A/TXD10/SMOSI10/SSDA10/MMC_D7-A/IRQ14 |
| 61 | PC6/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/RXD8/SMISO8/SSCL8/MOSIA | PC6/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/TIC0/PO30/RXD8/SMISO8/SSCL8/MOSIA-A/RXD10/SMISO10/SSCL10/MMC_D6-A/IRQ13 |
| 62 | PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TMRI2/SCK8/RSPCKA | PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TMRI2/PO29/SCK8/RSPCKA-A/SCK10/MMC_D5-A |
| 63 | P82/MTIOC4A/TXD10/SMOSI10/SSDA10 | TRSYNC/P82/EDREQ1/MTIOC4A/PO28/TXD10/SMOSI10/SSDA10/MMC_D4-A |
| 64 | P81/MTIOC3D/RXD10/SMISO10/SSCL10 | TRDATA1/P81/EDACK0/MTIOC3D/PO27/RXD10/SMISO10/SSCL10/MMC_D3-A/SDHI_CD-A/QIO3-A |
| 65 | P80/MTIOC3B/SCK10 | TRDATA0/P80/EDREQ0/MTIOC3B/PO26/SCK10/RTS10#/MMC_D2-A/SDHI_WP-A/QIO2-A |
| 66 | PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0 | PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0-A/CTS10#/RTS10#/SS10#/MMC_D1-A/SDHI_D1-A/SDSI_D1-A/QIO1-A/QMI-A |
| 67 | PC3/A19/MTIOC4D/TCLKB/TXD5/SMOSI5/SSDA5 | PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/SMOSI5/SSDA5/MMC_D0-A/SDHI_D0-A/SDSI_D0-A/QIO0-A/QMO-A |
| 68 | P77/TXD11/SMOSI11/SSDA11 | TRDATA7/P77/CS7#/PO23/TXD11/SMOSI11/SSDA11/MMC_CLK-A/SDHI_CLK-A/SDSI_CLK-A/QSPCLK-A |
| 69 | P76/RXD11/SMISO11/SSCL11 | TRDATA6/P76/CS6#/PO22/RXD11/SMISO11/SSCL11/MMC_CMD-A/SDHI_CMD-A/SDSI_CMD-A/QSSL-A |
| 70 | PC2/A18/MTIOC4B/TCLKA/RXD5/SMISO5/SSCL5/SSLA3 | PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/SMISO5/SSCL5/SSLA3-A/MMC_CD-A/SDHI_D3-A/SDSI_D3-A |
| 71 | P75/SCK11 | TRSYNC1/P75/CS5#/PO20/SCK11/RTS11#/MMC_RES#-A/SDHI_D2-A/SDSI_D2-A |
| 72 | P74/CTS11#/RTS11#/SS11# | TRDATA5/P74/A20/CS4#/PO19/CTS11#/SS11# |

| 144pin LFQFP | RX210 | RX651 |
|---|---|---|
| 73 | PC1/A17/MTIOC3A/TCLKD/SCK5/SSLA2 | PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/SSLA2-A/IRQ12 |
| 74 | PL1 | VCC |
| 75 | PC0/A16/MTIOC3C/TCLKC/CTS5#/RTS5#/SS5#/SSLA1 | PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/SS5#/SSLA1-A/IRQ14 |
| 76 | PL0 | VSS |
| 77 | P73 | TRDATA4/P73/CS3#/PO16 |
| 78 | PB7/A15/MTIOC3B/TIOCB5/TXD9/SMOSI9/SSDA9 | PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/SMOSI9/SSDA9/TXD11/SMOSI11/SSDA11/SDSI_D1-B |
| 79 | PB6/A14/MTIOC3D/TIOCA5/RXD9/SMISO9/SSCL9 | PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/SMISO9/SSCL9/RXD11/SMISO11/SSCL11/SDSI_D0-B |
| 80 | PB5/A13/MTIOC2A/MTIOC1B/TMRI1/POE1#/TIOCB4/SCK9 | PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/PO29/POE4#/SCK9/SCK11/SDSI_CLK-B |
| 81 | PB4/A12/TIOCA4/CTS9#/RTS9#/SS9# | PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/SS9#/CTS11#/RTS11#/SS11#/SDSI_CMD-B |
| 82 | PB3/A11/MTIOC0A/MTIOC4A/TMO0/POE3#/TIOCD3/TCLKD/SCK4/SCK6 | PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/SDSI_D3-B |
| 83 | PB2/A10/TIOCC3/TCLKC/CTS4#/RTS4#/SS4#/CTS6#/RTS6#/SS6# | PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/RTS4#/CTS6#/RTS6#/SS4#/SS6#/SDSI_D2-B |
| 84 | PB1/A9/MTIOC0C/MTIOC4C/TMCI0/TIOCB3/TXD4/SMOSI4/SSDA4/TXD6/SMOSI6/SSDA6/IRQ4-DS | PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/TXD4/TXD6/SMOSI4/SMOSI6/SSDA4/SSDA6/IRQ4-DS |
| 85 | P72 | P72/A19/CS2# |
| 86 | P71 | P71/A18/CS1# |
| 87 | PB0/A8/MTIC5W/TIOCA3/RXD4/SMISO4/SSCL4/RXD6/SMISO6/SSCL6/RSPCKA | PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/RXD6/SMISO4/SMISO6/SSCL4/SSCL6/IRQ12 |
| 88 | PA7/A7/TIOCB2/MISOA | PA7/A7/TIOCB2/PO23/MISOA-B |
| 89 | PA6/A6/MTIC5V/MTCLKB/TMCI3/POE2#/TIOCA2/CTS5#/RTS5#/SS5#/MOSIA | PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/POE10#/CTS5#/RTS5#/SS5#/MOSIA-B |
| 90 | PA5/A5/TIOCB1/RSPCKA | PA5/A5/MTIOC6B/TIOCB1/PO21/RSPCKA-B |
| 91 | VCC | VCC |
| 92 | PA4/A4/MTIC5U/MTCLKA/TMRI0/TIOCA1/TXD5/SMOSI5/SSDA5/SSLA0/IRQ5-DS/CVREFB1 | PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/IRQ5-DS |
| 93 | VSS | VSS |
| 94 | PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/RXD5/SMISO5/SSCL5/IRQ6-DS/CMPB1 | PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19/RXD5/SMISO5/SSCL5/IRQ6-DS |
| 95 | PA2/A2/RXD5/SMISO5/SSCL5/SSLA3 | PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/SSCL5/SSLA3-B |
| 96 | PA1/A1/MTIOC0B/MTCLKC/TIOCB0/SCK5/SSLA2/CVREFA | PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/PO17/SCK5/SSLA2-B/IRQ11 |
| 97 | PA0/A0/BC0#/MTIOC4A/TIOCA0/SSLA1/CACREF | PA0/A0/BC0#/MTIOC4A/MTIOC6D/TIOCA0/CACREF/PO16/SSLA1-B |
| 98 | P67 | P67/CS7#/DQM1/MTIOC7C/IRQ15 |
| 99 | P66 | P66/CS6#/DQM0/MTIOC7D |
| 100 | P65 | P65/CS5#/CKE |
| 101 | PE7/D15[A15/D15]/IRQ7/AN015 | PE7/D15[A15/D15]/MTIOC6A/TOC1/MISOB-B/MMC_RES#-B/SDHI_WP-B/IRQ7/AN105 |

| 144pin LFQFP | RX210 | RX651 |
|---|---|---|
| 102 | PE6/D14[A14/D14]/CTS4#/RTS4#/SS4#/IRQ6/AN014 | PE6/D14[A14/D14]/MTIOC6C/TIC1/MOSIB-B/MMC_CD-B/SDHI_CD-B/IRQ6/AN104 |
| 103 | PK5/TXD4/SMOSI4/SSDA4 | VCC |
| 104 | P70/SCK4 | SDCLK/P70 |
| 105 | PK4/RXD4/SMISO4/SSCL4 | VSS |
| 106 | PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/IRQ5/AN013 | PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/RSPCKB-B/IRQ5/AN103 |
| 107 | PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/AN012/CMPA2 | PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/PO28/SSLB0-B/AN102 |
| 108 | PE3/D11[A11/D11]/MTIOC4B/POE8#/CTS12#/RTS12#/SS12#/AN011/CMPA1 | PE3/D11[A11/D11]/MTIOC4B/PO26/POE8#/TOC3/CTS12#/RTS12#/SS12#/MMC_D7-B/AN101 |
| 109 | PE2/D10[A10/D10]/MTIOC4A/RXD12/RXDX12/SMISO12/SSCL12/IRQ7-DS/AN010/CVREFB0 | PE2/D10[A10/D10]/MTIOC4A/PO23/TIC3/RXD12/SMISO12/SSCL12/RXDX12/SSLB3-B/MMC_D6-B/IRQ7-DS/AN100 |
| 110 | PE1/D9[A9/D9]/MTIOC4C/TXD12/TXDX12/SIOX12/SMOSI12/SSDA12/AN009/CMPB0 | PE1/D9[A9/D9]/MTIOC4C/MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2-B/MMC_D5-B/ANEX1 |
| 111 | PE0/D8[A8/D8]/SCK12/AN008 | PE0/D8[A8/D8]/MTIOC3D/SCK12/SSLB1-B/MMC_D4-B/ANEX0 |
| 112 | P64 | P64/CS4#/WE# |
| 113 | P63 | P63/CS3#/CAS# |
| 114 | P62 | P62/CS2#/RAS# |
| 115 | P61/CTS9#/RTS9#/SS9# | P61/CS1#/SDCS# |
| 116 | PK3/RXD9/SMISO9/SSCL9 | VSS |
| 117 | P60/SCK9 | P60/CS0# |
| 118 | PK2/TXD9/SMOSI9/SSDA9 | VCC |
| 119 | PD7/D7[A7/D7]/MTIC5U/POE0#/IRQ7 | PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3/MMC_D1-B/SDHI_D1-B/QIO1-B/QMI-B/IRQ7/AN107 |
| 120 | PD6/D6[A6/D6]/MTIC5V/POE1#/IRQ6 | PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/SSLC2/MMC_D0-B/SDHI_D0-B/QIO0-B/QMO-B/IRQ6/AN106 |
| 121 | PD5/D5[A5/D5]/MTIC5W/POE2#/IRQ5 | PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/SSLC1/MMC_CLK-B/SDHI_CLK-B/QSPCLK-B/IRQ5/AN113 |
| 122 | PD4/D4[A4/D4]/POE3#/IRQ4 | PD4/D4[A4/D4]/MTIOC8B/POE11#/SSLC0/MMC_CMD-B/SDHI_CMD-B/QSSL-B/IRQ4/AN112 |
| 123 | PD3/D3[A3/D3]/POE8#/IRQ3 | PD3/D3[A3/D3]/MTIOC8D/POE8#/TOC2/RSPCKC/MMC_D3-B/SDHI_D3-B/QIO3-B/IRQ3/AN111 |
| 124 | PD2/D2[A2/D2]/MTIOC4D/IRQ2 | PD2/D2[A2/D2]/MTIOC4D/TIC2/CRX0/MISOC/MMC_D2-B/SDHI_D2-B/QIO2-B/IRQ2/AN110 |
| 125 | PD1/D1[A1/D1]/MTIOC4B/IRQ1 | PD1/D1[A1/D1]/MTIOC4B/POE0#/CTX0/MOSIC/IRQ1/AN109 |
| 126 | PD0/D0[A0/D0]/IRQ0 | PD0/D0[A0/D0]/POE4#/IRQ0/AN108 |
| 127 | P93/CTS7#/RTS7#/SS7# | P93/A19/POE0#/CTS7#/RTS7#/SS7#/AN117 |
| 128 | P92/RXD7/SMISO7/SSCL7 | P92/A18/POE4#/RXD7/SMISO7/SSCL7/AN116 |
| 129 | P91/SCK7 | P91/A17/SCK7/AN115 |

| 144pin LFQFP | RX210 | RX651 |
|---|---|---|
| 130 | VSS | VSS |
| 131 | P90/TXD7/SMOSI7/SSDA7 | P90/A16/TXD7/SMOSI7/SSDA7/AN114 |
| 132 | VCC | VCC |
| 133 | P47/AN007 | P47/IRQ15-DS/AN007 |
| 134 | P46/AN006 | P46/IRQ14-DS/AN006 |
| 135 | P45/AN005 | P45/IRQ13-DS/AN005 |
| 136 | P44/AN004 | P44/IRQ12-DS/AN004 |
| 137 | P43/AN003 | P43/IRQ11-DS/AN003 |
| 138 | P42/AN002 | P42/IRQ10-DS/AN002 |
| 139 | P41/AN001 | P41/IRQ9-DS/AN001 |
| 140 | VREFL0 | VREFL0 |
| 141 | P40/AN000 | P40/IRQ8-DS/AN000 |
| 142 | VREFH0 | VREFH0 |
| 143 | AVCC0 | AVCC0 |
| 144 | P07/ADTRG0# | P07/IRQ15/ADTRG0# |

## 3.2 145pin Package

Table 3.2 shows a Comparative Listing of Pin Functions (145pin Package).

**Table 3.2 Comparative Listing of Pin Functions (145pin Package)**

| 145pin TFLGA | RX210 | RX651 |
|---|---|---|
| A1 | AVSS0 | AVSS0 |
| A2 | P07/ADTRG0# | P07/IRQ15/ADTRG0# |
| A3 | P40/AN000 | P40/IRQ8-DS/AN000 |
| A4 | P42/AN002 | P42/IRQ10-DS/AN002 |
| A5 | P45/AN005 | P45/IRQ13-DS/AN005 |
| A6 | P90/TXD7/SMOSI7/SSDA7 | P90/A16/TXD7/SMOSI7/SSDA7/AN114 |
| A7 | P92/RXD7/SMISO7/SSCL7 | P92/A18/POE4#/RXD7/SMISO7/SSCL7/AN116 |
| A8 | PD2/D2[A2/D2]/MTIOC4D/IRQ2 | PD2/D2[A2/D2]/MTIOC4D/TIC2/CRX0/MISOC/MMC_D2-B/SDHI_D2-B/QIO2-B/IRQ2/AN110 |
| A9 | PD6/D6[A6/D6]/MTIC5V/POE1#/IRQ6 | PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/SSLC2/MMC_D0-B/SDHI_D0-B/QIO0-B/QMO-B/IRQ6/AN106 |
| A10 | PK3/RXD9/SMISO9/SSCL9 | VSS |
| A11 | P62 | P62/CS2#/RAS# |
| A12 | PE1/D9[A9/D9]/MTIOC4C/TXD12/TXDX12/SIOX12/SMOSI12/SSDA12/AN009/CMPB0 | PE1/D9[A9/D9]/MTIOC4C/MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2-B/MMC_D5-B/ANEX1 |
| A13 | PE3/D11[A11/D11]/MTIOC4B/POE8#/CTS12#/RTS12#/SS12#/AN011/CMPA1 | PE3/D11[A11/D11]/MTIOC4B/PO26/POE8#/TOC3/CTS12#/RTS12#/SS12#/MMC_D7-B/AN101 |
| B1 | VREFH | AVCC1 |
| B2 | AVCC0 | AVCC0 |
| B3 | P05/DA1 | P05/IRQ13/DA1 |
| B4 | VREFL0 | VREFL0 |
| B5 | P43/AN003 | P43/IRQ11-DS/AN003 |
| B6 | P47/AN007 | P47/IRQ15-DS/AN007 |
| B7 | P91/SCK7 | P91/A17/SCK7/AN115 |
| B8 | PD0/D0[A0/D0]/IRQ0 | PD0/D0[A0/D0]/POE4#/IRQ0/AN108 |
| B9 | PD4/D4[A4/D4]/POE3#/IRQ4 | PD4/D4[A4/D4]/MTIOC8B/POE11#/SSLC0/MMC_CMD-B/SDHI_CMD-B/QSSL-B/IRQ4/AN112 |
| B10 | PK2/TXD9/SMOSI9/SSDA9 | VCC |
| B11 | P61/CTS9#/RTS9#/SS9# | P61/CS1#/SDCS# |
| B12 | PE2/D10[A10/D10]/MTIOC4A/RXD12/RXDX12/SMISO12/SSCL12/IRQ7-DS/AN010/CVREFB0 | PE2/D10[A10/D10]/MTIOC4A/PO23/TIC3/RXD12/SMISO12/SSCL12/RXDX12/SSLB3-B/MMC_D6-B/IRQ7-DS/AN100 |
| B13 | PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/AN012/CMPA2 | PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/PO28/SSLB0-B/AN102 |
| C1 | VREFL | AVSS1 |
| C2 | P02/TMCI1/SCK6 | P02/TMCI1/SCK6/IRQ10/AN120 |
| C3 | VREFH0 | VREFH0 |
| C4 | P41/AN001 | P41/IRQ9-DS/AN001 |
| C5 | P46/AN006 | P46/IRQ14-DS/AN006 |
| C6 | VSS | VSS |

| 145pin TFLGA | RX210 | RX651 |
|---|---|---|
| C7 | PD1/D1[A1/D1]/MTIOC4B/IRQ1 | PD1/D1[A1/D1]/MTIOC4B/POE0#/CTX0/MOSIC/IRQ1/AN109 |
| C8 | PD3/D3[A3/D3]/POE8#/IRQ3 | PD3/D3[A3/D3]/MTIOC8D/POE8#/TOC2/RSPCKC/MMC_D3-B/SDHI_D3-B/QIO3-B/IRQ3/AN111 |
| C9 | PD7/D7[A7/D7]/MTIC5U/POE0#/IRQ7 | PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3/MMC_D1-B/SDHI_D1-B/QIO1-B/QMI-B/IRQ7/AN107 |
| C10 | P63 | P63/CS3#/CAS# |
| C11 | PE0/D8[A8/D8]/SCK12/AN008 | PE0/D8[A8/D8]/MTIOC3D/SCK12/SSLB1-B/MMC_D4-B/ANEX0 |
| C12 | P70/SCK4 | P70/SDCLK |
| C13 | PK4/RXD4/SMISO4/SSCL4 | VSS |
| D1 | P00/TMRI0/TXD6/SMOSI6/SSDA6 | P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/AN118 |
| D2 | PF5/IRQ4 | PF5/IRQ4 |
| D3 | P03/DA0 | P03/IRQ11/DA0 |
| D4 | P01/TMCI0/RXD6/SMISO6/SSCL6 | P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/AN119 |
| D5 | VCC | VCC |
| D6 | P93/CTS7#/RTS7#/SS7# | P93/A19/POE0#/CTS7#/RTS7#/SS7#/AN117 |
| D7 | PD5/D5[A5/D5]/MTIC5W/POE2#/IRQ5 | PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/SSLC1/MMC_CLK-B/SDHI_CLK-B/QSPCLK-B/IRQ5/AN113 |
| D8 | P60/SCK9 | P60/CS0# |
| D9 | P64 | P64/CS4#/WE# |
| D10 | PE7/D15[A15/D15]/IRQ7/AN015 | PE7/D15[A15/D15]/MTIOC6A/TOC1/MISOB-B/MMC_RES#-B/SDHI_WP-B/IRQ7/AN105 |
| D11 | PK5/TXD4/SMOSI4/SSDA4 | VCC |
| D12 | PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/IRQ5/AN013 | PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/RSPCKB-B/IRQ5/AN103 |
| D13 | PE6/D14[A14/D14]/CTS4#/RTS4#/SS4#/IRQ6/AN014 | PE6/D14[A14/D14]/MTIOC6C/TIC1/MOSIB-B/MMC_CD-B/SDHI_CD-B/IRQ6/AN104 |
| E1 | VSS | VSS |
| E2 | VCL | VCL |
| E3 | PJ5 | PJ5/POE8#/CTS2#/RTS2#/SS2# |
| E4 | NC | EMLE |
| E5 | P44/AN004 | P44/IRQ12-DS/AN004 |
| E10 | PA0/A0/BC0#/MTIOC4A/TIOCA0/SSLA1/CACREF | PA0/A0/BC0#/MTIOC4A/MTIOC6D/TIOCA0/CACREF/PO16/SSLA1-B |
| E11 | P66 | P66/CS6#/DQM0/MTIOC7D |
| E12 | P65 | P65/CS5#/CKE |
| E13 | P67 | P67/CS7#/DQM1/MTIOC7C/IRQ15 |
| F1 | XCIN | XCIN |
| F2 | XCOUT | XCOUT |
| F3 | PJ3/MTIOC3C/CTS6#/RTS6#/SS6#/CTS0#/RTS0#/SS0# | PJ3/EDACK1/MTIOC3C/CTS6#/RTS6#/CTS0#/RTS0#/SS6#/SS0# |
| F4 | PJ1/MTIOC3A | VBATT |
| F10 | PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/RXD5/SMISO5/SSCL5/IRQ6-DS/CMPB1 | PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19/RXD5/SMISO5/SSCL5/IRQ6-DS |
| F11 | VSS | VSS |

| 145pin TFLGA | RX210 | RX651 |
|---|---|---|
| F12 | PA1/A1/MTIOC0B/MTCLKC/TIOCB0/SCK5/SSLA2/CVREFA | PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/PO17/SCK5/SSLA2-B/IRQ11 |
| F13 | PA2/A2/RXD5/SMISO5/SSCL5/SSLA3 | PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/SSCL5/SSLA3-B |
| G1 | XTAL/P37 | XTAL/P37 |
| G2 | RES# | RES# |
| G3 | MD/FINED | MD/FINED |
| G4 | NC | BSCANP |
| G10 | PA5/A5/TIOCB1/RSPCKA | PA5/A5/MTIOC6B/TIOCB1/PO21/RSPCKA-B |
| G11 | PA6/A6/MTIC5V/MTCLKB/TMCI3/POE2#/TIOCA2/CTS5#/RTS5#/SS5#/MOSIA | PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/POE10#/CTS5#/RTS5#/SS5#/MOSIA-B |
| G12 | VCC | VCC |
| G13 | PA4/A4/MTIC5U/MTCLKA/TMRI0/TIOCA1/TXD5/SMOSI5/SSDA5/SSLA0/IRQ5-DS/CVREFB1 | PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/IRQ5-DS |
| H1 | EXTAL/P36 | EXTAL/P36 |
| H2 | VCC | VCC |
| H3 | VSS | VSS |
| H4 | P35/NMI | UPSEL/P35/NMI |
| H10 | P72 | P72/A19/CS2# |
| H11 | P71 | P71/A18/CS1# |
| H12 | PB0/A8/MTIC5W/TIOCA3/RXD4/SMISO4/SSCL4/RXD6/SMISO6/SSCL6/RSPCKA | PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/RXD6/SMISO4/SMISO6/SSCL4/SSCL6/IRQ12 |
| H13 | PA7/A7/TIOCB2/MISOA | PA7/A7/TIOCB2/PO23/MISOA-B |
| J1 | P34/MTIOC0A/TMCI3/POE2#/SCK6/SCK0/IRQ4 | TRST#/P34/MTIOC0A/TMCI3/PO12/POE10#/SCK6/SCK0/IRQ4 |
| J2 | P33/MTIOC0D/TMRI3/POE3#/TIOCD0/RXD6/SMISO6/SSCL6/RXD0/SMISO0/SSCL0/IRQ3-DS | P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/POE4#/POE11#/RXD6/RXD0/SMISO6/SMISO0/SSCL6/SSCL0/CRX0/PCKO/IRQ3-DS |
| J3 | P32/MTIOC0C/TMO3/TIOCC0/TXD6/SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/IRQ2-DS/RTCOUT/RTCIC2 | P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCOUT/RTCIC2/POE0#/POE10#/TXD6/TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS |
| J4 | P30/MTIOC4B/TMRI3/POE8#/RXD1/SMISO1/SSCL1/IRQ0-DS/RTCIC0 | TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS |
| J10 | PB3/A11/MTIOC0A/MTIOC4A/TMO0/POE3#/TIOCD3/TCLKD/SCK4/SCK6 | PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/SDSI_D3-B |
| J11 | PB4/A12/TIOCA4/CTS9#/RTS9#/SS9# | PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/SS9#/CTS11#/RTS11#/SS11#/SDSI_CMD-B |
| J12 | PB2/A10/TIOCC3/TCLKC/CTS4#/RTS4#/SS4#/CTS6#/RTS6#/SS6# | PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/RTS4#/CTS6#/RTS6#/SS4#/SS6#/SDSI_D2-B |
| J13 | PB1/A9/MTIOC0C/MTIOC4C/TMCI0/TIOCB3/TXD4/SMOSI4/SSDA4/TXD6/SMOSI6/SSDA6/IRQ4-DS | PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/TXD4/TXD6/SMOSI4/SMOSI6/SSDA4/SSDA6/IRQ4-DS |
| K1 | P27/CS3#/MTIOC2B/TMCI3/SCK1 | TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB-A |
| K2 | P26/CS2#/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/SS3# | TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/MOSIB-A |

| 145pin TFLGA | RX210 | RX651 |
|---|---|---|
| K3 | P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/IRQ1-DS/RTCIC1 | TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS |
| K4 | P15/MTIOC0B/MTCLKB/TMCI2/TIOCB2/TCLKB/RXD1/SMISO1/SSCL1/SCK3/IRQ5 | P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/CRX1-DS/PIXD0/IRQ5 |
| K5 | P54/ALE/MTIOC4B/TMCI1/CTS2#/RTS2#/SS2# | TRDATA2/P54/ALE/EDACK0/MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/CTX1 |
| K6 | BCLK/P53 | P53/BCLK |
| K7 | P51/WR1#/BC1#/WAIT#/SCK2 | P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A |
| K8 | VCC | VCC |
| K9 | P80/MTIOC3B/SCK10 | TRDATA0/P80/EDREQ0/MTIOC3B/PO26/SCK10/RTS10#/MMC_D2-A/SDHI_WP-A/QIO2-A |
| K10 | P76/RXD11/SMISO11/SSCL11 | TRDATA6/P76/CS6#/PO22/RXD11/SMISO11/SSCL11/MMC_CMD-A/SDHI_CMD-A/SDSI_CMD-A/QSSL-A |
| K11 | PB7/A15/MTIOC3B/TIOCB5/TXD9/SMOSI9/SSDA9 | PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/SMOSI9/SSDA9/TXD11/SMOSI11/SSDA11/SDSI_D1-B |
| K12 | PB6/A14/MTIOC3D/TIOCA5/RXD9/SMISO9/SSCL9 | PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/SMISO9/SSCL9/RXD11/SMISO11/SSCL11/SDSI_D0-B |
| K13 | PB5/A13/MTIOC2A/MTIOC1B/TMRI1/POE1#/TIOCB4/SCK9 | PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/PO29/POE4#/SCK9/SCK11/SDSI_CLK-B |
| L1 | P25/CS1#/MTIOC4C/MTCLKB/TIOCA4/RXD3/SMISO3/SSCL3/ADTRG0# | P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/HSYNC/ADTRG0# |
| L2 | P23/MTIOC3D/MTCLKD/TIOCD3/CTS0#/RTS0#/SS0#/TXD3/SMOSI3/SSDA3 | P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/SSDA3/PIXD7 |
| L3 | P16/MTIOC3C/MTIOC3D/TMO2/TIOCB1/TCLKC/TXD1/SMOSI1/SSDA1/MOSIA/SCL-DS/RXD3/SMISO3/SSCL3/IRQ6/RTCOUT/ADTRG0# | P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/SMISO3/SSDA1/SSCL3/SCL2-DS/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB/IRQ6/ADTRG0# |
| L4 | P24/CS0#/MTIOC4A/MTCLKA/TMRI1/TIOCB4/SCK3 | P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/PIXCLK |
| L5 | P13/MTIOC0B/TMO3/TIOCA5/SDA/TXD2/SMOSI2/SSDA2/IRQ3 | P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG1# |
| L6 | P56/MTIOC3C/TIOCA1 | P56/EDACK1/MTIOC3C/TIOCA1 |
| L7 | P52/RD#/RXD2/SMISO2/SSCL2 | P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A |
| L8 | P83/MTIOC4C/CTS10#/RTS10# | TRCLK/P83/EDACK1/MTIOC4C/CTS10#/SS10#/SCK10 |
| L9 | PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TMRI2/SCK8/RSPCKA | PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TMRI2/PO29/SCK8/RSPCKA-A/SCK10/MMC_D5-A |
| L10 | PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0 | PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0-A/CTS10#/RTS10#/SS10#/MMC_D1-A/SDHI_D1-A/SDSI_D1-A/QIO1-A/QMI-A |

| 145pin TFLGA | RX210 | RX651 |
|---|---|---|
| L11 | PC2/A18/MTIOC4B/TCLKA/RXD5/SMISO5/SSCL5/SSLA3 | PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/SMISO5/SSCL5/SSLA3-A/MMC_CD-A/SDHI_D3-A/SDSI_D3-A |
| L12 | P73 | TRDATA4/P73/CS3#/PO16 |
| L13 | PL0 | VSS |
| M1 | P22/MTIOC3B/MTCLKC/TMO0/TIOCC3/SCK0 | P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0/USB0_OVRCURB/PIXD6 |
| M2 | P17/MTIOC3A/MTIOC3B/TMO1/POE8#/TIOCB0/TCLKD/SCK1/MISOA/SDA-DS/TXD3/SMOSI3/SSDA3/IRQ7 | P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/PIXD3/IRQ7/ADTRG1# |
| M3 | P86/TIOCA0 | P86/MTIOC4D/TIOCA0/RXD10/SMISO10/SSCL10/PIXD1 |
| M4 | P12/TMCI1/SCL/RXD2/SMISO2/SSCL2/IRQ2 | P12/TMCI1/RXD2/SMISO2/SSCL2/SCL0[FM+]/IRQ2 |
| M5 | PH3/TMCI0 | VCC_USB |
| M6 | PH0/CACREF | VSS_USB |
| M7 | P50/WR0#/WR#/TXD2/SMOSI2/SSDA2 | P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1-A |
| M8 | PC6/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/RXD8/SMISO8/SSCL8/MOSIA | PC6/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/TIC0/PO30/RXD8/SMISO8/SSCL8/MOSIA-A/RXD10/SMISO10/SSCL10/MMC_D6-A/IRQ13 |
| M9 | P81/MTIOC3D/RXD10/SMISO10/SSCL10 | TRDATA1/P81/EDACK0/MTIOC3D/PO27/RXD10/SMISO10/SSCL10/MMC_D3-A/SDHI_CD-A/QIO3-A |
| M10 | P77/TXD11/SMOSI11/SSDA11 | TRDATA7/P77/CS7#/PO23/TXD11/SMOSI11/SSDA11/MMC_CLK-A/SDHI_CLK-A/SDSI_CLK-A/QSPCLK-A |
| M11 | PC0/A16/MTIOC3C/TCLKC/CTS5#/RTS5#/SS5#/SSLA1 | PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/SS5#/SSLA1-A/IRQ14 |
| M12 | PC1/A17/MTIOC3A/TCLKD/SCK5/SSLA2 | PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/SSLA2-A/IRQ12 |
| M13 | PL1 | VCC |
| N1 | P21/MTIOC1B/TMCI0/TIOCA3/RXD0/SMISO0/SSCL0 | P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/USB0_EXICEN/PIXD5/IRQ9 |
| N2 | P20/MTIOC1A/TMRI0/TIOCB3/TXD0/SMOSI0/SSDA0 | P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/USB0_ID/PIXD4/IRQ8 |
| N3 | P87/TIOCA2 | P87/MTIOC4C/TIOCA2/TXD10/SMOSI10/SSDA10/PIXD2 |
| N4 | P14/MTIOC3A/MTCLKA/TMRI2/TIOCB5/TCLKA/CTS1#/RTS1#/SS1#/IRQ4 | P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_OVRCURA/IRQ4 |
| N5 | PH2/TMRI0/IRQ1 | USB0_DM |
| N6 | PH1/TMO0/IRQ0 | USB0_DP |
| N7 | P55/WAIT#/MTIOC4D/TMO3 | TRDATA3/P55/WAIT#/EDREQ0/MTIOC4D/TMO3/CRX1/IRQ10 |
| N8 | VSS | VSS |
| N9 | PC7/A23/CS0#/MTIOC3A/TMO2/MTCLKB/TXD8/SMOSI8/SSDA8/MISOA/CACREF | UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/TMO2/TOC0/PO31/CACREF/TXD8/SMOSI8/SSDA8/MISOA-A/TXD10/SMOSI10/SSDA10/MMC_D7-A/IRQ14 |

| 145pin TFLGA | RX210 | RX651 |
|---|---|---|
| N10 | P82/MTIOC4A/TXD10/SMOSI10/SSDA10 | TRSYNC/P82/EDREQ1/MTIOC4A/PO28/TXD10/SMOSI10/SSDA10/MMC_D4-A |
| N11 | PC3/A19/MTIOC4D/TCLKB/TXD5/SMOSI5/SSDA5 | PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/SMOSI5/SSDA5/MMC_D0-A/SDHI_D0-A/SDSI_D0-A/QIO0-A/QMO-A |
| N12 | P75/SCK11 | TRSYNC1/P75/CS5#/PO20/SCK11/RTS11#/MMC_RES#-A/SDHI_D2-A/SDSI_D2-A |
| N13 | P74/CTS11#/RTS11#/SS11# | TRDATA5/P74/A20/CS4#/PO19/CTS11#/SS11# |

## 3.3 100pin Package (QFP)

Table 3.4 shows a Comparative Listing of Pin Functions (100pin Package (TFLGA)).

**Table 3.3 Comparative Listing of Pin Functions (100pin Package (QFP))**

| 100pin | RX210 (LFQFP) | RX651 (LQFP) |
|---|---|---|
| 1 | VREFH | AVCC1 |
| 2 | P03/DA0 | EMLE |
| 3 | VREFL | AVSS1 |
| 4 | PJ3/MTIOC3C/CTS6#/RTS6#/SS6# | PJ3/EDACK1/MTIOC3C//CTS6#/RTS6#/CTS0#/RTS0#/SS6#/SS0# |
| 5 | VCL | VCL |
| 6 | PJ1/MTIOC3A | VBATT |
| 7 | MD/FINED | MD/FINED |
| 8 | XCIN | XCIN |
| 9 | XCOUT | XCOUT |
| 10 | RES# | RES# |
| 11 | XTAL/P37 | P37/XTAL |
| 12 | VSS | VSS |
| 13 | EXTAL/P36 | P36/EXTAL |
| 14 | VCC | VCC |
| 15 | P35/NMI | P35/UPSEL/NMI |
| 16 | P34/MTIOC0A/TMCI3/POE2#/SCK6/IRQ4 | P34/TRST#/MTIOC0A/TMCI3/PO12/POE10#/SCK6/SCK0/IRQ4 |
| 17 | P33/MTIOC0D/TMRI3/POE3#/RXD6/SMISO6/SSCL6/IRQ3-DS | P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/POE4#/POE11#/RXD6/RXD0/SMISO6/SMISO0/SSCL6/SSCL0/CRX0/IRQ3-DS |
| 18 | P32/MTIOC0C/TMO3/TXD6/SMOSI6/SSDA6/IRQ2-DS/RTCOUT/RTCIC2 | P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCOUT/RTCIC2/POE0#/POE10#/TXD6/TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/CTX0/USB0_VBUSEN/IRQ2-DS |
| 19 | P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/IRQ1-DS/RTCIC1 | P31/TMS/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS |
| 20 | P30/MTIOC4B/TMRI3/POE8#/RXD1/SMISO1/SSCL1/IRQ0-DS/RTCIC0 | P30/TDI/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS |
| 21 | P27/CS3#/MTIOC2B/TMCI3/SCK1 | P27/TCK/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB-A |
| 22 | P26/CS2#/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1 | P26/TDO/CS6#/MTIOC2A/TMO1/PO6/TXD1/CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/MOSIB-A |
| 23 | P25/CS1#/MTIOC4C/MTCLKB/ADTRG0# | P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/ADTRG0# |
| 24 | P24/CS0#/MTIOC4A/MTCLKA/TMRI1 | P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN |
| 25 | P23/MTIOC3D/MTCLKD/CTS0#/RTS0#/SS0# | P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/SSDA3 |
| 26 | P22/MTIOC3B/MTCLKC/TMO0/SCK0 | P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0/USB0_OVRCURB |
| 27 | P21/MTIOC1B/TMCI0/RXD0/SMISO0/SSCL0 | P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/USB0_EXICEN/IRQ9 |

| 100pin | RX210 (LFQFP) | RX651 (LQFP) |
|---|---|---|
| 28 | P20/MTIOC1A/TMRI0/TXD0/SMOSI0/SSDA0 | P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/USB0_ID/IRQ8 |
| 29 | P17/MTIOC3A/MTIOC3B/TMO1/POE8#/SCK1/MISOA/SDA-DS/IRQ7 | P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/IRQ7/ADTRG1# |
| 30 | P16/MTIOC3C/MTIOC3D/TMO2/TXD1/SMOSI1/SSDA1/MOSIA/SCL-DS/IRQ6/RTCOUT/ADTRG0# | P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/SMISO3/SSDA1/SSCL3/SCL2-DS/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB/IRQ6/ADTRG0# |
| 31 | P15/MTIOC0B/MTCLKB/TMCI2/RXD1/SMISO1/SSCL1/IRQ5 | P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/CRX1-DS/IRQ5 |
| 32 | P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/RTS1#/SS1#/IRQ4 | P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_OVRCURA/IRQ4 |
| 33 | P13/MTIOC0B/TMO3/SDA/IRQ3 | P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG1# |
| 34 | P12/TMCI1/SCL/IRQ2 | P12/TMCI1/RXD2/SMISO2/SSCL2/SCL0[FM+]/IRQ2 |
| 35 | PH3/TMCI0 | VCC_USB |
| 36 | PH2/TMRI0/IRQ1 | USB0_DM |
| 37 | PH1/TMO0/IRQ0 | USB0_DP |
| 38 | PH0/CACREF | VSS_USB |
| 39 | P55/WAIT#/MTIOC4D/TMO3 | P55/WAIT#/EDREQ0/MTIOC4D/TMO3/CRX1/IRQ10 |
| 40 | P54/ALE/MTIOC4B/TMCI1 | P54/ALE/EDACK0/MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/CTX1 |
| 41 | BCLK/P53 | P53/BCLK |
| 42 | P52/RD# | P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A |
| 43 | P51/WR1#/BC1#/WAIT# | P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A |
| 44 | P50/WR0#/WR# | P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1-A |
| 45 | PC7/A23/CS0#/MTIOC3A/TMO2/MTCLKB/TXD8/SMOSI8/SSDA8/MISOA/CACREF | PC7/UB/A23/CS0#/MTIOC3A/MTCLKB/TMO2/TOC0/PO31/CACREF/TXD8/SMOSI8/SSDA8/MISOA-A/TXD10/SMOSI10/SSDA10/IRQ14 |
| 46 | PC6/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/RXD8/SMISO8/SSCL8/MOSIA | PC6/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/TIC0/PO30/RXD8/SMISO8/SSCL8/MOSIA-A/RXD10/SMISO10/SSCL10/IRQ13 |
| 47 | PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TMRI2/SCK8/RSPCKA | PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TMRI2/PO29/SCK8/RSPCKA-A/SCK10 |
| 48 | PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0 | PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0-A/CTS10#/RTS10#/SS10# |
| 49 | PC3/A19/MTIOC4D/TXD5/SMOSI5/SSDA5 | PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/SMOSI5/SSDA5 |
| 50 | PC2/A18/MTIOC4B/RXD5/SMISO5/SSCL5/SSLA3 | PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/SMISO5/SSCL5/SSLA3-A |
| 51 | PC1/A17/MTIOC3A/SCK5/SSLA2 | PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/SSLA2-A/IRQ12 |
| 52 | PC0/A16/MTIOC3C/CTS5#/RTS5#/SS5#/SSLA1 | PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/SS5#/SSLA1-A/IRQ14 |

| 100pin | RX210 (LFQFP) | RX651 (LQFP) |
|---|---|---|
| 53 | PB7/A15/MTIOC3B/TXD9/SMOSI9/SSDA9 | PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/SMOSI9/SSDA9/TXD11/SMOSI11/SSDA11/SDSI_D1-B |
| 54 | PB6/A14/MTIOC3D/RXD9/SMISO9/SSCL9 | PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/SMISO9/SSCL9/RXD11/SMISO11/SSCL11/SDSI_D0-B |
| 55 | PB5/A13/MTIOC2A/MTIOC1B/TMRI1/POE1#/SCK9 | PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/PO29/POE4#/SCK9/SCK11/SDSI_CLK-B |
| 56 | PB4/A12/CTS9#/RTS9#/SS9# | PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/SS9#/CTS11#/RTS11#/SS11#/SDSI_CMD-B |
| 57 | PB3/A11/MTIOC0A/MTIOC4A/TMO0/POE3#/SCK6 | PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE11#/SCK6/SDSI_D3-B |
| 58 | PB2/A10/CTS6#/RTS6#/SS6# | PB2/A10/TIOCC3/TCLKC/PO26/CTS6#/RTS6#/SS6#/SDSI_D2-B |
| 59 | PB1/A9/MTIOC0C/MTIOC4C/TMCI0/TXD6/SMOSI6/SSDA6/IRQ4-DS | PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/TXD6/SMOSI6/SSDA6/IRQ4-DS |
| 60 | VCC | VCC |
| 61 | PB0/A8/MTIC5W/RXD6/SMISO6/SSCL6/RSPCKA | PB0/A8/MTIC5W/TIOCA3/PO24/RXD6/SMISO6/SSCL6/IRQ12 |
| 62 | VSS | VSS |
| 63 | PA7/A7/MISOA | PA7/A7/TIOCB2/PO23/MISOA-B |
| 64 | PA6/A6/MTIC5V/MTCLKB/TMCI3/POE2#/CTS5#/RTS5#/SS5#/MOSIA | PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/POE10#/CTS5#/RTS5#/SS5#/MOSIA-B |
| 65 | PA5/A5/RSPCKA | PA5/A5/MTIOC6B/TIOCB1/PO21/RSPCKA-B |
| 66 | PA4/A4/MTIC5U/MTCLKA/TMRI0/TXD5/SMOSI5/SSDA5/SSLA0/IRQ5-DS/CVREFB1 | PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/IRQ5-DS |
| 67 | PA3/A3/MTIOC0D/MTCLKD/RXD5/SMISO5/SSCL5/IRQ6-DS/CMPB1 | PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19/RXD5/SMISO5/SSCL5/IRQ6-DS |
| 68 | PA2/A2/RXD5/SMISO5/SSCL5/SSLA3 | PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/SSCL5/SSLA3-B |
| 69 | PA1/A1/MTIOC0B/MTCLKC/SCK5/SSLA2/CVREFA | PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/PO17/SCK5/SSLA2-B/IRQ11 |
| 70 | PA0/A0/BC0#/MTIOC4A/SSLA1/CACREF | PA0/A0/BC0#/MTIOC4A/MTIOC6D/TIOCA0/CACREF/PO16/SSLA1-B |
| 71 | PE7/D15[A15/D15]/IRQ7/AN015 | PE7/D15[A15/D15]/MTIOC6A/TOC1/MISOB-B/MMC_RES#-B/SDHI_WP-B/IRQ7/AN105 |
| 72 | PE6/D14[A14/D14]/IRQ6/AN014 | PE6/D14[A14/D14]/MTIOC6C/TIC1/MOSIB-B/MMC_CD-B/SDHI_CD-B/IRQ6/AN104 |
| 73 | PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/IRQ5/AN013 | PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/RSPCKB-B/IRQ5/AN103 |
| 74 | PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/AN012/CMPA2 | PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/PO28/SSLB0-B/AN102 |
| 75 | PE3/D11[A11/D11]/MTIOC4B/POE8#/CTS12#/RTS12#/SS12#/AN011/CMPA1 | PE3/D11[A11/D11]/MTIOC4B/PO26/POE8#/TOC3/CTS12#/RTS12#/SS12#/MMC_D7-B/AN101 |
| 76 | PE2/D10[A10/D10]/MTIOC4A/RXD12/RXDX12/SMISO12/SSCL12/IRQ7-DS/AN010/CVREFB0 | PE2/D10[A10/D10]/MTIOC4A/PO23/TIC3/RXD12/SMISO12/SSCL12/RXDX12/SSLB3-B/MMC_D6-B/IRQ7-DS/AN100 |
| 77 | PE1/D9[A9/D9]/MTIOC4C/TXD12/TXDX12/SIOX12/SMOSI12/SSDA12/AN009/CMPB0 | PE1/D9[A9/D9]/MTIOC4C/MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2-B/MMC_D5-B/ANEX1 |
| 78 | PE0/D8[A8/D8]/SCK12/AN008 | PE0/D8[A8/D8]/MTIOC3D/SCK12/SSLB1-B/MMC_D4-B/ANEX0 |

| 100pin | RX210 (LFQFP) | RX651 (LQFP) |
|---|---|---|
| 79 | PD7/D7[A7/D7]/MTIC5U/POE0#/IRQ7 | PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3/MMC_D1-B/SDHI_D1-B/QIO1-B/QMI-B/IRQ7/AN107 |
| 80 | PD6/D6[A6/D6]/MTIC5V/POE1#/IRQ6 | PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/SSLC2/MMC_D0-B/SDHI_D0-B/QIO0-B/QMO-B/IRQ6/AN106 |
| 81 | PD5/D5[A5/D5]/MTIC5W/POE2#/IRQ5 | PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/SSLC1/MMC_CLK-B/SDHI_CLK-B/QSPCLK-B/IRQ5/AN113 |
| 82 | PD4/D4[A4/D4]/POE3#/IRQ4 | PD4/D4[A4/D4]/MTIOC8B/POE11#/SSLC0/MMC_CMD-B/SDHI_CMD-B/QSSL-B/IRQ4/AN112 |
| 83 | PD3/D3[A3/D3]/POE8#/IRQ3 | PD3/D3[A3/D3]/MTIOC8D/POE8#/TOC2/RSPCKC/MMC_D3-B/SDHI_D3-B/QIO3-B/IRQ3/AN111 |
| 84 | PD2/D2[A2/D2]/MTIOC4D/IRQ2 | PD2/D2[A2/D2]/MTIOC4D/TIC2/CRX0/MISOC/MMC_D2-B/SDHI_D2-B/QIO2-B/IRQ2/AN110 |
| 85 | PD1/D1[A1/D1]/MTIOC4B/IRQ1 | PD1/D1[A1/D1]/MTIOC4B/POE0#/CTX0/MOSIC/IRQ1/AN109 |
| 86 | PD0/D0[A0/D0]/IRQ0 | PD0/D0[A0/D0]/POE4#/IRQ0/AN108 |
| 87 | P47/AN007 | P47/IRQ15-DS/AN007 |
| 88 | P46/AN006 | P46/IRQ14-DS/AN006 |
| 89 | P45/AN005 | P45/IRQ13-DS/AN005 |
| 90 | P44/AN004 | P44/IRQ12-DS/AN004 |
| 91 | P43/AN003 | P43/IRQ11-DS/AN003 |
| 92 | P42/AN002 | P42/IRQ10-DS/AN002 |
| 93 | P41/AN001 | P41/IRQ9-DS/AN001 |
| 94 | VREFL0 | VREFL0 |
| 95 | P40/AN000 | P40/IRQ8-DS/AN000 |
| 96 | VREFH0 | VREFH0 |
| 97 | AVCC0 | AVCC0 |
| 98 | P07/ADTRG0# | P07/IRQ15/ADTRG0# |
| 99 | AVSS0 | AVSS0 |
| 100 | P05/DA1 | P05/IRQ13/DA1 |

## 3.4 100pin Package (TFLGA)

Table 3.4 shows a Comparative Listing of Pin Functions (100pin Package (TFLGA)).

**Table 3.4 Comparative Listing of Pin Functions (100pin Package (TFLGA))**

| 100pin TFLGA | RX210 | RX651 |
|---|---|---|
| A1 | P05/DA1 | P05/IRQ13/DA1 |
| A2 | VREFH | AVCC1 |
| A3 | P07/ADTRG0# | P07/IRQ15/ADTRG0# |
| A4 | VREFL0 | VREFL0 |
| A5 | P43/AN003 | P43/IRQ11-DS/AN003 |
| A6 | PD0/D0[A0/D0]/IRQ0 | PD0/D0[A0/D0]/POE4#/IRQ0/AN108 |
| A7 | PD4/D4[A4/D4]/POE3#/IRQ4 | PD4/D4[A4/D4]/MTIOC8B/POE11#/SSLC0/MMC_CMD-B/SDHI_CMD-B/QSSL-B/IRQ4/AN112 |
| A8 | PE0/D8[A8/D8]/SCK12/AN008 | PE0/D8[A8/D8]/MTIOC3D/SCK12/SSLB1-B/MMC_D4-B/ANEX0 |
| A9 | PE1/D9[A9/D9]/MTIOC4C/TXD12/TXDX12/SIOX12/SMOSI12/SSDA12/AN009/CMPB0 | PE1/D9[A9/D9]/MTIOC4C/MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2-B/MMC_D5-B/ANEX1 |
| A10 | PE2/D10[A10/D10]/MTIOC4A/RXD12/RXDX12/SMISO12/SSCL12/IRQ7-DS/AN010/CVREFB0 | PE2/D10[A10/D10]/MTIOC4A/PO23/TIC3/RXD12/SMISO12/SSCL12/RXDX12/SSLB3-B/MMC_D6-B/IRQ7-DS/AN100 |
| A11 | P03/DA0 | EMLE |
| A12 | AVSS0 | AVSS0 |
| A13 | AVCC0 | AVCC0 |
| B1 | P40/AN000 | P40/IRQ8-DS/AN000 |
| B2 | P44/AN004 | P44/IRQ12-DS/AN004 |
| B3 | PD1/D1[A1/D1]/MTIOC4B/IRQ1 | PD1/D1[A1/D1]/MTIOC4B/POE0#/CTX0/MOSIC/IRQ1/AN109 |
| B4 | PD3/D3[A3/D3]/POE8#/IRQ3 | PD3/D3[A3/D3]/MTIOC8D/POE8#/TOC2/RSPCKC/MMC_D3-B/SDHI_D3-B/QIO3-B/IRQ3/AN111 |
| B5 | PD6/D6[A6/D6]/MTIC5V/POE1#/IRQ6 | PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/SSLC2/MMC_D0-B/SDHI_D0-B/QIO0-B/QMO-B/IRQ6/AN106 |
| B6 | PD7/D7[A7/D7]/MTIC5U/POE0#/IRQ7 | PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3/MMC_D1-B/SDHI_D1-B/QIO1/QMI-B/IRQ7/AN107 |
| B7 | PE3/D11[A11/D11]/MTIOC4B/POE8#/CTS12#/RTS12#/SS12#/AN011/CMPA1 | PE3/D11[A11/D11]/MTIOC4B/PO26/POE8#/TOC3/CTS12#/RTS12#/SS12#/MMC_D7-B/AN101 |
| B8 | VCL | VCL |
| B9 | VREFL | AVSS1 |
| B10 | PJ3/MTIOC3C/CTS6#/RTS6#/SS6# | PJ3/EDACK1/MTIOC3C/CTS6#/RTS6#/CTS0#/RTS0#/SS6#/SS0# |
| B11 | VREFH0 | VREFH0 |
| B12 | P42/AN002 | P42/IRQ10-DS/AN002 |
| B13 | P47/AN007 | P47/IRQ15-DS/AN007 |
| C1 | PD2/D2[A2/D2]/MTIOC4D/IRQ2 | PD2/D2[A2/D2]/MTIOC4D/TIC2/CRX0/MISOC/MMC_D2-B/SDHI_D2-B/QIO2-B/IRQ2/AN110 |

| 100pin TFLGA | RX210 | RX651 |
|---|---|---|
| C2 | PD5/D5[A5/D5]/MTIC5W/POE2#/IRQ5 | PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/SSLC1/MMC_CLK-B/SDHI_CLK-B/QSPCLK-B/IRQ5/AN113 |
| C3 | PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/IRQ5/AN013 | PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/RSPCKB-B/IRQ5/AN103 |
| C4 | PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/AN012/CMPA2 | PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/PO28/SSLB0-B/AN102 |
| C5 | XCIN | XCIN |
| C6 | XCOUT | XCOUT |
| C7 | MD/FINED | MD/FINED |
| C8 | PJ1/MTIOC3A | VBATT |
| C9 | P45/AN005 | P45/IRQ13-DS/AN005 |
| C10 | P46/AN006 | P46/IRQ14-DS/AN006 |
| C11 | PE6/D14[A14/D14]/IRQ6/AN014 | PE6/D14[A14/D14]/MTIOC6C/TIC1/MOSIB-B/MMC_CD-B/SDHI_CD-B/IRQ6/AN104 |
| C12 | PE7/D15[A15/D15]/IRQ7/AN015 | PE7/D15[A15/D15]/MTIOC6A/TOC1/MISOB-B/MMC_RES#-B/SDHI_WP-B/IRQ7/AN105 |
| C13 | PA1/A1/MTIOC0B/MTCLKC/SCK5/SSLA2/CVREFA | PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/PO17/SCK5/SSLA2-B/IRQ11 |
| D1 | PA0/A0/BC0#/MTIOC4A/SSLA1/CACREF | PA0/A0/BC0#/MTIOC4A/MTIOC6D/TIOCA0/CACREF/PO16/SSLA1-B |
| D2 | XTAL/P37 | XTAL/P37 |
| D3 | VSS | VSS |
| D4 | RES# | RES# |
| D5 | P34/MTIOC0A/TMCI3/POE2#/SCK6/IRQ4 | TRST#/P34/MTIOC0A/TMCI3/PO12/POE10#/SCK6/SCK0/IRQ4 |
| D6 | P41/AN001 | P41/IRQ9-DS/AN001 |
| D7 | PA2/A2/RXD5/SMISO5/SSCL5/SSLA3 | PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/SSCL5/SSLA3-B |
| D8 | PA6/A6/MTIC5V/MTCLKB/TMCI3/POE2#/CTS5#/RTS5#/SS5#/MOSIA | PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/POE10#/CTS5#/RTS5#/SS5#/MOSIA-B |
| D9 | PA4/A4/MTIC5U/MTCLKA/TMRI0/TXD5/SMOSI5/SSDA5/SSLA0/IRQ5-DS/CVREFB1 | PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/IRQ5-DS |
| D10 | PA5/A5/RSPCKA | PA5/A5/MTIOC6B/TIOCB1/PO21/RSPCKA-B |
| D11 | PA3/A3/MTIOC0D/MTCLKD/RXD5/SMISO5/SSCL5/IRQ6-DS/CMPB1 | PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19/RXD5/SMISO5/SSCL5/IRQ6-DS |
| D12 | EXTAL/P36 | EXTAL/P36 |
| D13 | VCC | VCC |
| E1 | P35/NMI | UPSEL/P35/NMI |
| E2 | P32/MTIOC0C/TMO3/TXD6/SMOSI6/SSDA6/IRQ2-DS/RTCOUT/RTCIC2 | P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCOUT/RTCIC2/POE0#/POE10#/TXD6/TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/CTX0/USB0_VBUSEN/IRQ2-DS |
| E3 | P12/TMCI1/SCL/IRQ2 | P12/TMCI1/RXD2/SMISO2/SSCL2/SCL0[FM+]/IRQ2 |
| E4 | PB3/A11/MTIOC0A/MTIOC4A/TMO0/POE3#/SCK6 | PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE11#/SCK6/SDSI_D3-B |
| E5 | PB2/A10/CTS6#/RTS6#/SS6# | PB2/A10/TIOCC3/TCLKC/PO26/CTS6#/RTS6#SS6#/SDSI_D2-B |
| E10 | PB0/A8/MTIC5W/RXD6/SMISO6/SSCL6/RSPCKA | PB0/A8/MTIC5W/TIOCA3/PO24/RXD6/SMISO6/SSCL6/IRQ12 |

| 100pin TFLGA | RX210 | RX651 |
|---|---|---|
| E11 | PA7/A7/MISOA | PA7/A7/TIOCB2/PO23/MISOA-B |
| E12 | VSS | VSS |
| E13 | P33/MTIOC0D/TMRI3/POE3#/RXD6/SMISO6/SSCL6/IRQ3-DS | P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/POE4#/POE11#/RXD6/RXD0/SMISO6/SMISO0/SSCL6/SSCL0/CRX0/IRQ3-DS |
| F1 | P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/IRQ1-DS/RTCIC1 | TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS |
| F2 | P30/MTIOC4B/TMRI3/POE8#/RXD1/SMISO1/SSCL1/IRQ0-DS/RTCIC0 | TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS |
| F3 | P27/CS3#/MTIOC2B/TMCI3/SCK1 | TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB-A |
| F4 | BCLK/P53 | P53/BCLK |
| F10 | P52/RD# | P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A |
| F11 | PB5/A13/MTIOC2A/MTIOC1B/TMRI1/POE1#/SCK9 | PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/PO29/POE4#/SCK9/SCK11/SDSI_CLK-B |
| F12 | PB4/A12/CTS9#/RTS9#/SS9# | PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/SS9#/CTS11#/RTS11#/SS11#/SDSI_CMD-B |
| F13 | PB1/A9/MTIOC0C/MTIOC4C/TMCI0/TXD6/SMOSI6/SSDA6/IRQ4-DS | PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/TXD6/SMOSI6/SSDA6/IRQ4-DS |
| G1 | VCC | VCC |
| G2 | P26/CS2#/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1 | TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/MOSIB-A |
| G3 | P25/CS1#/MTIOC4C/MTCLKB/ADTRG0# | P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/ADTRG0# |
| G4 | P16/MTIOC3C/MTIOC3D/TMO2/TXD1/SMOSI1/SSDA1/MOSIA/SCL-DS/IRQ6/RTCOUT/ADTRG0# | P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/SMISO3/SSDA1/SSCL3/SCL2-DS/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB/IRQ6/ADTRG0# |
| G10 | P15/MTIOC0B/MTCLKB/TMCI2/RXD1/SMISO1/SSCL1/IRQ5 | P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/CRX1-DS/IRQ5 |
| G11 | P55/WAIT#/MTIOC4D/TMO3 | P55/WAIT#/EDREQ0/MTIOC4D/TMO3/CRX1/IRQ10 |
| G12 | P54/ALE/MTIOC4B/TMCI1 | P54/ALE/EDACK0/MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/CTX1 |
| G13 | PC7/A23/CS0#/MTIOC3A/TMO2/MTCLKB/TXD8/SMOSI8/SSDA8/MISOA/CACREF | UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/TMO2/TOC0/PO31/CACREF/TXD8/SMOSI8/SSDA8/MISOA-A/TXD10/SMOSI10/SSDA10/IRQ14 |
| H1 | PC6/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/RXD8/SMISO8/SSCL8/MOSIA | PC6/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/TIC0/PO30/RXD8/SMISO8/SSCL8/MOSIA-A/RXD10/SMISO10/SSCL10/IRQ13 |
| H2 | PB6/A14/MTIOC3D/RXD9/SMISO9/SSCL9 | PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/SMISO9/SSCL9/SMISO11/SSCL11/SDSI_D0-B |
| H3 | PB7/A15/MTIOC3B/TXD9/SMOSI9/SSDA9 | PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/SMOSI9/SSDA9/TXD11/SMOSI11/SSDA11/SDSI_D1-B |
| H4 | P24/CS0#/MTIOC4A/MTCLKA/TMRI1 | P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN |

| 100pin TFLGA | RX210 | RX651 |
|---|---|---|
| H10 | P21/MTIOC1B/TMCI0/RXD0/SMISO0/SSCL0 | P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/USB0_EXICEN/IRQ9 |
| H11 | P17/MTIOC3A/MTIOC3B/TMO1/POE8#/SCK1/MISOA/SDA-DS/IRQ7 | P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/IRQ7/ADTRG1# |
| H12 | P13/MTIOC0B/TMO3/SDA/IRQ3 | P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG1# |
| H13 | PH0/CACREF | VSS_USB |
| J1 | PH3/TMCI0 | VCC_USB |
| J2 | P50/WR0#/WR# | P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1-A |
| J3 | PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0 | PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0-A/CTS10#/RTS10#/SS10# |
| J4 | PC0/A16/MTIOC3C/CTS5#/RTS5#/SS5#/SSLA1 | PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/SS5#/SSLA1-A/IRQ14 |
| J10 | PC1/A17/MTIOC3A/SCK5/SSLA2 | PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/SSLA2-A/IRQ12 |
| J11 | P23/MTIOC3D/MTCLKD/CTS0#/RTS0#/SS0# | P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/SSDA3 |
| J12 | P22/MTIOC3B/MTCLKC/TMO0/SCK0 | P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0/USB0_OVRCURB |
| J13 | P20/MTIOC1A/TMRI0/TXD0/SMOSI0/SSDA0 | P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/USB0_ID/IRQ8 |
| K1 | P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/RTS1#/SS1#/IRQ4 | P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_OVRCURA/IRQ4 |
| K2 | PH2/TMRI0/IRQ1 | USB0_DM |
| K3 | PH1/TMO0/IRQ0 | USB0_DP |
| K4 | P51/WR1#/BC1#/WAIT# | P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A |
| K5 | PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TMRI2/SCK8/RSPCKA | PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TMRI2/PO29/SCK8/RSPCKA-A/SCK10 |
| K6 | PC3/A19/MTIOC4D/TXD5/SMOSI5/SSDA5 | PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/SMOSI5/SSDA5 |
| K7 | PC2/A18/MTIOC4B/RXD5/SMISO5/SSCL5/SSLA3 | PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/SMISO5/SSCL5/SSLA3-A |
| K8 | P05/DA1 | P05/IRQ13/DA1 |
| K9 | VREFH | AVCC1 |
| K10 | P07/ADTRG0# | P07/IRQ15/ADTRG0# |

# 4. Notes on Migration

There are some notes about difference between RX210 Group and RX651 Group.

Description about the Hardware, there is on the < Chapter 4.1 Notes on Pin Design >.

Description about the Software, there is on the <Chapter 4.2 Notes on Function Setting>.

## 4.1 Notes on Pin Design

### 4.1.1 Operating Modes

The Operating mode has difference between RX210 Group and RX651 Group.

On the RX651 Group, the chip starts up in boot mode (FINE interface) when the MD pin is set to the low level at the time of release from the reset state and then is then switched to the high level within 20 to 100 msec.

**Table 4.1 Comparative Listing of Operating Modes**

| RX210 | | | RX651 | | |
|---|---|---|---|---|---|
| MD1 | PC7 | Operating modes | MD | UB | Operating modes |
| 0 | 0 | Boot mode | 0 | 0 | Boot mode (SCI Interface) |
| 0 | 1 | User boot mode | 0 | 1 | Boot mode (USB Interface) |
| — | — | — | 0->1 | 0 | Boot mode (FINE Interface) |
| 1 | — | Single chip mode | 1 | — | Single chip mode |

### 4.1.2 VCL Pin (External Capacitor)

Connect a smoothing capacitor rated at 0.22 µF to the VCL pin of the RX651 Group for stabilization of the internal power supply.

### 4.1.3 VBATT Pin

On the RX651 Group, when the voltage at the VCC pin is dropped, power can be supplied to the realtime clock (RTC) and sub-clock oscillator from the dedicated battery backup power pin (VBATT pin).

Connect the VBATT pin to the VCC pin when do not use the battery backup function or do not use Sub-clock oscillator with realtime-clock (RTC).

### 4.1.4 Main Clock Oscillator

When connecting an oscillator to EXTAL pin and XTAL pin of RX651 Group, frequency should be in a range of 8 MHz to 24 MHz

On the RX651 Group, EXTAL pin and XTAL pin can not be used as General I/O ports.

## 4.2 Notes on Function Settings

### 4.2.1 Notes on Using Power-On Reset and PLL Circuit Together

On the RX651 Group, when using a power-on reset and the PLL circuit together, set the LVD1CR1.LVD1IDTSEL[1:0] bits or LVD2CR1.LVD2IDTSEL[1:0] bits to 01b, and select the voltage monitoring interrupt to be generated when a drop (Vcc < Vdet) is detected.
In addition, at the beginning of the interrupt handling routine, set the SCKCR3.CKSEL[2:0] bits to a value other than 100b to select a clock source other than the PLL circuit, then set the PLLCR2.PLLEN bit to 1 to stop the PLL circuit.

### 4.2.2 Data for Programming Reserved Areas and Reserved Bits in the Option-Setting Memory

On the RX651 Group, when reserved areas and reserved bits in the option-setting memory are within the scope of programming, write 1 as the value for all bits of reserved areas and all reserved bits. Normal operation cannot be guaranteed if 0 is written to such bits.

### 4.2.3 Point for Caution when Shifting from Low-Speed Operating Mode to Software Standby Mode

On the RX651 Group, on return from software standby, the chip enters high-speed operating mode. Even if a WAIT instruction is executed in low-speed operating mode, if generation of the return interrupt precedes completion of the transition to software standby and processing for the transition is canceled, the chip does not return to the mode before execution of the WAIT instruction. If this creates a problem, set the OPCCR.OPCM[2:0] bits to 000b during processing of the return interrupt.

### 4.2.4 Interrupt Requests in Software Standby Mode

On the RX651 Group, when an interrupt request occurs in software standby mode but the interrupt source is not set as a source for exiting software standby mode, the request is held in the ICU. The request is handled after exiting by another interrupt source.

Note that the interrupt request for the external pin interrupt is not held.

### 4.2.5 Setting Value of the Port Direction Register (PDR) for each Packages

In the RX651 Group, the initialization of the reserved bits of the Port Direction Register (PDR), refer to the User's Manual <Chapter 22.4 Initialization of the Port Direction Register>

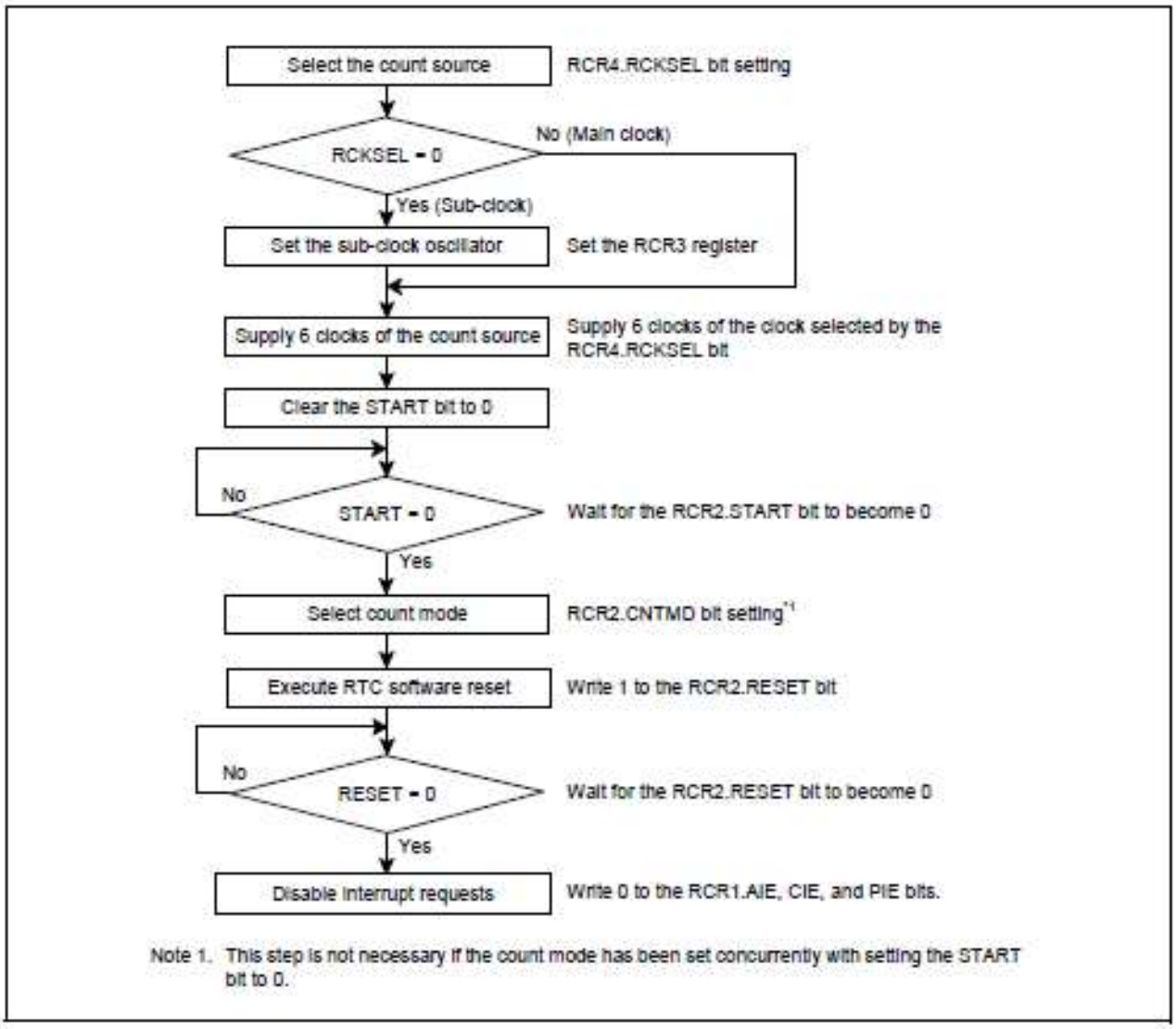
### 4.2.6 Initialization Procedure When the Realtime Clock is Not to be Used

On the RX651 Group, registers in the RTC are not initialized by a reset. Accordingly, depending on the initial state, the generation of an unintentional interrupt request or operation of the counter may lead to increased power consumption.

For products that do not require a realtime clock, initialize the registers.

Alternatively, when the sub-clock is not used as the system clock or realtime clock, the counter can be stopped by writing 0 (sub-clock oscillator is selected) to the RCR4.RCKSEL bit and stopping the sub-clock.

When making the setting to stop the sub-clock, write 0 to the RCR3.RTCEN bit and write 1 to the SOSCCR.SOSTP bit.




### 4.2.7 Note on Transmit Enable Bit (TE Bit)

On the RX651 Group, when setting the SCR.TE bit to 0 (serial transmission is disabled) while the pin function is "TXDn", output of the pin becomes high impedance.

Prevent the TXDn line from becoming high impedance by any of the following ways:

(1) Connect a pull-up resistor to the TXDn line.
(2) Change the pin function to "general-purpose I/O port, output" before setting the SCR.TE bit to 0.

Set the SCR.TE bit to 1 before changing the pin function to "TXDn".

### 4.2.8 Note on Stopping Reception When Using the RTS Function in Asynchronous Mode

On the RX651 Group, one clock cycle of PCLK is required for the time from setting the SCR.RE bit to 0 to stopping the RTS signal generator in asynchronous mode.

When reading the RDR (or RDRL) register after setting the SCR.RE bit to 0, confirm that the RE bit has been set to 0 before reading the RDR (or RDRL) register to prevent these two processes from being performed consecutively.

### 4.2.9 S12AD A/D Conversion Restarting Timing and Termination Timing

It takes a maximum of six ADCLK cycles (in case of RX210 four cycles) for the idle analog unit of the 12-bit A/D converter to be restarted by setting the ADCSR.ADST bit to 1. It takes a maximum of two ADCLK cycles for the operating analog unit of the 12-bit A/D converter to be terminated by setting the ADCSR.ADST bit to 0.

### 4.2.10 S12AD 12Pin Setting When Using the 12-bit A/D Converter

When using the 12-bit A/D converter unit 0, do not use the P40 to P47, P03, P05, and P07 pins as output pins. We also recommend not using the P00 to P02, P90 to P930, PD0 to PD7, and PE0 to PE7 pins as output pins. If any of the P00 to P02, P90 to P93, PD0 to PD7, and PE0 to PE7 pins is used for an output pin, perform A/D conversion several times, eliminate the maximum and minimum values, and obtain the average of the other results.

When using the 12-bit A/D conversion unit1, we recommend not using the P00 to P02, P90 to P93, PD0 to PD7, and PE0 to PE7 pins as output pins. If any of the P00 to P02, P90 to P93, PD0 to PD7, and PE0 to PE7 pins is used for an output pins, perform A/D conversion several times, eliminate the maximum and minimum values, and obtain the average of the other results.

### 4.2.11 S12AD Caution When Using an External Bus

On the RX651 Group, A/D conversion at the same time as access to an external bus may produce poor results.

In this case, use a software approach, such as performing A/D conversion several times, then obtaining the average after excluding the highest and lowest values.

### 4.2.12 Note on Usage When Measure against Interference between D/A and A/D Conversion is Enabled

On the RX651 Group, when the DAADSCR.DAADST bit is 1 (measure against interference between D/A and A/D conversion is enabled), do not place the 12-bit A/D converter (unit 1) in the module stop state. It may halt D/A conversion in addition to A/D conversion.

### 4.2.13 D/A Note on Event Link Operation

On the RX651 Group, when the event link function is used, do not use output buffer amplifier.

### 4.2.14 Initial Setting Procedure when the Output Buffer Amplifier is Used

On the RX651 Group, when using the output buffer amplifier, enable the amplifier output in the following procedure. An example for channel 0 is described below.

(1) Confirm that the DACR.DAE and DACR.DAE0 bits are 0.
(2) Write 0000h to the DACR0 register.
(3) Set the DAA.SWCR.DAASW0 bit to 1.
(4) Set the DAA.SWCR.DAAMP0 bit to 1.
(5) Set the DACR.DAE or DACR.DAOE0 bit to 1. The output buffer amplifier starts the operation.
(6) Wait for at least 3 μs and then set the DAAWCR.DAASW0 bit to 0.
(7) Write a value to be converted in the DADR0 register.

While the output buffer amplifier is operating, setting the DACR.DAE and DACR.DAOE bits to 0 disables the output buffer amplifier. Repeat the procedure from (1) to (7) to use the output buffer amplifier again.

### 4.2.15 Supplementary Explanation on RAM Self-Test

On the RX651 Group, when a value is written to RAM and then execute a read access to the same address, the value may be read from the buffer, not from the RAM.

Perform the following operation to ensure that a value will be read from RAM.

To read RAM data at an address of 4-aligned bytes (*) after writing a value to the RAM address of the same 4-aligned bytes:

Write a value to any other RAM address which is out of the 4-aligned bytes, and then execute a read access to the RAM address where you want to read.

### 4.2.16 Setting Number of Flash Memory Access Wait States

On the RX651 Group it is necessary to specify the number of access wait states to be used when accessing the flash memory, based on the system clock (ICLK) frequency of the microcontroller. This setting is made to the ROMWT register.

Table 4.2 shows The Number of Flash Memory Access Wait States.

**Table 4.2 The Number of Flash Memory Access Wait States**

| Item | ICLK ≤ 50 MHz | 50 MHz < ICLK ≤ 100 MHz | 100 MHz < |
|---|---|---|---|
| Wait states | 0 to 2 | 1 or 2 | 2 |

### 4.2.17 Transferring Firmware to the FCU RAM

On the RX210 Group, FCU commands could only be used if the FCU RAM holds the firmware for the FCU. However, this is not necessary on the RX651 Group.

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### 4.2.18 Command of Flash Memory Usage

On the RX210 Group, the Flash memory can be programmed or erased by issuing FCU commands to FCU.

On the RX651 Group, the Flash memory can be programmed or erased by setting the FACI commands specified in the FACI command issuing area and by controlling the FCU.

Table 4.3 shows The Specification Comparison Between FCU Commands and FACI Commands

**Table 4.3 The Specification Comparison Between FCU Commands and FACI Commands**

| Item | FCU Commands (RX210) | FACI commands (RX651) |
|---|---|---|
| Command issuing area | Address for programming/erasure (00E0 0000h to 00FF FFFFh) | FACI command issuing area (007E 0000h) |
| Available commands | • P/E normal mode transition<br>• Status read mode transition<br>• Lock bit read mode transition<br>• Peripheral clock notification<br>• Programming<br>• Block erase<br>• P/E suspend<br>• P/E resume<br>• Status register clear<br>• Lock bit read 2<br>• Lock bit programming<br>• Blank checking | • Program<br>• Block erase<br>• P/E suspend<br>• P/E resume<br>• Status clear<br>• Forced stop<br>• Configuration setting |

### 4.2.19 Note of ID Code Protection

On the RX210 Group, when the control code is 52h and the ID code is 50h, 72h, 6Fh, 74h, 65h, 63h, 74h, FFh, ..., FFh (from the ID code 1 field), there is no determination of matching and the ID code is always considered to be non-matching. Accordingly, reading, programming, and erasure from the host are prohibited.

On the RX65N Group, when the On-Chip Debugger is connected, the ID Code is authenticated regardless of the setting of SPCC.SPE. For details of ID code authentication operation please refer to RENESAS TECHINICAL UPDATE (TN-RX*-A166A/E)

## 5. Reference Documents

User's Manual: Hardware

RX210 Group User's Manual: Hardware Rev.1.50 (R01UH0037EJ0150)
(The latest version can be downloaded from the Renesas Electronics website.)

RX65N Group, RX651 Group User's Manual: Hardware Rev.1.00 (R01UH0590EJ0100)
(The latest version can be downloaded from the Renesas Electronics website.)

RX65N Group, RX651 Group Flash Memory User's Manual: Hardware Interface Rev.1.00 (R01UH0602EJ0100)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News
(The latest version can be downloaded from the Renesas Electronics website.)

## Related Technical Updates

This module reflects the content of the following technical updates.

- TN-RX*-A164A/E
- TN-RX*-A165A/E
- TN-RX*-A166A/E
- TN-RX*-A173A/E
- TN-RX*-A176A/E

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| | | Description | |
|---|---|---|---|
| **Rev.** | **Date** | **Page** | **Summary** |
| 1.00 | Sep. 21, 2018 | — | First edition issued |

## General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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