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# **H8SX Family**

# Outputting Two Groups of 4-Bit Signals

## Introduction

Asynchronous pulses are output as two groups of 4-bit signals by using the programmable pulse generator (PPG) outputs.

# **Target Device**

H8SX/1653F

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# 1. Specifications

- Asynchronous pulses are output as two groups of 4-bit signals by using the programmable pulse generator (PPG) outputs as shown in figure 1.
- The PPG is activated by compare match of the timer pulse unit (TPU).

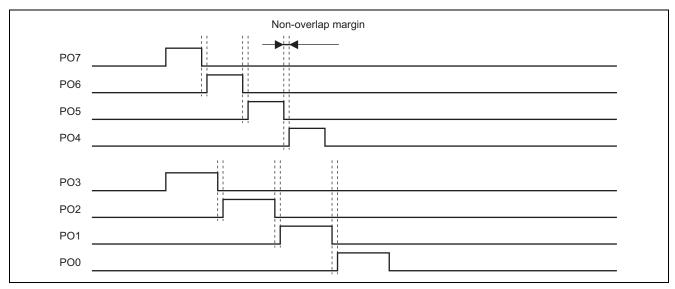


Figure 1 Example Output of Two Groups of 4-Bit Signals



# 2. Conditions for Application

# Table 1 Conditions for Application

Item	Contents		
Operating frequency	Input clock:	16 MHz	
	System clock (Iφ):	16 MHz	
	Peripheral module clock (Pφ):	16 MHz	
	External bus clock (Βφ):	16 MHz	
Operating mode	Mode 6 (MD2 = 1, MD1 = 1, MD0 = 0)		
	MD_CLK = 0		
Development tool	High-performance Embedded Workshop Version 4.00.02		
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler Version 6.01.00		
	(from Renesas Technology Corp.)		
Compile option	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3, -speed = (register, shift, struct, expression)		

## Table 2 Section Settings

Address	Section Name	Description
H'001000	Р	Program area
	С	Data table storage
H'FF2000	В	Non-initialized data area (RAM area)



## 3. Description of Modules Used

In this sample task, asynchronous pulses are output as two groups of 4-bit signals using channels 0 and 1 of the TPU and PPG output groups 0 and 1.

Figure 2 shows a block diagram of the pulse output generation using TPU channels 0, 1 and PPG groups 0, 1. This sample task uses the following features of the TPU and PPG.

- An output trigger signal can be selected for each 4-bit group and up to two 4-bit groups can be output.
- An output trigger signal can be selected for each group from among the compare-match signals on the four channels
  of the TPU.
- A non-overlapping margin can be set between the multiple pulse outputs.

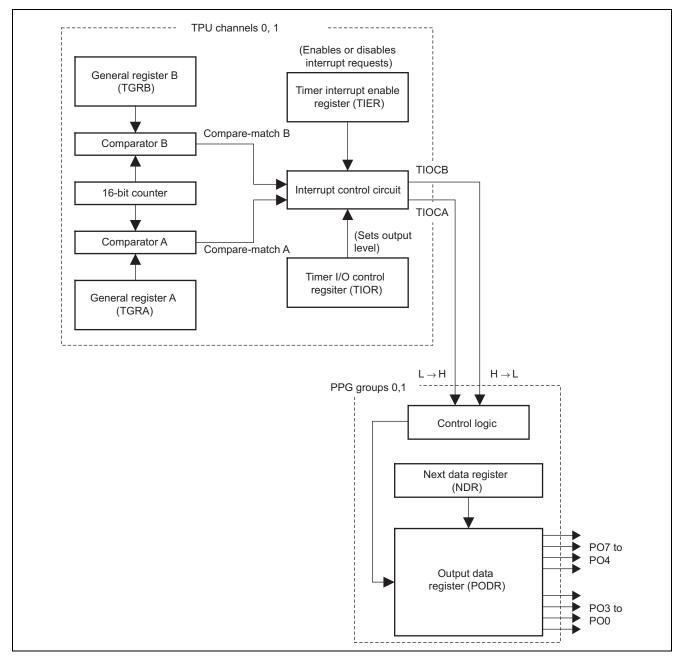


Figure 2 Block Diagram of the Output of Two 4-Bit Signals (Groups 0 and 1)



# 4. Description of Operation

Figure 3 illustrates the principles of the data output operation using PPG output group 0 as an example. The hardware processing and software processing of figure 3 are explained in table 3.

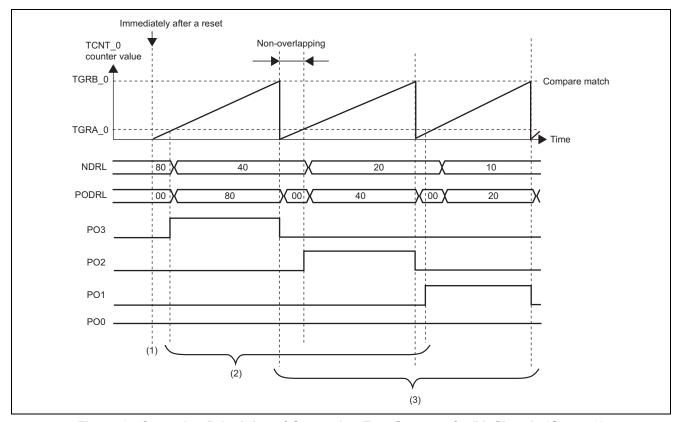


Figure 3 Operation Principles of Outputting Two Groups of 4-Bit Signals (Group 0)



## Table 3 Hardware and Software Processing

	Hardware Processing	Software Processing
(1)	No processing	Initial settings
		Processing for the TPU:
		(a) Set the non-overlapping margin in TGRA_0 and the PPG output trigger cycle in TGRB_0.
		(b) Set up the TGIA interrupt.
		(c) Start counting by TPU0 and TPU1.
		Processing for the PPG:
		(a) Set the initial output value in PODRL, and set up the PPG output.
		(b) Enable the PPG group 0 output, and select the trigger for transfer.
		(c) Select non-overlap operation for group 0.
		(d) Set the next pulse output value in NDRL.
(2)	(a) Generate the TGRA_0 compare-match	TGI0A interrupt processing
	signal.	(a) Set the next output data in the upper 4 bits of NDRL.
	(b) Transfer the value in NDRL to PODRL.	
	(c) Output 4-bit data from the group 0 output pins of the PPG.	
(3)	(a) Generate the TGRB_0 compare-match signal.	No processing
	(b) Generate non-overlapping PPG outputs.	



# 5. Description of Software

## 5.1 List of Functions

#### Table 4 List of Functions

<b>Function Name</b>	Functions
init	Initialization routine
	Cancels module stop mode, sets the clock, and calls the main function.
main	Main routine
	Initializes the PPG and TPU.
tgi0a_int	Sets the data to be output next in the lower 4 bits of NDRL (group 0).
tgi1a_int Sets the data to be output next in the upper 4 bits of NDRL (group 1).	

## 5.2 Arguments

This sample task does not use arguments.

# 5.3 Vector Table

**Table 5 Exception Handling Vector Table** 

<b>Exception Handling</b>			Exception Handling
Source	Vector Number	Vector Table Address	Routine
Reset	0	H'000000	init
TPU_0 TGI0A	88	H'000160	tgi0a_int
TPU_1 TGI1A	93	H'000174	tgi1a_int

# 5.4 RAM Usage

### Table 6 RAM Usage

Туре	Variable Name	Description	Used In
unsigned char	cnt0	Transfer counter for PPG group 0 output	main, tgi0a_int
unsigned char	cnt1	Transfer counter for PPG group 1 output	main, tgi1a_int



## 5.5 Data Table

Table 7 Description of Data Table

Type	Array Name	Description	Used In
unsigned char	ndat_tab0[5]	Stores the data to be output as PPG group 0.	main, tgi0a_int
		{0xF8, 0xF4, 0xF2, 0xF1, 0xF0}	
unsigned char	ndat_tab1[5]	Stores the data to be output as PPG group 1.	main, tgi1a_int
		{0x8F, 0x4F, 0x2F, 0x1F, 0x0F}	

# 5.6 Internal Registers

The internal registers used in this sample task are described in table 8.

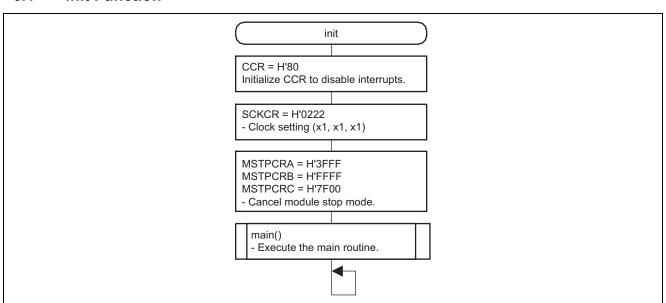
Table 8 Description of Internal Registers

Register Name		Function
PPG	PMR	Specifies PO7 to PO4 and PO3 to PO0 for non-overlapping outputs.
	PCR	Selects a pulse output trigger signal for each group.
		Group 1: Compare match on TPU channel 1
		Group 0: Compare match on TPU channel 0
	NDERL	Enables PPG outputs on PO7 to PO4 and PO3 to PO0.
	PODRL	The value in NDRL is transferred here and output from PO7 to PO4 and PO3 to PO0.
	NDRL	Sets the next pattern to be output on PO7 to PO4 and PO3 to PO0.
TPU	TGRA_0, TGRA_1	These registers set non-overlapping margins.
	TGRB_0, TGRB_1	These registers set PPG output trigger cycles.
	TCR_0, TCR_1	These registers are set such that
		the corresponding counters are cleared upon compare match with TGRB, and counting is driven by internal clock P $\phi$ .
	TSR_0, TSR_1	These registers indicate the occurrence of compare match.
	TIER_0, TIER_1	These registers enable TGIA interrupts.
	TSTR	Enables counting by TCNT.
MSTPCRA, M	STPCRB, MSTPCRC	These registers cancel module stop mode of the TPU and PPG.
SCKCR		Sets the frequency multipliers for Iφ, Pφ, and Bφ.



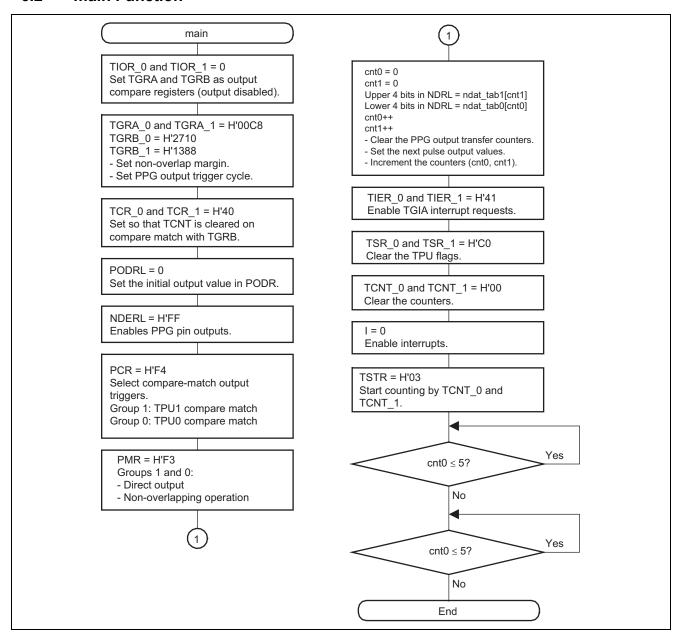
## 6. Flowchart

## 6.1 init Function



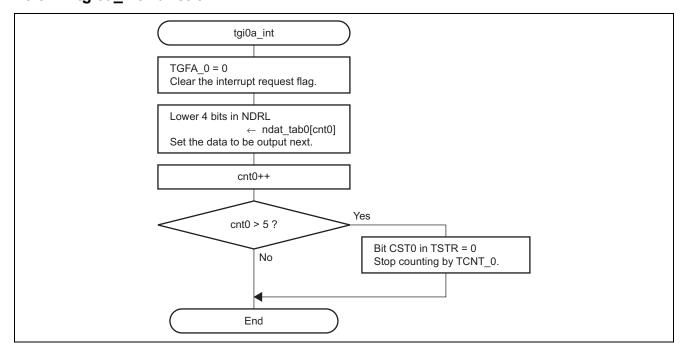


### 6.2 main Function

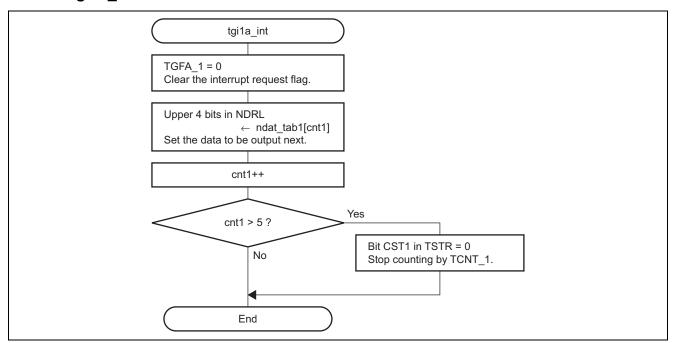




# 6.3 tgi0a\_int Function



# 6.4 tgi1a\_int Function





# **Revision Record**

		Descript	tion	
Rev.	Date	Page	Summary	
1.00	Mar.10.06	_	First edition issued	



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