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April 1st, 2010
Renesas Electronics Corporation

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M16C/62A Group

Operation of SI/O3,4

1.0 Abstract

In transmitting data in this mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

Table 1. Chosen functions

Item	Set-up	Item	Set-up
Transfer clock source	<input type="radio"/> Internal clock (f ₁ / f ₈ / f ₃₂)	SOUTi initial value set function	<input type="radio"/> Not used
	<input type="radio"/> External clock (CLKi pin)		<input type="radio"/> Used
Transfer clock	<input type="radio"/> LSB first		
	<input type="radio"/> MSB first		

2.0 Introduction

Operation (1) Transfer begins upon writing the SI/Oi transmit data.

The transmit data is sent out from the S_{OUTi} pin synchronously with falling edges of the transfer clock.

(2) When S_{OUT} finishes sending one byte of data, the interrupt request bit is set to 1.

(3) After the transfer is completed, S_{OUT} holds the last data for a 1/2 transfer clock period before going to a high-impedance state.

Note

- Do not write data to the SI/Oi transmit/receive register (i = 3, 4; addresses 0360₁₆, 0364₁₆) during a transfer.
- Data can only be written to the SI/Oi transmit/receive register when the device is idle neither sending nor receiving data.

Figure 1 shows the operation timing

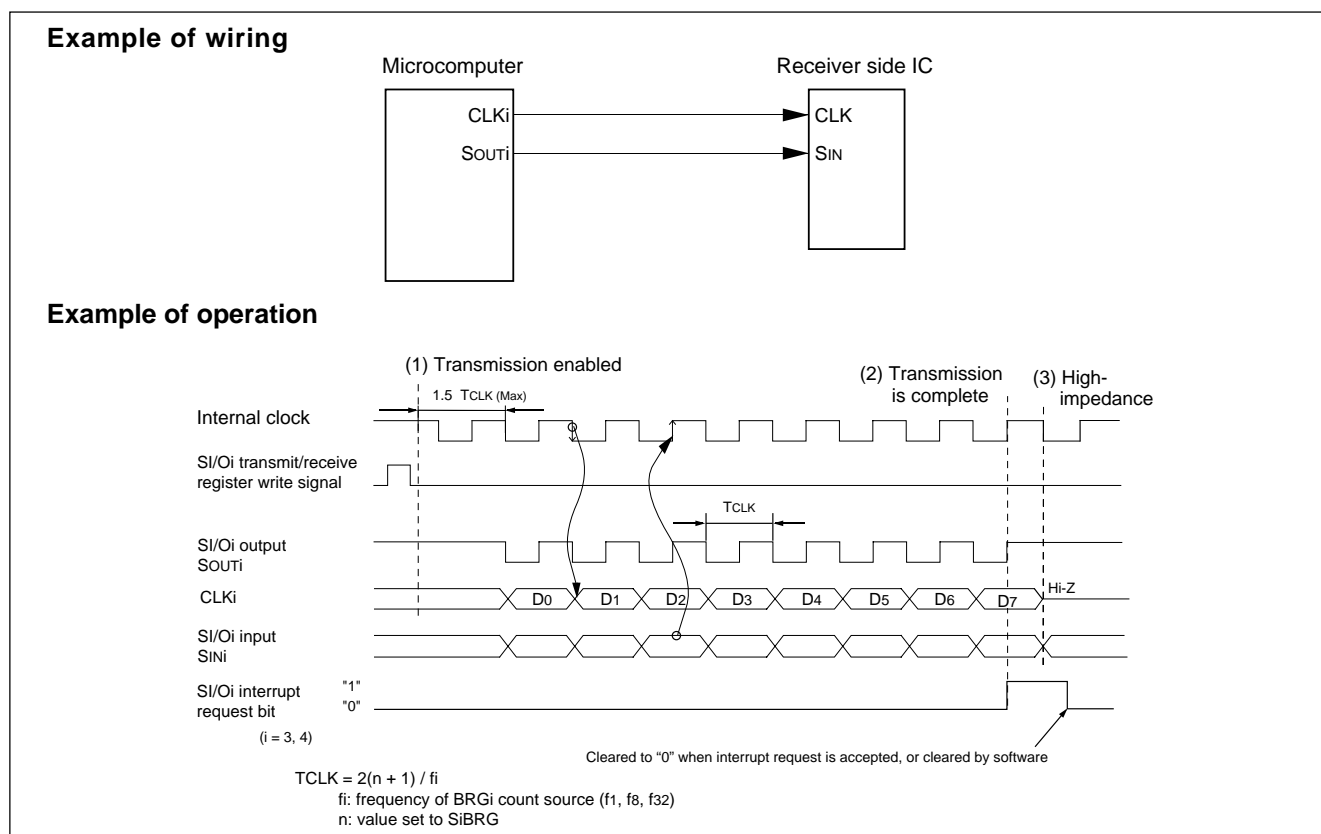
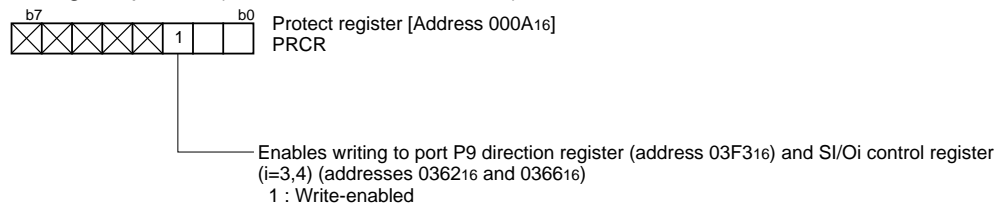


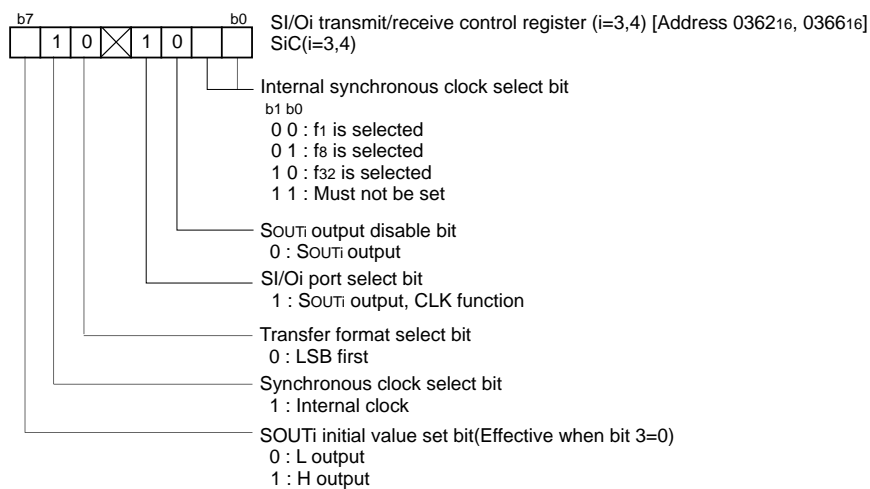
Figure 1. Operation timing of transmission in SI/O3, 4 mode

3.0 Set-up procedure

Clearing the protect (set to write-enabled state)

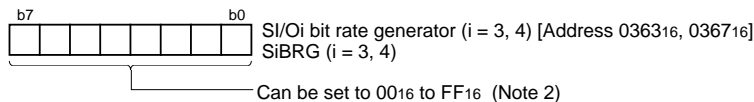


Setting SI/Oi transmit/receive control register (i=3, 4)



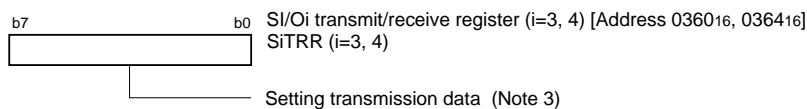
Note 1: Be sure to set the protect register and SI/Oi control register successively.

Setting SI/Oi bit rate generator (i = 3, 4)

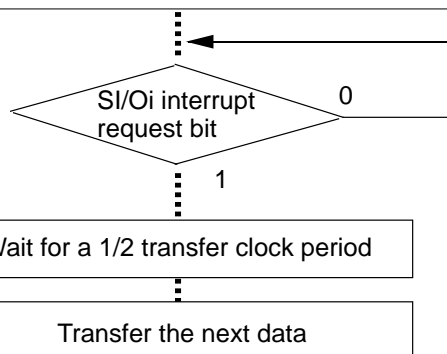


Note 2: Write to SI/Oi bit rate generator when transmission/reception is halted.

Writing transmit data



Note 3: Write to SI/Oi transmit/receive register when transmission/reception is halted.



4.0 Programming Code

```

;*****
;
; M16C/62A Program Collection
;
; FILE NAME : rjj05b0052_src.a30
; CPU      : M16C/62A Group
; FUNCTION  : Operation of SI/O3,4
; HISTORY   : 2003.05.16 Ver 1.00
;
; Copyright(C)2003, Renesas Technology Corp.
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;
;*****
;*****
; Include
;*****
;      .LIST      OFF      ;Stops outputting lines to the assembler list file
;      .INCLUDE    sfr62a.inc ;Reads the file that defined SFR
;      .LIST      ON      ;Starts outputting lines to the assembler list file
;
;*****
;      Symbol definition
;*****
RAM_TOP      .EQU    00400H    ;Start address of RAM
RAM_END      .EQU    00FFFH    ;End address of RAM
ROM_TOP      .EQU    0F8000H   ;Start address of ROM
FIXED_VECT_TOP .EQU    0FFFDCH  ;Start address of fixed vector
;
;*****
;      Allocation of work RAM area
;*****
;      .SECTION    WORKRAM, DATA
;      .ORG        RAM_TOP
WORKRAM_TOP:
C_POWER      .EQU    3
C_DATA_SIZE  .EQU    (1<< C_POWER) ;Data size
v_Trans_data: .BLKB   C_DATA_SIZE  ;Area of send data for sample
WORKRAM_END:
;
;*****
;      Program area
;*****
;=====
;      Start up
;=====
;      .SECTION    PROGRAM, CODE ;Declares section name and section type
;      .ORG        ROM_TOP      ;Declares start address
RESET:
MOV.B        #03H, prcr          ;Removes protect
;                               ;Set processor mode registers 0 and 1
MOV.B        #00000000B, pm0     ; Single-chip mode
MOV.B        #00000000B, pm1     ; No expansion, No wait
;                               ;Set system clock control registers 0 and 1
MOV.B        #00001000B, cm0     ; Xcin-Xcout High
MOV.B        #00100000B, cm1     ; Xin-Xout High, Main clock is No divison
MOV.B        #00H, prcr          ;Protects all registers
;

```

```

; Clears WORKRAM area
MOV.W    #0, R0
MOV.W    #(RAM_END-RAM_TOP)/2, R3
MOV.W    #WORKRAM_TOP, A1
SSTR.W

; Makes transmit data for sample ( 1 to C_DATA_SIZE )
MOV.B    #1, R0L           ;1st data
MOV.W    #0, A0           ;Initialize offset address
MAKE_DATA:
;
MOV.B    R0L, v_Trans_data[A0] ;
ADD.B    #1, R0L           ;
ADD.W    #1, A0           ;
CMP.W    #C_DATA_SIZE, A0   ;
JLTU     MAKE_DATA         ;
;
;=====
;      SI/O3,4
;=====
MOV.B    #00h, s3ic        ;Disabled SI/O3 interrupt and
                           ;clear interrupt request bit to "0"
;
; Be sure to set the protect register and SI/Oi control register successively
MOV.B    #00000100B, prcr   ;Clearing the protect
;
;      +-----;Write-enabled (SI/Oi control register)
MOV.B    #01001000B, s3c    ;Setting SI/O3 transmit/receive control register
;
;      || | |++-----;Internal synchronous clock select bit (00:f1 is selected)
;      || | |++-----;SOUTi output disable bit (0:SOUTi output)
;      || | |++-----;SI/Oi port select bit (1:SOUTi output,CLK function)
;      || | |++-----;Transfer format select bit (0:LSB first)
;      || | |++-----;Synchronous clock select bit (1:Internal clock)
;      || | |++-----;SOUTi initial value set bit (Effective when bit 3 = 0)
MOV.B    #07H, s3brg        ;Setting SI/O3 bit rate generator (1MHz, @16MHz f1)
;
;=====
;      Main program
;=====
MOV.W    #0, A0           ; Initialize offset
; Writing transmit data --> Transfer begins
WRITE_DATA:
MOV.B    v_Trans_data[A0], s3trr
;
CHK_SIO_INT:
; Check SI/O interrupt request
BTST     ir_s3ic
JNC      CHK_SIO_INT
; Wait for a 1/2 transfer clock period
; (ex.)
; In this sample, wait for a 1/2 transfer clock period by the following instructions.
; where, f1=16MHz is selected for synchronous clock and transfer rate=1MHz
MOV.B    #00, s3ic        ;Clear interrupt request bit
;
PREPARE_NEXT_DATA:
ADD.W    #1, A0
AND.W    #(C_DATA_SIZE-1), A0
JNZ      WRITE_DATA
;
COMPLETE_TRANS:
JMP      COMPLETE_TRANS
;

```

```

=====
;      Dummy interrupt processing program
=====
dummy:
    REIT
;
;*****
;      Setting of fixed vector
;*****
    .SECTION    F_VECT, ROMDATA
    .ORG        FIXED_VECT_TOP
;
    .LWORD     dummy    ;Undefined instruction interrupt vector
    .LWORD     dummy    ;Overflow (INT0 instruction) interrupt vector
    .LWORD     dummy    ;BRK instruction interrupt vector
    .LWORD     dummy    ;Address match interrupt vector
    .LWORD     dummy    ;Single-step interrupt vector
    .LWORD     dummy    ;Watchdog timer interrupt vector
    .LWORD     dummy    ;DBC interrupt vector
    .LWORD     dummy    ;NMI interrupt vector
    .LWORD     RESET    ;Sets reset vector
;
    .END

```

5.0 Reference

Renesas Technology Corporation Semiconductor Home page
<http://www.renesas.com/>

Technical Support

E-mail: support_apl@renesas.com

Data Sheet

M16C/62A group Rev. C.1
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User's Manual

M16C/62A group Rev. 1.0
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